Understanding output voltage limitations of DC/DC buck converters

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Low Power DC/DC Applications

Introduction

Product datasheets for DC/DC converters typically show an operating range for input and output voltages. These operating ranges may be broad and in some cases may overlap. It is usually not possible to derive any arbitrary output voltage from the entire range of permissible input voltages. There are several factors that can cause this, including the internal reference voltage, the minimum controllable ON time, and the maximum duty-cycle constraints.

Ideal buck-converter operation

Consider the theoretical, ideal buck converter shown in Figure 1. The buck converter is used to generate a lower output voltage from a higher DC input voltage.

If the losses in the switch and catch diode are ignored, then the duty cycle, or the ratio of ON time to the total period, of the converter can be expressed as

$$D = \frac{V_{OUT}}{V_{IN}}. \tag{1}$$

The duty cycle is determined by the output of the error amplifier and the PWM ramp voltage as shown in Figure 2. The ON time starts on the falling edge of the PWM ramp voltage and stops when the ramp voltage equals the output voltage of the error amplifier. The output of the error amplifier in turn is set so that the feedback portion of the output voltage is equal to the internal reference voltage. This closed-loop feedback system causes the output voltage to regulate at the desired level. If the output of the

Figure 1. Theoretical, ideal buck converter

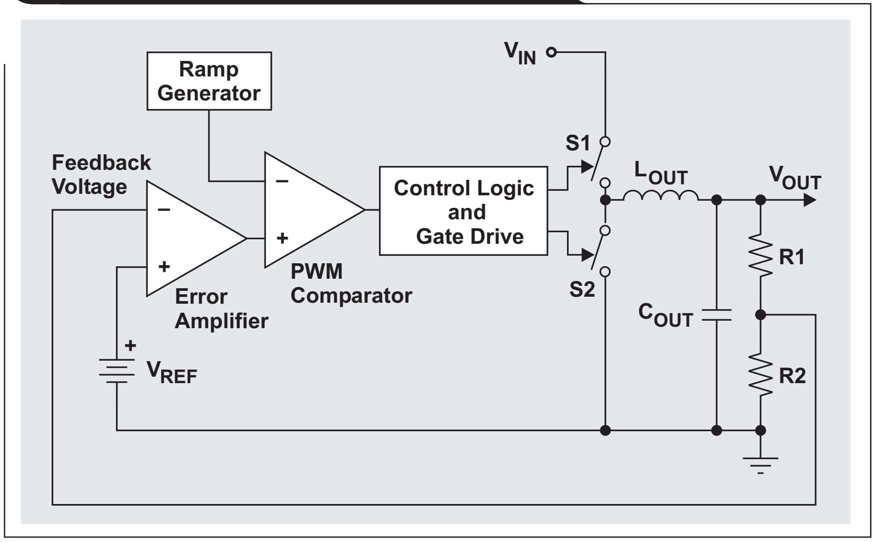
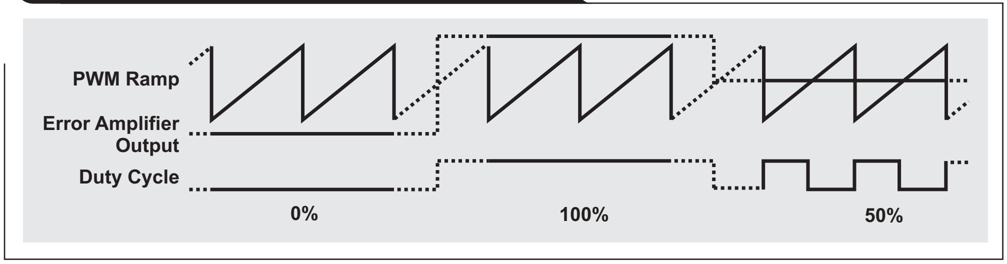


Figure 2. Typical PWM waveforms at duty-cycle extremes and midpoint



error amplifier falls below the PWM ramp minimum, then a 0% duty cycle is commanded, the converter will not switch, and the output voltage is 0 V. If the error-amplifier output is above the PWM ramp peak, then the commanded duty cycle is 100% and the output voltage is equal to the input voltage. For error-amplifier outputs between these two extremes, the output voltage will regulate to

$$V_{OUT} = D \times V_{IN}. \tag{2}$$

Practical limitations

For the ideal buck converter, any output voltage from 0 V to V_{IN} may be obtained. In actual DC/DC converter circuits, there are practical limitations. It has been shown that the output voltage is proportional to the duty cycle and input voltage. Given a particular input voltage, there are limitations that prevent the duty cycle from covering the entire range from 0 to 100%. Most obvious is the internal reference voltage, V_{REF}. Normally, a resistor divider network as shown in Figure 1 is used to feed back a portion of the output voltage to the inverting terminal of the error amplifier. This voltage is compared to V_{REF}; and, during steady-state regulation, the error-amplifier output will not go below the voltage required to maintain the feedback voltage equal to V_{REF}. So the output voltage will be

$$V_{OUT} = V_{REF}\left(\frac{R1}{R2} + 1\right). \tag{3}$$

As R2 approaches infinity, the output voltage goes to V_{REF} so that the output cannot be regulated to below the reference voltage.

There may also be constraints on the minimum controllable ON time. This may be caused by limitations in the gate-drive circuitry or by intentional delays. This minimum controllable ON time puts an additional constraint on the minimum achievable V_{OUT}:

$$V_{OUT(min)} = t_{on(min)} \times V_{IN} \times f_s, \tag{4}$$

where $t_{on(min)}$ is the minimum controllable ON time and f_s is the switching frequency.

The duty cycle may also be constrained at the upper end. In many converters, a dead time is required to charge the high-side switching FET gate-drive circuit. Feedforward circuitry may also cause a flattening of the PWM ramp waveform as the slope of the PWM ramp is increased while the period remains constant. This will limit the maximum output voltage with respect to V_{IN}. Typically, if there is a maximum duty-cycle limit, it will be expressed as a percentage, and the maximum output voltage will be

$$V_{OUT(max)} = V_{IN} \times D_{max}. \tag{5}$$

Effect of circuit losses

So far we have assumed that the components in the circuit are ideal and lossless. Of course, this is not the case. There are conduction losses associated with the components that are important in determining the minimum and maximum achievable output voltage. Most important of these are the on resistance of the high- and low-side switch elements, and the series resistance of the output inductor. Taking these losses into account, we can now express the duty cycle of the converter as

$$D = \frac{V_{OUT} + I_{OUT} \times (r_{DS2} + R_L)}{V_{IN} - I_{OUT} \times (r_{DS1} - r_{DS2})}, \tag{6}$$

where r_{DS1} is the on resistance of the high-side switch, S1; r_{DS2} is the on resistance of the low-side switch, S2; and R_L is the output-inductor series resistance. Since the loss terms are added to the numerator and subtracted from the denominator, the duty cycle increases with increasing load current relative to the ideal duty cycle. This has the effect of increasing the available minimum voltage. The worst-case situation for determining the minimum available output voltage occurs when the input voltage is at its maximum specification, the output current is at the minimum load specification, and the switching frequency is at its maximum value. The minimum output voltage is then

$$\begin{aligned} V_{OUT(min)} = {} & t_{on(min)} \times f_{s(max)} \times [V_{IN(max)} - I_{OUT(min)} \\ & \times (r_{DS1} - r_{DS2})] - [I_{OUT(min)} \times (r_{DS2} + R_L)]. \end{aligned} \tag{7}$$

In contrast, the loss terms decrease the available maximum voltage, and the worst-case conditions occur at the minimum input voltage and maximum load current. Since the limiting factor, maximum duty cycle, is specified as a percentage, the switching frequency is not relevant. The maximum available output voltage is given by

$$\begin{aligned} V_{OUT(max)} = {} & D_{max} \times [V_{IN(min)} - I_{OUT(max)} \times (r_{DS1} - r_{DS2})] \\ & -[I_{OUT(max)} \times (r_{DS2} + R_L)]. \end{aligned} \tag{8}$$

Examples

Now we can consider a typical application and calculate the minimum and maximum output voltages. For this example, the input-voltage range is 20 to 28 V, and the load current required is 2 to 3 A. Table 1 shows typical datasheet characteristics of the DC/DC converter.

First we need to calculate the minimum available output voltage by substituting the following parameters into

Table 1. Typical datasheet characteristics of DC/DC converter

PARAMETER	MINIMUM	NOMINAL	MAXIMUM
Reference Voltage (V)	--	1.221	--
Switching Frequency (kHz)	400	500	600
Minimum Controllable ON Time (ns)	--	150	200
Maximum Duty Cycle (%)	87	--	--
FET $r_{DS(on)}$ (V_{IN} < 10 V) (mΩ)	--	150	--
FET $r_{DS(on)}$ (V_{IN} = 10 to 30 V) (mΩ)	--	100	200

Equation 7: $t_{on(min)}$ = 200 ns, $f_{s(max)}$ = 600 kHz, $r_{DS1} = r_{DS2} = r_{DS(on)}$ = 100 mΩ, $V_{IN(max)}$ = 28 V, and $I_{OUT(min)}$ = 2 A. Since the worst-case conditions occur when $t_{on(min)}$ and f_s are at the maximum and the loss terms are at a minimum, we use the appropriate specifications from Table 1. We also need to supply the series resistance of the output inductor. A typical value for the series resistance is 25 mΩ, so Equation 7 can be solved as

$$\begin{aligned} &V_{OUT(min)} \\ &= 200\times 600\times[28-2\times(0.1-0.1)]-[2\times(0.1+0.025)] \\ &= 3.306\text{ V.} \end{aligned}$$

To calculate the maximum output voltage, we need to substitute the following values into Equation 8: $r_{DS1} = r_{DS2} = r_{DS(on)(max)}$ = 200 mW, $V_{IN(min)}$ = 20 V, $I_{OUT(max)}$ = 3 A, D_{max} = 87%, and R_L = 25 mW. With these values, Equation 8 becomes

$$\begin{aligned} &V_{OUT(max)} \\ &= 0.87\times[20-3\times(0.2-0.2)]-[3\times(0.2+0.25)] \\ &= 16.725\text{ V.} \end{aligned}$$

In the example, both switch elements, S1 and S2, are considered active switches. This configuration is the synchronous buck regulator. If both switches are internal to the converter's integrated circuit, they will likely have the same on-resistance characteristics, and $I_{OUT} \times (r_{DS1} - r_{DS2})$ will be zero. In many applications, the low-side switch element is replaced with a passive element, usually a Schottky diode. These devices do not specify an on resistance but instead have a forward conduction voltage; so, for the nonsynchronous buck converter, the minimum and maximum output voltages are

$$\begin{aligned} V_{OUT(min)} &= t_{on(min)}\times f_{s(max)}\times[V_{IN(max)}-(I_{OUT(min)} \\ &\quad \times r_{DS1})-V_d]-(I_{OUT(min)}\times R_L - V_d \end{aligned} \tag{9}$$

and

$$\begin{aligned} V_{OUT(max)} &= D_{max}\times[V_{IN(min)}-(I_{OUT(max)}\times r_{DS1})-V_d] \\ &\quad -(I_{OUT(max)}\times R_L)-V_d. \end{aligned} \tag{10}$$

If the diode forward-voltage drop is 0.4 V, then for the example given, the minimum and maximum output voltages would be 2.838 V and 18.525 V, respectively. The nonsynchronous buck converter is capable of lower or higher output voltages than the synchronous buck converter under the same conditions.

Conclusion

While the ideal buck converter can theoretically provide any output voltage from V_{IN} down to 0 V, practical limitations do exist. The output voltage cannot go below the internal reference voltage, and internal circuit operation may limit the minimum ON time and maximum duty cycle. Additionally, real-world circuits contain losses. These losses can act to extend the duty cycle at higher load currents and may be used to one's advantage when output-voltage extremes exist.

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