High-Performance Analog Products

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Stop-band limitations of the Sallen-Key low-pass filter

By Bonnie C. Baker
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We might expect the gain amplitude of an analog, low-pass anti-aliasing filter to continually decrease past the filter's cutoff frequency. This is a safe assumption for most filter topologies, but not necessarily for a Sallen-Key low-pass filter (Figure 1). The Sallen-Key filter attenuates any input signal in the frequency range above the cutoff frequency to a point, but then the response turns around and starts to increase in gain with frequency.

Figure 1. Second-order, active low-pass analog filters

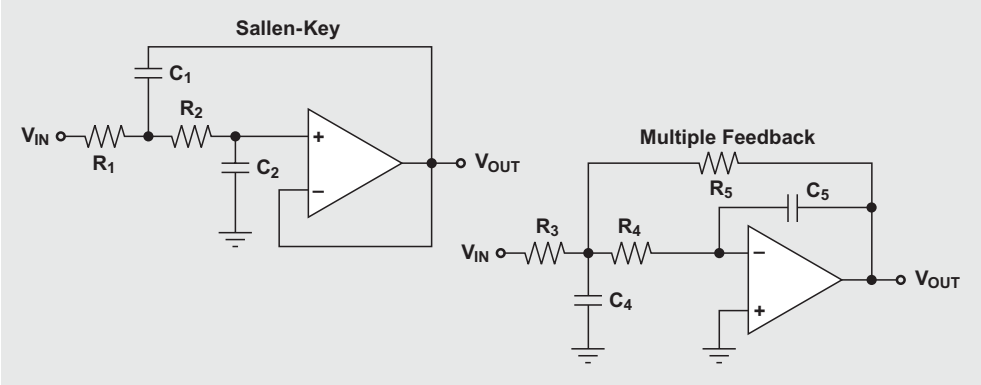


Figure 1 shows circuit diagrams for a second-order, Sallen-Key low-pass filter and a second-order, multiple-feedback (MFB) low-pass filter. In terms of the sign orientation of these two filters, the Sallen-Key filter produces a positive voltage from input to output without changing the sign. An MFB filter changes a positive input voltage into a negative voltage at the output of the filter. This difference provides the system designer added flexibility.

The relationships between the resistors and capacitors in both of these filters establish the filters' corner frequencies and response characteristics. The frequency responses of the two filters in Figure 1 are fundamentally the same. Theoretically, an input signal from DC to the filter's corner frequency passes to the output of the filter (V_{OUT}) without change. These two filters attenuate higher-frequency input signals that are above the cutoff frequency of the filter at a rate of 40 dB per frequency decade. Figure 2 illustrates the ideal transfer function of these two filters in the frequency domain. This figure shows a Butterworth, or maximally flat, response. Chebyshev and Bessel responses will be different.

The filter-response DC gain in Figure 2 is equal to 0 dB. The corner frequency of this low-pass filter occurs at 1 kHz, and the gain magnitude at 1 kHz is equal to –3 dB. Following this corner frequency, the filter response falls off at a rate of –40 dB/decade. Theoretically, the attenuation continues to occur as the frequency increases.

Figure 2. Ideal transfer function of low-pass filter with 1-kHz corner frequency

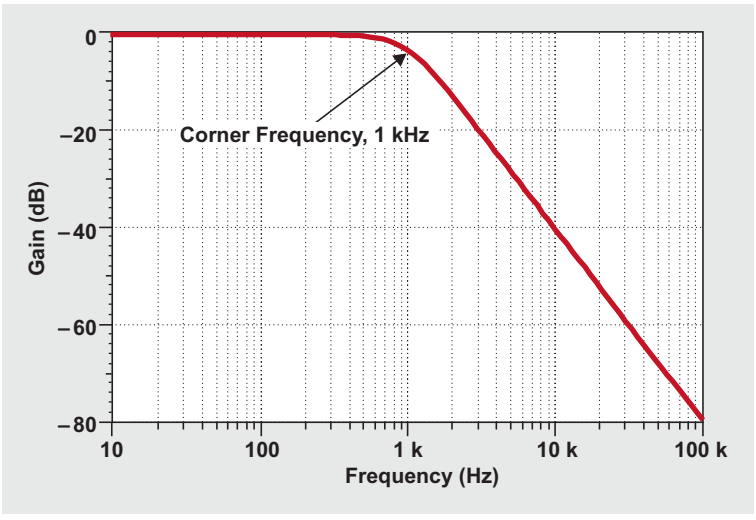
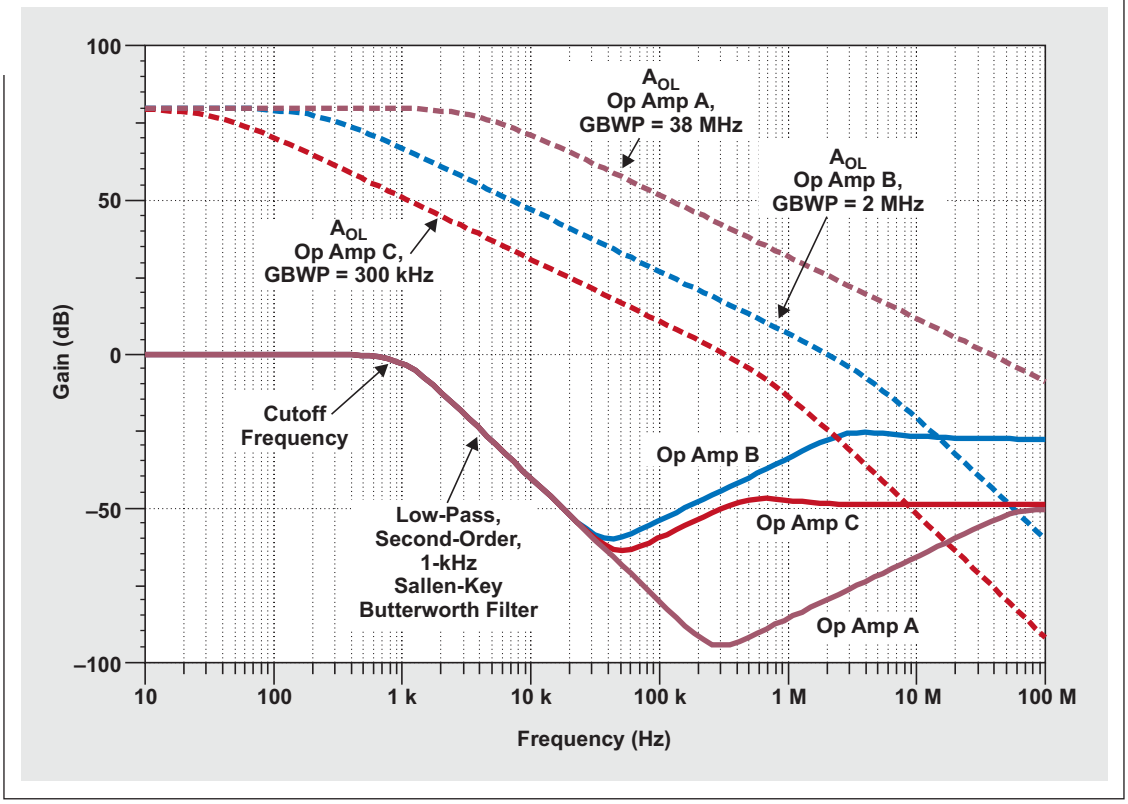


Figure 3. Frequency response of three low-pass filters and amplifier open-loop gain



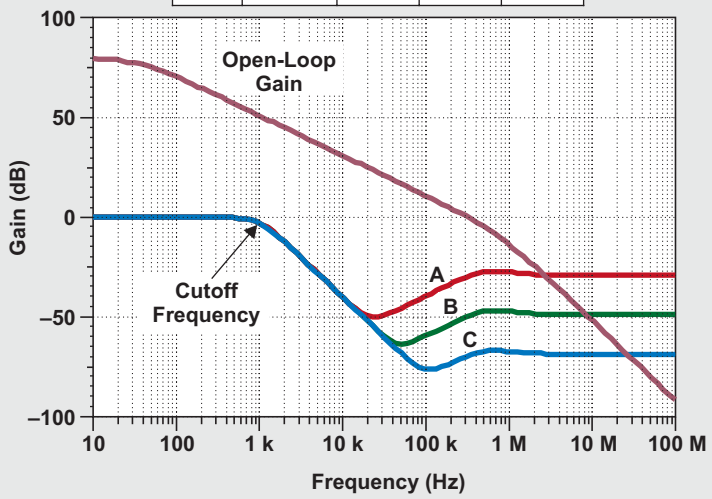
The MFB filter closely matches the theoretical attenuation of the filter in Figure 2. We would expect the Sallen-Key filter to follow suit, but it does not. Figure 3 shows the behavior of three Sallen-Key low-pass filters. The amplifier gain curves start at the top of the diagram at 80 dB, and the filter curves start at a gain of 1 V/V or 0 dB. The top three curves in Figure 3 show the open-loop gain, A_{OL}, of each amplifier as the response crosses 0 dB. The configuration for amplifiers in the top three curves is a simple gain of 10,000 V/V or 80 dB. In the diagram, the gain bandwidth product (GBWP) of these operational amplifiers—A, B, and C—are 38 MHz, 2 MHz, and 300 kHz, respectively.

The three lower curves in this figure show the frequency response of second-order, Sallen-Key low-pass filters for each amplifier. The resistor and capacitor values for the Sallen-Key filter (see Figure 1) are R_1 = 2.74 kΩ, R_2 = 19.6 kΩ, C_1 = 10 nF, and C_2 = 47 nF. These resistors and capacitors, combined with the amplifier, form a Butterworth, maximally flat response. After the cutoff frequency (Figure 3), the responses of all three of the filters show a slope of –40 dB/decade. This is the response we would expect from a second-order low-pass filter; then at some point the filter gain ceases to decrease and starts to increase at a rate of 20 dB/decade. The difference in the frequency response, where the three amplifiers change to a positive slope, depends on the individual amplifier's output impedance as it relates to the resistance values in the circuit. As the open-loop gain of the amplifier decreases, the closed-loop output impedance of the amplifier increases. An op amp's closed-loop output impedance is its open-loop impedance divided by the op amp's gain.

We can reduce the impact of the upward trend in the filter's response by preceding or following the offending active filter with a passive, R-C, second-order low-pass filter. The caveat to preceding or following the second-order active filter with a passive filter is that it may interfere with the phase response of the intended filter, which may cause additional ringing in the time domain. It will also create a stage whose input is not high-impedance or whose output is not low-impedance. Both solutions will possibly add offset and noise to the circuit. Finally, these solutions will add to the overall cost of the application circuit.

Figure 4. Second-order filter response with different R-C values

Second-Order Filter Values				
Filter	R_1 (kΩ)	R_2 (kΩ)	C_1 (nF)	C_2 (nF)
A	0.274	1.96	100	470
B	2.74	19.6	10	47
C	27.4	196	1	4.7



At the frequency where the amplifier's output impedance is greater than the impedance of the resistor (R_1), the feedback looks inductive and the response increases at a rate of 20 dB/decade. The curves in Figure 4, which show the response of a second-order circuit using the OPA234, exaggerate this effect. In Figure 4, the values of the resistances from A to C increase by 10×, and the values of the capacitors from A to C decrease by 10×. With these changes, the general filter response does not change until after the lower three curves pass 0 dB. The corner frequency, where the filter response starts to increase, is dependent upon the relationship between the closed-loop output impedance of the amplifier and the magnitude of R_1.

Eventually each filter's response flattens at the 0-dB crossing frequency of the op amp's open-loop gain. It is no coincidence that the flattening of the filter response occurs at this crossing. As the frequency increases beyond this point, the open-loop gain of the amplifier has no gain.

Needless to say, if a Sallen-Key low-pass filter is used, some characterization is in order. This discussion about analog filters may be discouraging, but we can use alternative filters to solve the problem presented without increasing the filter resistances or adding a passive R-C filter. When an inverting filter is an acceptable alternative, an MFB topology can be used. The MFB configuration does not display this reversal in the gain response at higher frequencies and has the advantage of not taxing the input stage's transistors through their common-mode range.

References

1. Bonnie Baker, *A Baker's Dozen: Real Analog Solutions for Digital Designers* (Amsterdam: Elsevier, 2005), ISBN 0-7506-7819-4.
2. Dave Van Ess. Signals-from-Noise: What Sallen-Key Filter Articles Don't Tell You, Parts I to III. *ConnectivityZONE* [Online]. Available: www.en-genius.net (search Sallen-Key)

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Getting the most battery life from portable systems

By Keith Keller, *Power Analog Field Applications,*
and M.A. Banak, *Electronics Design Consultant*

Introduction

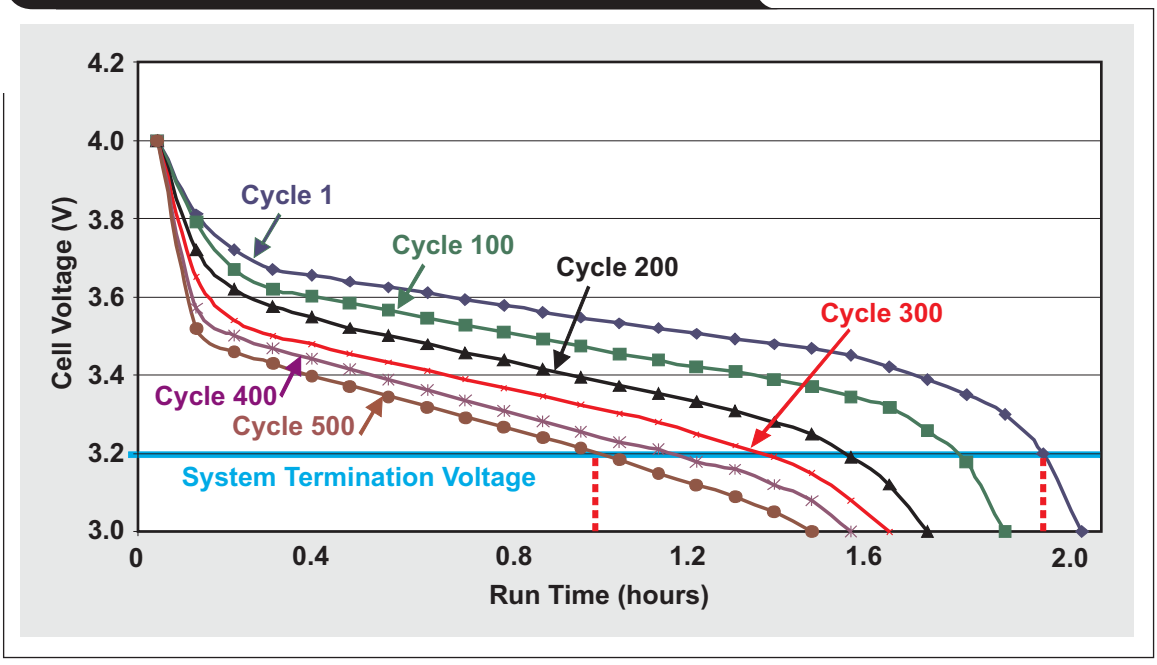
Run time of portable systems is increasingly important as devices become more feature-rich with power-hungry processors, transmitters, receivers, and media playback, to name just a few. Using a battery "fuel gauge" is the natural step to increasing run time of the system. Unfortunately, previous-generation gauges are up to 15% inaccurate, depending on usage profiles and cell aging. In this article, we describe a third-generation technology from Texas Instruments (TI) called *Impedance Track*™, which can provide up to 99% accuracy for the entire lifetime of the battery pack and extend its life.

Common problems in Li-ion battery applications

The most important considerations in the design of a battery subsystem are its safe use and the reliability of the available power; but even the safest design is of little value if the battery life is unpredictable. No one expects a charged battery to last forever, and fault mechanisms are an established fact of life. Thus, the battery-system designer must devise a means of telling the user how much charge is left in the battery and of protecting the cells from various fault conditions. Much of this attention centers around the management of the battery near the point where it is considered fully discharged.

Customers do not like to have their systems abruptly halt or, even worse, halt and lose data. With previous-generation battery-monitoring technology and an "aggressive" system implementation that did not take into account real-life battery behavior, unpredictable system shutdown was a real possibility. Inaccuracies in true capacity would creep in over time. We could only make an educated guess as to how the individual cells would age over time (develop an increased internal impedance of the electrolyte anode/cathode material) from normal charge/discharge cycling. Figure 1 shows that with normal cell aging, 500 charge/discharge cycles can increase cell impedance such that the run time is half that of a new cell. (A cycle is defined as a transfer of greater than 70% of the total energy out of and into the cell.)

Figure 1. Impedance change with charge/discharge aging



Li-ion cells have certain known characteristics. Impedance is extremely dependent on temperature during discharge. High temperatures and a minute overvoltage on a cell cause a large degradation to cell lifetime. Figure 2 shows that charging a cell even 50 mV higher than its specified maximum will decrease cell life by up to 50%.[1] Figure 3 shows that cells discharged more than 80% will see a fivefold increase in DC impedance (from approximately 300 mΩ to greater than 1.5 Ω) from room temperature to 0ºC.[1]

Over an extended period of time, it is possible for cells in series to become imbalanced. The usable life of the pack can be reduced if one cell in the stack reaches the cell undervoltage (CUV) sooner than the others. At that point the cell pack needs to report zero capacity and shut down. An analogy is a chain, which is only as strong as its weakest link. In extreme circumstances, one of the low-cell-voltage protectors can trip and immediately halt all further discharge. The system shuts down without warning, yet previous-generation fuel gauges would report more than adequate time remaining.

Indeed, the mistracking of protection devices with fuel-gauge registers has been a perennial problem. One strategy for coping with this has been to pad the fuel-gauge report with considerable margin. This allows the system designer to guarantee that zero capacity is reported at a cell level that is well above the low-voltage shutdown threshold. This will prevent an unexpected shutdown while the system is in service; but typically the 15% margin needed to guarantee reliability is a high price to pay, and this margin may need to be further increased to allow for the uncertainties of cell aging, temperature effects, and user discharge profiles.

Figure 2. Charge voltage affects battery service life

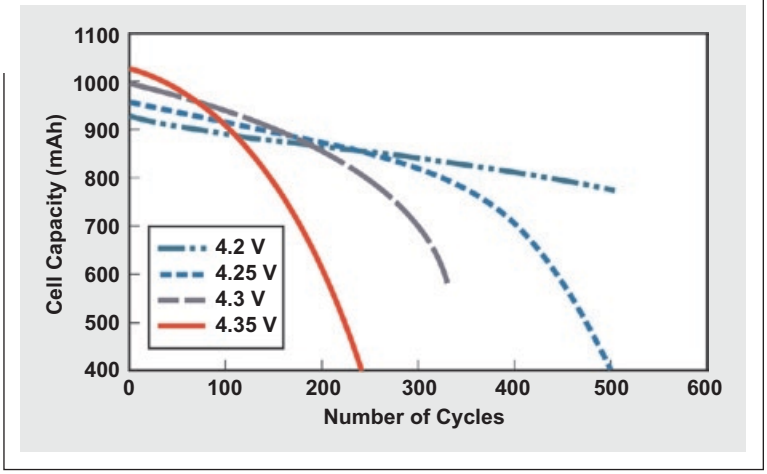
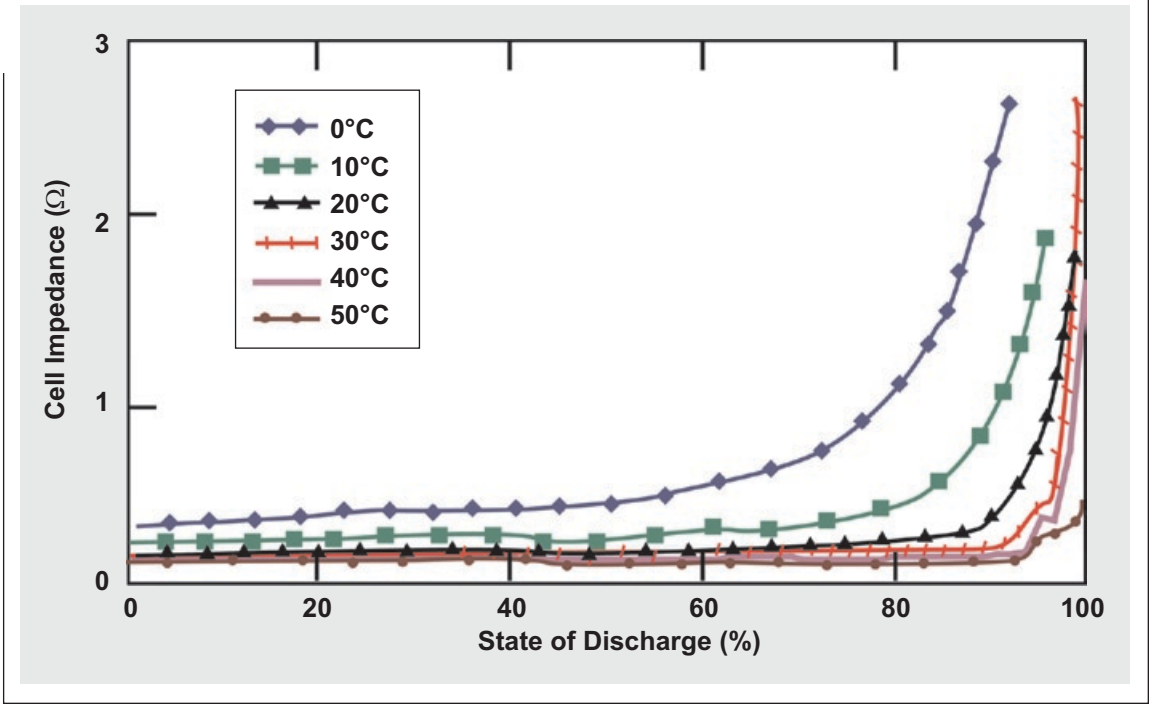


Figure 3. Li-ion impedance dependence on temperature and depth of discharge



A complete model of battery capacity under all conditions

The state of charge for a Li-ion cell can be fully predicted if the following parameters are included in a comprehensive model:

- The cell's total chemical capacity (Q_{max}). This is initially specified as the datasheet capacity (e.g., 2400 mAh for an 18650 cylindrical cell), but the fuel gauge automatically updates it after the first charge/discharge cycle of the battery.
- The amount of electric charge that has passed into or out of the cell, which is measured/acquired by the coulomb-counting process.
- The present load current in the system (average and peak).
- The cell's internal resistance while delivering current. This varies with temperature changes, effects of cell aging, and the cell's state of charge.
- The cell's relaxed open-circuit voltage (OCV). This is measured at light load (<C/20) with a change in battery voltage of less than a few microvolts over a sampling period. When fully charged, the cell requires a shorter rest period than when it is deeply depleted.

A precise capacity estimate can be calculated by measuring the cell's open-circuit (relaxed) voltage, monitoring the voltage profile of the cell under load (finding the cell's impedance), and integrating current in and out of the battery. All Li-ion batteries with the same chemistry and anode/cathode material have extremely similar relaxed OCV profiles. This voltage measurement directly correlates to the cell's state of charge and is amazingly independent of the cell manufacturer. For example, with $LiMnO_2$ cells from either Sony or Panasonic, an OCV measurement of 3.9 V will equate to 90% full charge. Keep in mind, though, that $LiMnO_2$ cells do not have the same OCV profile as $LiCoO_2$ or $LiFePO_4$ cells.

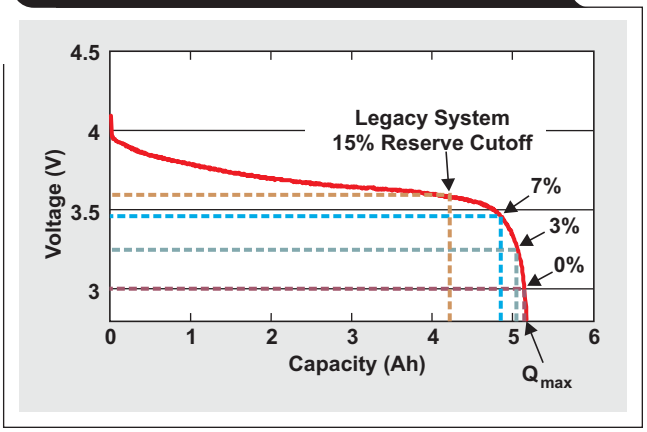
TI's *Impedance Track*™ solution

Over the last several years, advanced battery-management solutions from TI have evolved from a two-IC chipset to the currently available single-IC solutions like the bq20z75 and bq20z95. (For single-cell "1s" applications, please see the bq27500-v100 and bq27540.) These Smart Battery Specification (SBS) 1.1-compliant ICs are protection-enabled and implement *Impedance Track* fuel-gauging technology to continuously analyze the battery impedance and maximum capacity (Q_{max}), resulting in superior fuel-gauging accuracy.

Improved accuracy means greater available capacity

Fuel gauging is used to provide a graceful system shutdown as the battery approaches its end of discharge. The remaining charge is estimated and used to trigger shutdown when the battery is getting close to empty. As mentioned earlier, most designs using legacy devices must allow for an inaccuracy margin of up to 15% because errors creep in when a full discharge doesn't occur. With the *Impedance Track* system, which can provide up to 99% accuracy, we can program the terminate voltage (V_{Term}) at which zero capacity is defined. If we have true 99% accuracy, then the 14% capacity we gain back can be used to significantly increase the run time of the system (see Figure 4).

Figure 4. Extended capacity available with *Impedance Track* technology



For example, at 7% capacity, the operating system could warn the user that a shutdown is imminent; and, at 3%, a shutdown could be forced, including saving the data. That last 1 to 2% of capacity could be saved for servicing a few extra reboots, where the user is reminded that the battery is empty and needs to be recharged. The *Impedance Track* system also automatically balances the cells during charge taper, thus squeezing additional capacity from the cell stack and extending the life of the pack overall.

Elimination of charger banks on the production floor

Legacy fuel gauges require Q_{max} calibration with a four-step charge/discharge cycle:

1. Assemble pack; calibrate voltage, current, and temperature; run final electrical check.
2. Discharge pack to empty.
3. Charge pack to full capacity. The fuel gauge has now learned Q_{max}.
4. Drain off cells to approximately 40% capacity for storage.

The entire process can take nearly an entire production shift, and the production-grade chargers need maintenance. A typical factory will have dozens of such chargers on the floor, while production technicians spend dizzying hours keeping them in repair.

With *Impedance Track* technology, we need only characterize a typical battery pack from the targeted cell manufacturer and then save those characterization parameters for download to all cell packs. Production packs are assembled with the cells at the charge level set by the manufacturer, and a simple, inexpensive programming fixture is used to program the onboard flash memory with the design parameters.

With this method, there is no lost production time, no lost factory space for all those chargers, and no need for special development of factory-grade chargers.

Smart charger/smart battery interface

Conformance to the SBS allows smart chargers to communicate directly with the battery pack. When paired with an SBS-compliant battery charger, an *Impedance Track* fuel gauge like the bq20z75 can request optimal charge currents to properly top off cell capacity via the SMBus interface. Also, status flags in the charger are visible to the host processor, which will broadcast timely warnings to the charger to stop charging. In short, the entire business of optimizing charger design is resolved by using this SBS-compliant battery monitor/fuel gauge.

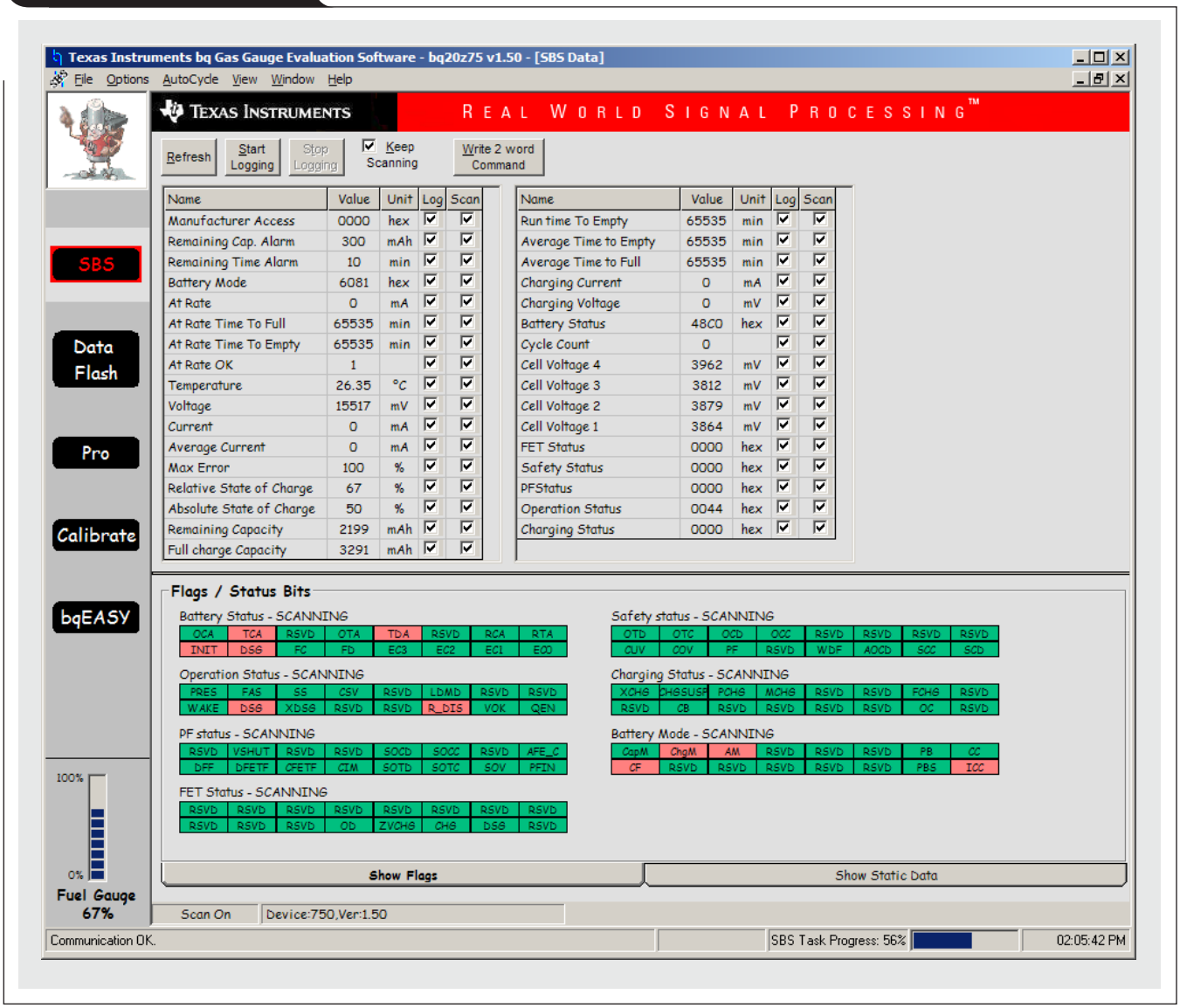
During field operation, all standard SBS commands can be requested of the battery pack and fuel gauge, such as AtRateTimeToEmpty (0x06), Temperature (0x08), Voltage (0x09), Current (0x0a), RelativeStateOfCharge (0x0d), RemainingCapacity (0x0f), and CycleCount (0x17), to name just a few (see Figure 5). Support for many of these commands already exists within operating systems such as WinCE. Please note that SMBus communication is only point-to-point. Multiple batteries are not allowed to communicate on the same lines. There are several I²C/SMBus expanders to help us with multiple-pack systems.

Up-front design effort saves time and lowers costs

The advantages of using *Impedance Track* technology are realized from the engineering effort that is invested up front. The ICs come preloaded with defaults that require refinement for a specific target application. With proper configuration, an optimal design can be made to run trouble-free in the field.

It is important to note that the comprehensive nature of the *Impedance Track* system actually makes for a rigorous checklist of design considerations for the engineer. Taking the time to work through each configuration register makes battery-pack design issues become evident. It is

Figure 5. SBS data screen



common for designers to discover overlooked areas of concern well before product release.

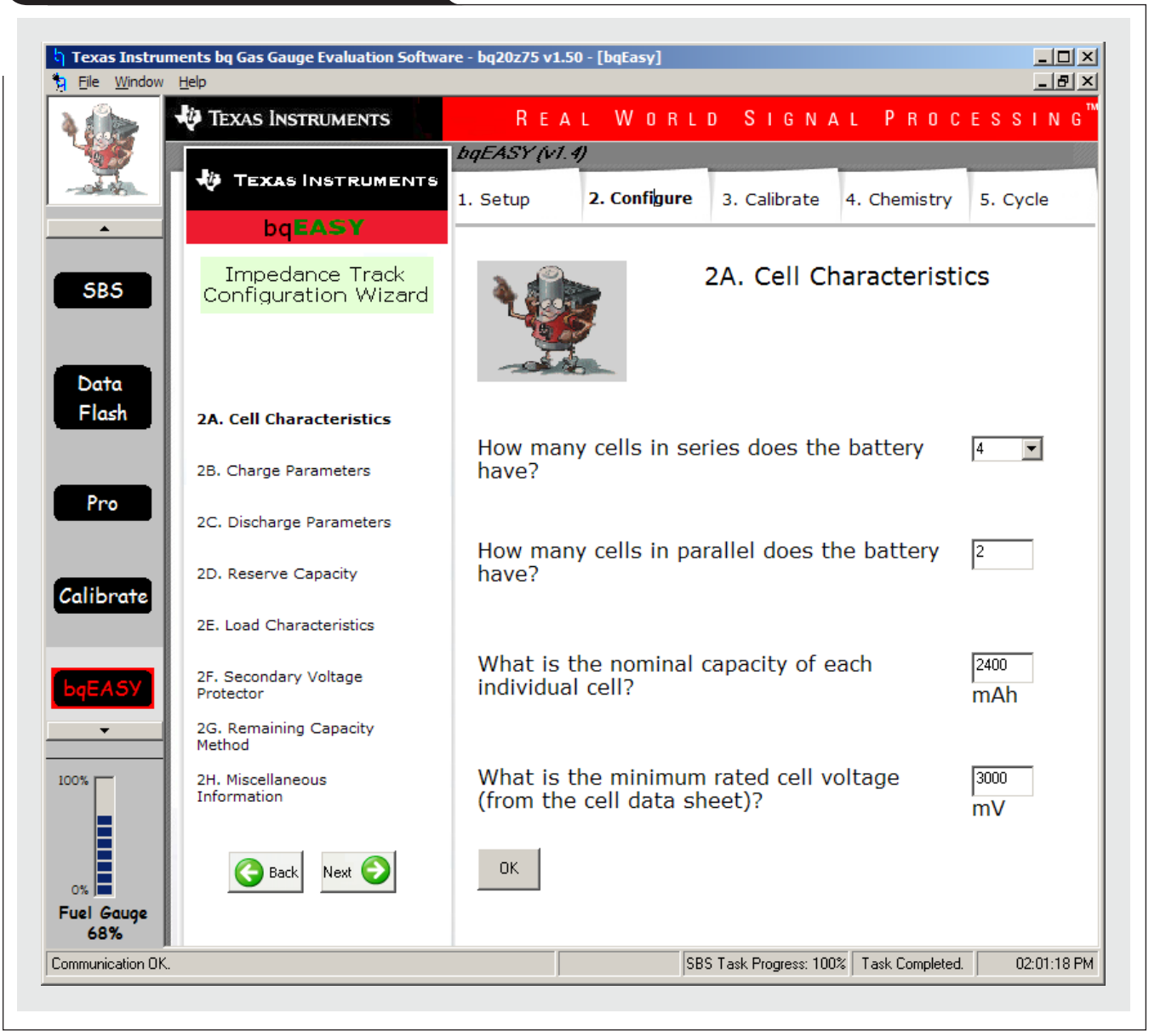
Configuration of the "golden-unit" battery pack is accomplished with a device evaluation module (EVM), an EV2300 USB interface board, and device-specific profiles in the support software, all available from TI. The software has a graphical user interface (GUI) that allows the entry of configuration data for the battery-pack design. The software also includes a system-setup wizard called bqEASY™, which allows the designer to answer questions about the system and then configures the dataflash constants automatically.

For example, the *Impedance Track* analog front end (AFE) will service a complete menu of alarm options, covering overcurrent during charge and discharge. These alarm threshold values are entered into the software's GUI menus, from which they are downloaded into the EVM board. In each case, these limits must be based on the expected system parameters. The specifications in the datasheet for the particular cell size employed must also be considered.

Likewise, the cell manufacturer's requirements for charge/discharge current levels and battery capacity must be entered into the bqEASY wizard or the GUI menus (see Figure 6). Other configuration features include units of capacity and SMBus communication options.

It is rare that the defaults in the IC configuration are adequate for a particular design. Along with the bqEASY wizard software, TI offers a set of quick-start instructions to get past the defaults for the most common applications.

Figure 6. bqEASY configuration wizard



These instructions also serve as an excellent introduction to the *Impedance Track* methodology. For in-depth design, the datasheets and related technical documents have comprehensive information on such parameters as register configuration, its default values, and its practical limits.

It is well-known that battery testing, by its very nature, is a time-consuming business. In the past, it has often taken many days to track down the status of a critical parameter that was hindering optimal performance. Fortunately, TI's *Impedance Track* EVM software has extensive analysis tools that display battery conditions in real time, including state of charge, voltage, current level, and a host of other parameters and flags. The software also performs real-time data logging to enable pinpoint debugging of overnight tests.

The most critical step after downloading the configuration parameters is setting up the golden-unit image file. After running bqEASY or setting the dataflash values for a particular design, we need only a series of charge/discharge cycles to calibrate the *Impedance Track* algorithm. The steps described in TI's documentation may take a couple of days to complete; however, the big time and cost savings come from never again having to perform capacity charge/discharge-cycle calibration on battery packs during production or in the field.

Once the choice of design parameters is deemed good on a single golden-unit prototype, its setup image is uploaded to a special configuration file, from which data is loaded into several more battery packs for further testing. After qualification, the golden-unit design parameters are simply downloaded into assembled battery packs in production, with no further fuel-gauge capacity calibration necessary.

As long as a particular manufacturer's part number for the Li-ion cell is used in the factory, the programming parameters remain the same. There is one additional consideration, however—battery technology is always improving. The original 1800-mAh 18650 cell today typically yields 2400 mAh or as high as 3000 mAh in some cases. TI devices can easily accommodate updated values for cell capacity that may come with technological improvements.

Conclusion

Impedance Track technology offers three main benefits:

- Dramatically improved fuel-gauging accuracy of up to 99% over the life of the battery pack.
- Ease of manufacture, since there is no need to calibrate capacity for every battery pack in production.
- A standard battery communication interface (SMBus) for interoperability and immediate use with modern applications and smart chargers.

An additional benefit is the knowledge of powerful battery-system design found in the documentation that is used as part of the proper design process for this system.

A complete hardware schematic for a typical system can be found at www-s.ti.com/sc/techlit/sluu277. Designers will benefit greatly from the extra battery capacity and ease of manufacture afforded by *Impedance Track* technology, which figures to become a *de facto* standard for battery-pack design in the near future.

Reference

1. Soo Seok Choi and Hong S. Lim, "Factors that affect cycle-life and possible degradation mechanisms of a Li-ion cell based on $LiCoO_2$," *Journal of Power Sources*, Vol. 111, Issue 1 (Sept. 18, 2002), pp. 130–136.

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Smart Battery System Implementers Forum (SBS-IF), **www.sbs-forum.org**

System Management Bus (SMBus), **www.smbus.org**

System Management Interface Forum (SMIF), **www.smiforum.org**

Compensating and measuring the control loop of a high-power LED driver

By Jeff Falin
Senior Applications Engineer

A mathematical model is always helpful in determining the optimal compensation components for a particular design. However, compensating the loop of a WLED current-regulating boost converter is a bit different than compensating the same converter configured to regulate voltage. Measuring the control loop with traditional methods is cumbersome because of low impedance at the feedback (FB) pin and the lack of a top-side FB resistor. In Reference 1, Ray Ridley has presented a simplified, small-signal control-loop model for a boost converter with current-mode control. The following explains how to modify Ridley's model so that it fits a WLED current-regulating boost converter; it also explains how to measure the boost converter's control loop.

Loop components

As shown in Figure 1, any adjustable DC/DC converter can be modified to provide a higher or lower regulated output voltage from an input voltage. In this configuration, if we assume R_{OUT} is a purely resistive load, then $V_{OUT} = I_{OUT} \times R_{OUT}$. When used to power LEDs, a DC/DC converter actually controls the current through the LEDs by regulating the voltage across the low-side FB resistor as shown in Figure 2. Because the load itself (the LEDs) replaces the upper FB resistor, the traditional small-signal control-loop equations no longer apply. The DC load resistance is

$$R_{EQ} = V_{OUT}/I_{LED}, \quad (1)$$

with

$$V_{OUT} = n \times V_{FWD} + V_{FB}. \quad (2)$$

V_{FWD}, taken either from the diodes' datasheet or from measurements, is the forward voltage at I_{LED}; and n is the number of LEDs in the string.

Figure 1. Adjustable DC/DC converter used to regulate voltage

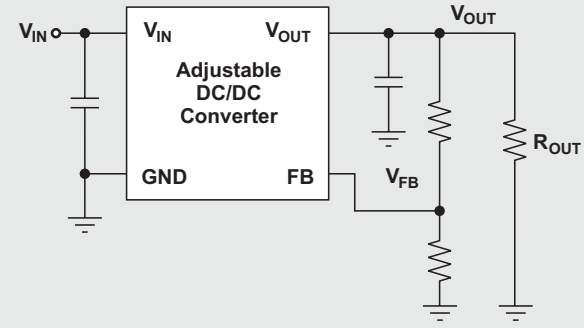


Figure 2. Adjustable DC/DC converter used to regulate current through LEDs

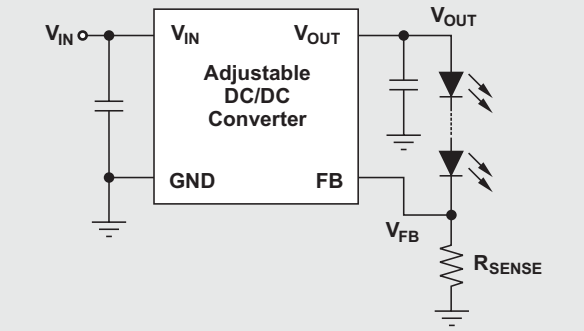
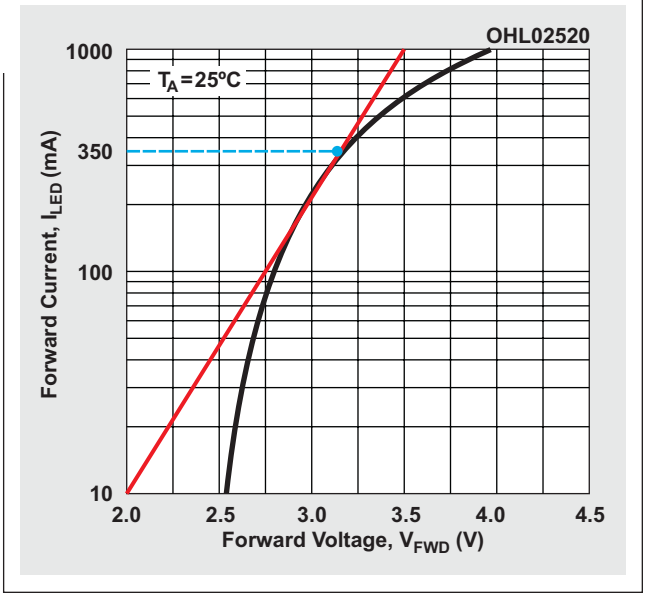


Figure 3. I-V curve of OSRAM LW W5SM



However, from a small-signal standpoint, the load resistance consists of R_{EQ} as well as the dynamic resistances of the LEDs, r_D, at the I_{LED}. While some LED manufacturers provide typical values of r_D at various current levels, the best way to determine r_D is to extract it from the typical LED I-V curve, which all manufacturers provide. Figure 3 shows an example I-V curve of an OSRAM LW W5SM high-power LED. Being a dynamic (or small-signal) quantity, r_D is defined as the change in voltage divided by the change in current, or $r_D = \Delta V_{FWD}/\Delta I_{LED}$. To extract r_D from Figure 3, we simply drive a straight tangent line from the V_{FWD} and I_{LED} for the application and compute the slope. For example, using the dotted tangent line in Figure 3, we get r_D = (3.5 – 2.0 V)/(1.000 – 0.010 A) = 1.51 Ω at I_{LED} = 350 mA.

Small-signal model

As an example of a small-signal model, the TPS61165 peak-current-mode converter driving three series OSRAM LW W5SM parts will be used. Figure 4a shows an equivalent small-signal model of a current-regulating boost converter, while Figure 4b shows an even more simplified model.

Equation 3 shows a frequency-based (s-domain) model for computing DC gain in both the current-regulating and the voltage-regulating boost converters:

$$G_P(s) = K_R \times \frac{(1-D)}{R_i} \times \frac{\left(1+\frac{s}{\omega_z}\right)\times\left(1-\frac{s}{\omega_{RHP}}\right)}{\left(1+\frac{s}{\omega_p}\right)\times\left(1+\frac{s}{Q_p\omega_n}+\frac{s^2}{\omega_n^2}\right)}, \quad (3)$$

where the common variables are

$$\omega_z = \frac{1}{ESR \times C_{OUT}},$$

$$Q_p = \frac{1}{\pi\left[\left(1+\frac{S_e}{S_n}\right)(1-D)-0.5\right]},$$

$$\omega_n = \pi \times f_{SW},$$

and

$$\omega_{RHP} = \frac{R_{EQ}}{(1-D)^2 \times L}.$$

Figure 4. Small-signal model of current-regulating boost converter

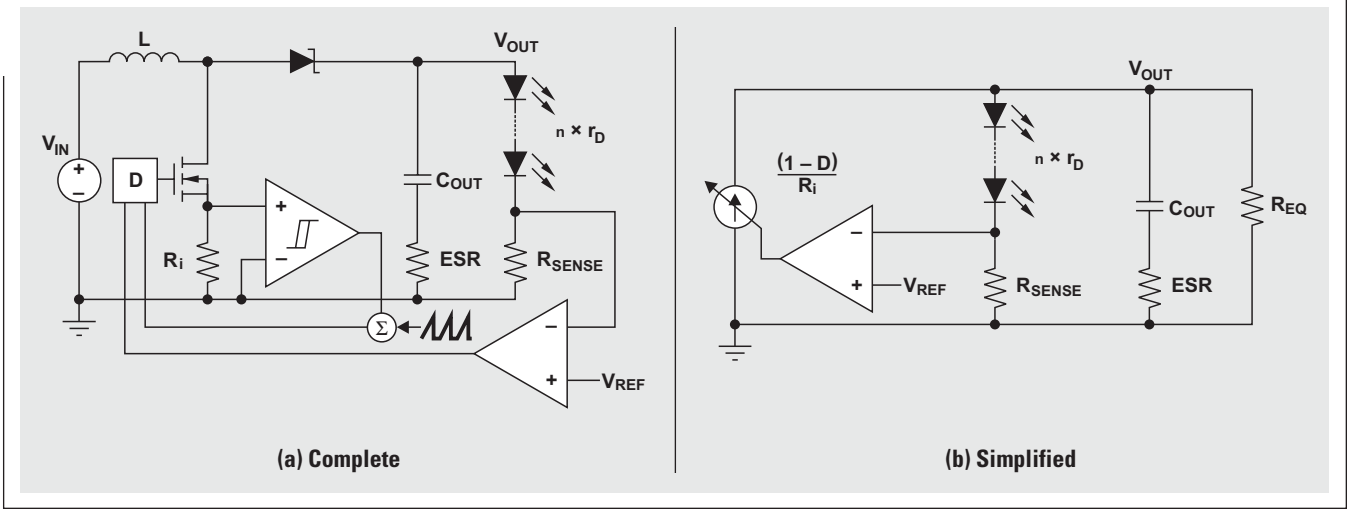


Table 1. Differences in Equation 3 terms for two converter models

TERM	EVALUATION OF CURRENT-REGULATING BOOST CONVERTER	EVALUATION OF VOLTAGE-REGULATING BOOST CONVERTER
K_R	$\frac{R_{EQ}}{1+\frac{R_{EQ}+n\times r_D}{R_{SENSE}}}$	$\frac{R_{OUT}}{2}$
ω_p	$\frac{1+\frac{n\times r_D+R_{SENSE}}{R_{EQ}}}{(n\times r_D+R_{SENSE}+ESR)\times C_{OUT}}$	$\frac{2}{(R_{OUT}+ESR)\times C_{OUT}}$

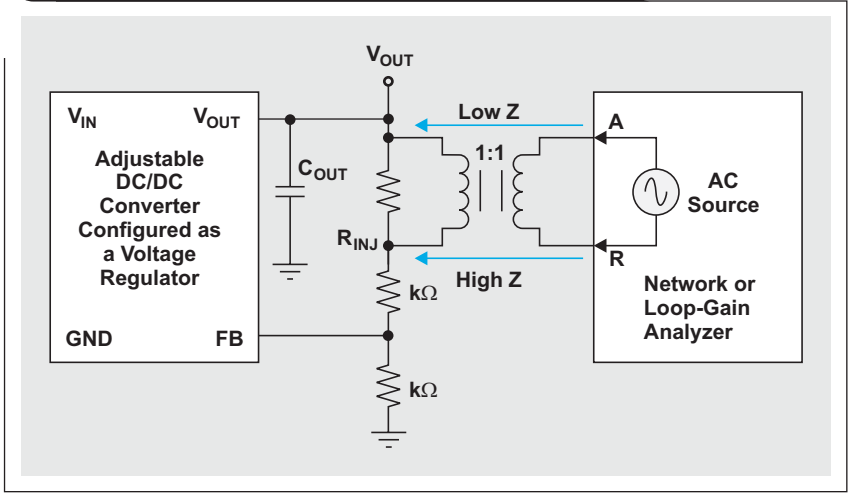
The duty cycle, D, and the modified values for V_{OUT} and R_{EQ} are computed the same way for both circuits. S_n and S_e are the natural inductor and compensation slopes, respectively, for the boost converter; and f_{SW} is the switching frequency. The only real differences between the small-signal model for the voltage-regulating boost converter and the model for a current-regulating boost converter is the resistance K_R—which multiplies by the transconductance term, $(1 – D)/R_i$—and the dominant pole, ω_p. These differences are summarized in Table 1. See Reference 1 for more information.

Since the value of R_{SENSE} is typically much lower than that of R_{OUT} in a converter configured to regulate voltage, the gain for a current-regulating converter, where $R_{OUT} = R_{EQ}$, will almost always be lower than the gain for a voltage-regulating converter.

Measuring the loop

To measure the control loop gain and phase of a voltage-regulating converter, a network or dedicated loop-gain/phase analyzer typically uses a 1:1 transformer to inject a small signal into the loop via a small resistance (R_{INJ}). The analyzer then measures and compares, over frequency, the injected signal at point A to the returned signal at point R and reports the ratio in terms of amplitude difference (gain) and time delay (phase). This resistance can be inserted anywhere in the loop as long as point A has relatively much lower impedance than point R; otherwise, the injected signal will be too large and disturb the converter's operating point. As shown in Figure 5, the high-impedance node where the FB resistors sense the output voltage at the output capacitor (low-impedance node) is the typical place for such a resistor.

Figure 5. Control-loop measurement for voltage-regulating converter



In a current-regulating configuration, with the load itself being the upper FB resistor, the injection resistor cannot be inserted in series with the LEDs. The converter's operating point must first be changed so the resistor can be inserted between the FB pin and the sense resistor as shown in Figure 6. In some cases, a non-inverting, unity-gain buffer amplifier may be necessary to lower the impedance at the injection point and reduce measurement noise.

With the measurement setup in Figure 6 but without the amplifier, and with R_{INJ} = 51.1 Ω, a Venable loop analyzer was used to measure the loop. The model of a current-regulating converter was constructed in Mathcad® using the datasheet design parameters of the TPS61170, which has the same core as the TPS61165. With V_{IN} = 5 V and I_{LED} set to 350 mA, the model gives the predicted loop response for the TPS61165EVM as shown in Figure 7, which provides an easy comparison with measured data.

We can easily explain the differences between the measured and simulated gain by observing variations in the WLED dynamic resistance and using the typical LED I-V curve as well as chip-to-chip variations in the IC's amplifier gain.

Figure 6. Control-loop measurement for current-regulating converter

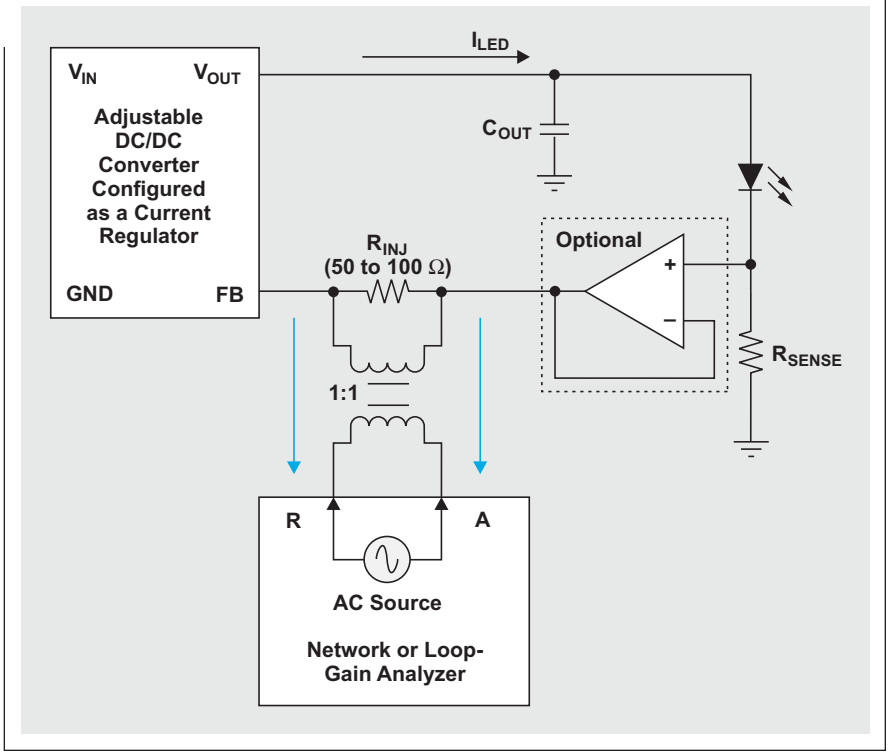
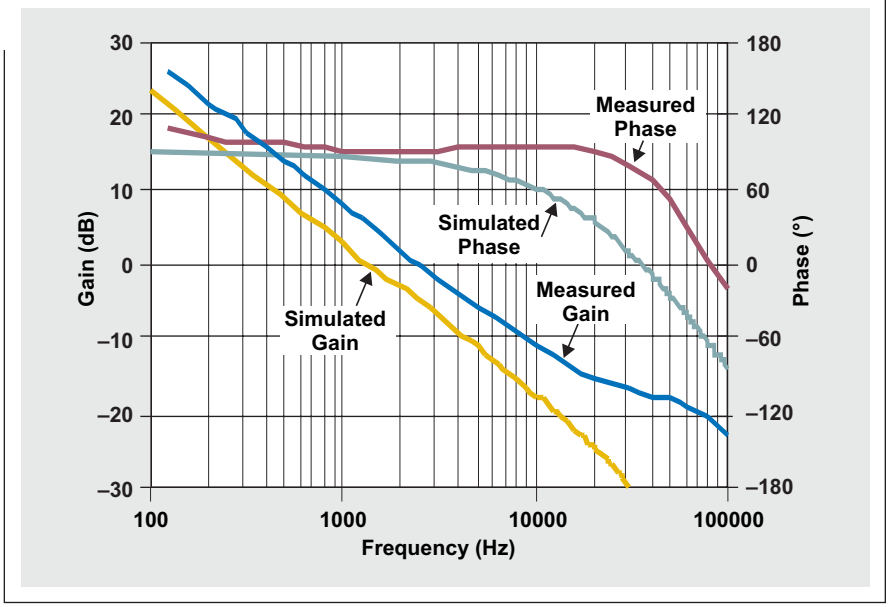


Figure 7. Measured and simulated loop gain and phase at V_{IN} = 5 V and I_{LED} = 350 mA



Conclusion

While not exact, the mathematical model gives the designer a good starting point for designing the compensation of a WLED current-regulating boost converter. In addition, the designer can measure the control loop with one of the alternate methods.

Reference

1. Ray Ridley. (2006). Designer's Series, Part V: Current-Mode Control Modeling. *Switching Power Magazine* [Online]. Available: http://www.switchingpowermagazine.com/downloads/5%20Current%20Mode%20Control%20Modeling.pdf

Related Web sites

power.ti.com
www.ti.com/sc/device/TPS61165
www.ti.com/sc/device/TPS61170

Designing DC/DC converters based on SEPIC topology

By Jeff Falin
Senior Applications Engineer

Introduction

The single-ended primary-inductance converter (SEPIC) is a DC/DC-converter topology that provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage. This type of conversion is handy when the designer uses voltages (e.g., 12 V) from an unregulated input power supply such as a low-cost wall wart. Unfortunately, the SEPIC topology is difficult to understand and requires two inductors, making the power-supply footprint quite large. Recently, several inductor manufacturers began selling off-the-shelf coupled inductors in a single package at a cost only slightly higher than that of the comparable single inductor. The coupled inductor not only provides a smaller footprint but also, to get the same inductor ripple current, requires only half the inductance required for a SEPIC with two separate inductors. This article explains how to design a SEPIC converter with a coupled inductor.

Basic operation

Figure 1 shows a simple circuit diagram of a SEPIC converter, consisting of an input capacitor, C_{IN}; an output capacitor, C_{OUT}; coupled inductors L1a and L1b; an AC coupling capacitor, C_P; a power FET, Q1; and a diode, D1. Figure 2 shows the SEPIC operating in continuous conduction mode (CCM). Q1 is on in the top circuit and off in the bottom circuit.

To understand the voltages at the various circuit nodes, it is important to analyze the circuit at DC when Q1 is off and not switching. During steady-state CCM, pulse-width-modulation (PWM) operation, and neglecting ripple voltage,

Figure 1. Simple circuit diagram of SEPIC converter

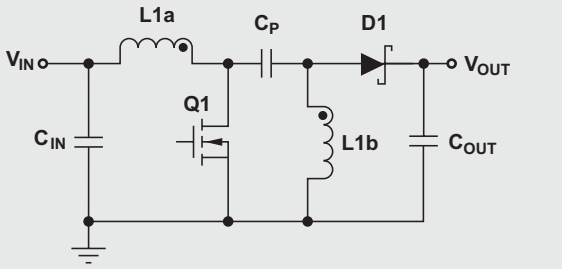
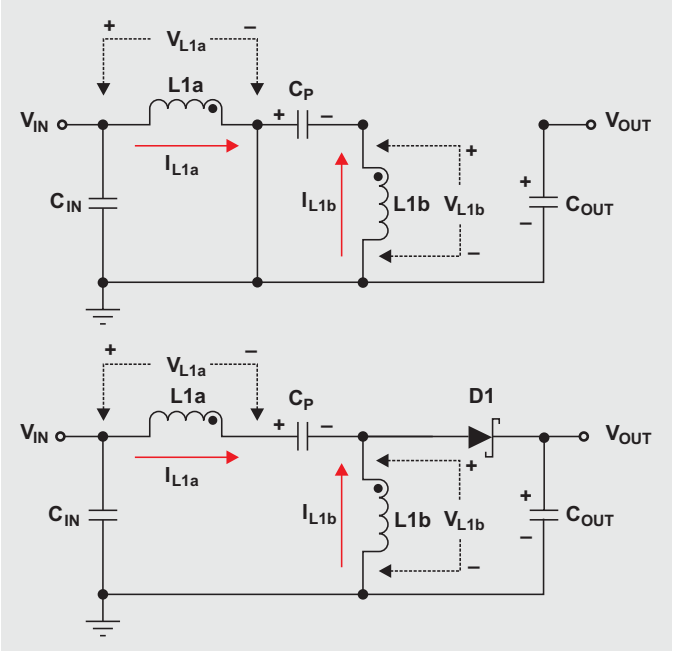


Figure 2. SEPIC during CCM operation when Q1 is on (top) and off (bottom)

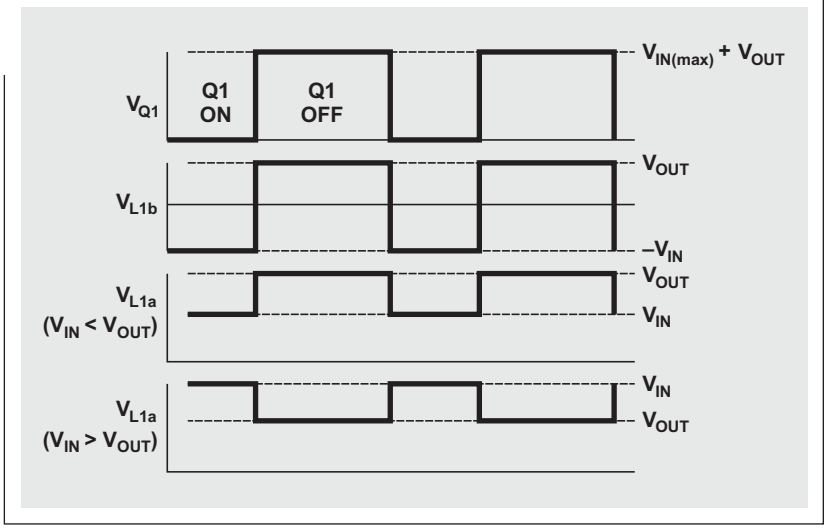


capacitor C_P is charged to the input voltage, V_{IN}. Knowing this, we can easily determine the voltages as shown in Figure 3.

When Q1 is off, the voltage across L1b must be V_{OUT}. Since C_{IN} is charged to V_{IN}, the voltage across Q1 when Q1 is off is V_{IN} + V_{OUT}, so the voltage across L1a is V_{OUT}. When Q1 is on, capacitor C_P, charged to V_{IN}, is connected in parallel with L1b, so the voltage across L1b is $-V_{IN}$.

The currents flowing through various circuit components are shown in Figure 4. When Q1 is on, energy is being stored in L1a from the input and in L1b from C_P. When Q1 turns off, L1a's current continues to flow through C_P and D1, and into C_{OUT} and the load. Both C_{OUT} and C_P get recharged so that they can provide the load current and charge L1b, respectively, when Q1 turns back on.

Figure 3. SEPIC component voltages during CCM



Duty cycle

Assuming 100% efficiency, the duty cycle, D, for a SEPIC converter operating in CCM is given by

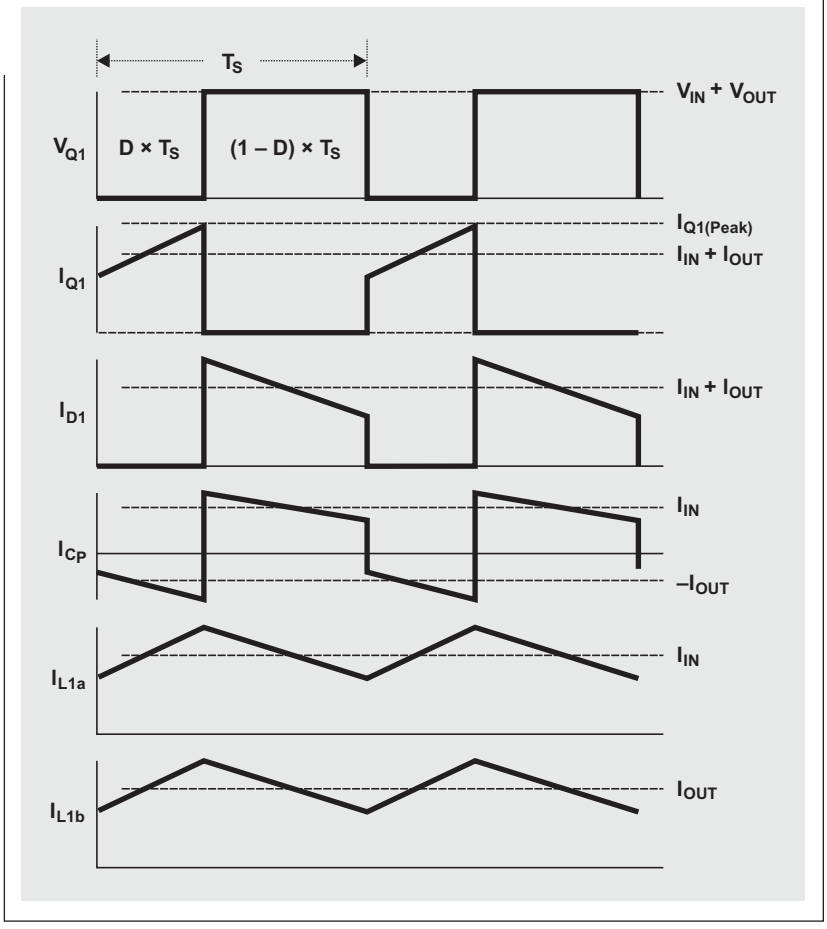
$$D = \frac{V_{OUT} + V_{FWD}}{V_{IN} + V_{OUT} + V_{FWD}}, \quad (1)$$

where V_{FWD} is the forward voltage drop of the Schottky diode. This can be rewritten as

$$\frac{D}{1-D} = \frac{V_{OUT} + V_{FWD}}{V_{IN}} = \frac{I_{IN}}{I_{OUT}}. \quad (2)$$

D(max) occurs at $V_{IN(min)}$, and D(min) occurs at $V_{IN(max)}$.

Figure 4. SEPIC component currents during CCM



Selecting passive components

One of the first steps in designing any PWM switching regulator is to decide how much inductor ripple current, ΔI_L, to allow. Too much increases EMI, while too little may result in unstable PWM operation. A rule of thumb is to use 20 to 40% of the input current, as computed with the power-balance equation,

$$\Delta I_L = 30\% \times \frac{I_{IN}}{\eta} = 30\% \times I_{IN}'. \quad (3)$$

In this equation, I_{IN} from Equation 2 is divided by the estimated worst-case efficiency, η, at $V_{IN(min)}$ and $I_{OUT(max)}$ for a more accurate estimate of the input current, I_{IN}'.

In an ideal, tightly coupled inductor, with each inductor having the same number of windings on a single core, the mutual inductance forces the ripple current to be split equally between the two coupled inductors. In a real coupled inductor, the inductors do

not have equal inductance and the ripple currents will not be exactly equal. Regardless, for a desired ripple-current value, the inductance required in a coupled inductor is estimated to be half of what would be needed if there were two separate inductors, as shown in Equation 4:

$$L1a(min) = L1b(min) = \frac{1}{2} \times \frac{V_{IN(min)} \times D(max)}{\Delta I_L \times f_{SW(min)}} \quad (4)$$

To account for load transients, the coupled inductor's saturation current rating needs to be at least 20% higher than the steady-state peak current in the high-side inductor, as computed in Equation 5:

$$I_{L1a(Peak)} = I_{IN}' + \frac{\Delta I_L}{2} = I_{IN}' \left(1 + \frac{30\%}{2}\right) \quad (5)$$

Note that $I_{L1b(Peak)} = I_{OUT} + \Delta I_L/2$, which is less than $I_{L1a(Peak)}$.

Figure 5 breaks down the capacitor ripple voltage as related to the output-capacitor current. When Q1 is on, the output capacitor must provide the load current. Therefore, the output capacitor must have at least enough capacitance, but not too much ESR, to meet the application's requirement for output voltage ripple, ΔV_{RPL}:

$$\Delta V_{RPL} \le \frac{I_{OUT} \times D(max)}{C_{OUT} \times f_{SW(min)}} + ESR \times \left[I_{L1a(Peak)} + I_{L1b(Peak)} \right] \quad (6)$$

If very low-ESR (e.g., ceramic) output capacitors are used, the ESR can be ignored and the equation reduces to

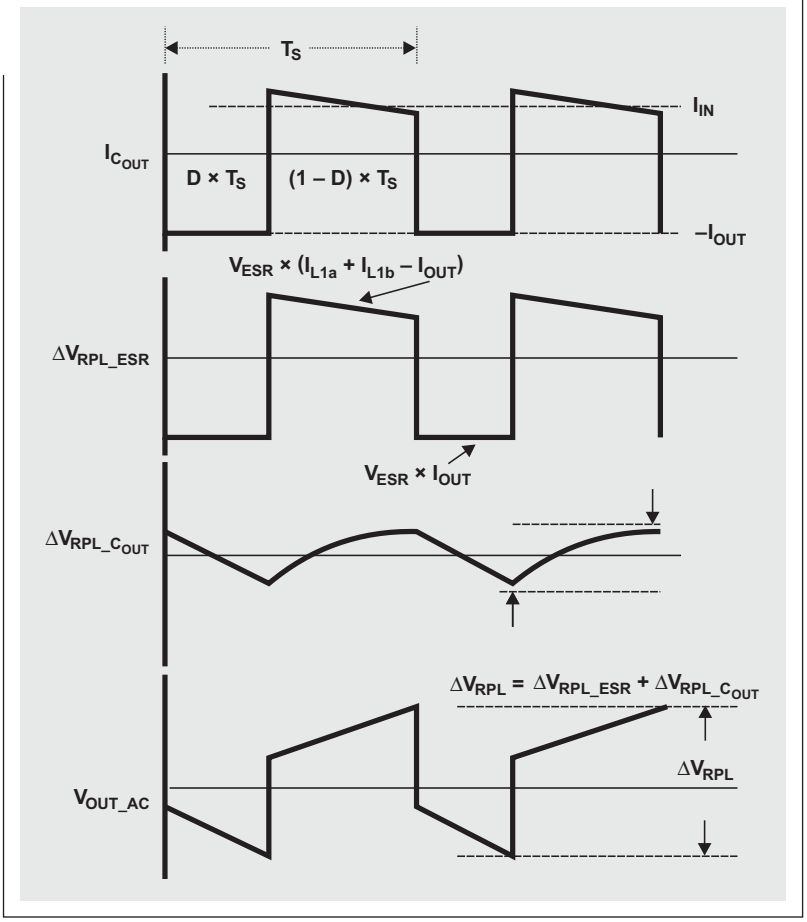
$$C_{OUT} \ge \frac{I_{OUT} \times D(max)}{\Delta V_{RPL} \times f_{SW(min)}}, \quad (7)$$

where $f_{SW(min)}$ is the minimum switching frequency. A minimum capacitance limit may be necessary to meet the application's load-transient requirement.

The output capacitor must have an RMS current rating greater than the capacitor's RMS current, as computed in Equation 8:

$$I_{C_{OUT}(RMS)} = I_{OUT} \times \sqrt{\frac{D(max)}{1 - D(max)}} \quad (8)$$

Figure 5. Ripple voltage of output capacitor



The input capacitor sees fairly low ripple currents due to the input inductor. Like a boost converter, the input-current waveform is continuous and triangular; therefore, the input capacitor needs the RMS current rating,

$$I_{C_{IN}(RMS)} = \frac{\Delta I_L}{\sqrt{12}}. \quad (9)$$

The coupling capacitor, C_P, sees large RMS current relative to the output power:

$$I_{C_P(RMS)} = I_{IN}' \times \sqrt{\frac{1 - D(max)}{D(max)}} \quad (10)$$

From Figure 3, the maximum voltage across C_P is

$$V_{Q1(max)} - V_{L1b(max)} = V_{IN} + V_{OUT} - V_{OUT} = V_{IN}.$$

The ripple across C_P is

$$\Delta V_{C_P} = \frac{I_{OUT} \times D(max)}{C_P \times f_{SW}}. \quad (11)$$

Selecting active components

The power MOSFET, Q1, must be carefully selected so that it can handle the peak voltage and currents while minimizing power-dissipation losses. The power FET's current rating (or current limit for a converter with an integrated FET) will determine the SEPIC converter's maximum output current.

As shown in Figure 3, Q1 sees a maximum voltage of $V_{IN(max)} + V_{OUT}$. As shown in Figure 4, Q1 must have a peak-current rating of

$$I_{Q1(Peak)} = I_{L1a(Peak)} + I_{L1b(Peak)} = I_{IN}' + I_{OUT} + \Delta I_L. \quad (12)$$

At the ambient temperature of interest, the FET's power-dissipation rating must be greater than the sum of the conductive losses (a function of the FET's $r_{DS[on]}$) and the switching losses (a function of the FET's gate charge) as given in Equation 13:

$$P_{D\_Q1} = I_{Q1(RMS)}^2 \times r_{DS(on)} \times D(max) + I_{Q1(Peak)} \times \left[V_{IN(min)} + V_{OUT} + V_{FWD} \right] \times \frac{t_{Rise} + t_{Fall}}{2} \times f_{SW}, \quad (13)$$

where t_{Rise} is the rise time on the gate of Q1 and can be computed as Q1's gate-to-drain charge, Q_{GD}, divided by the converter's gate-drive current, I_{DRV}. Q1's RMS current is

$$I_{Q1(RMS)} = \frac{I_{IN}'}{\sqrt{D(max)}}. \quad (14)$$

The output diode must be able to handle the same peak current as Q1, $I_{Q1(Peak)}$. The diode must also be able to withstand a reverse voltage greater than Q1's maximum voltage ($V_{IN[max]} + V_{OUT} + V_{FWD}$) to account for transients and ringing. Since the average diode current is the output current, the diode's package must be capable of dissipating up to $P_{D\_D1} = I_{OUT} \times V_{FWD}$.

Design example

A DC/DC converter is needed that can provide 12 V at 300 mA (maximum) with 90% efficiency from an input voltage ranging from 9 to 15 V. We select the TPS61170, which has a 38-V switch, a minimum switch-current limit of 0.96 A, and a 1.2-MHz nominal (1.0-MHz minimum) switching frequency. The maximum output voltage ripple allowed is 100 mV_{PP}. The maximum ambient temperature is 70ºC, and we will use a high-K board. In Reference 1, Ray Ridley explains how to compensate the control loop at the link.

Table 1 summarizes the computations using the equations given earlier. Equations 8 through 11 are not shown because ceramic capacitors with low ESR, high RMS current ratings, and the appropriate voltage ratings were used. Figure 6 shows the schematic. Figure 7 shows the design's efficiency with a Coiltronics DRQ73 inductor and a Wurth 744877220. Figure 8 shows the device operation in deep CCM.

References

1. Ray Ridley. (Nov. 2006). Analyzing the SEPIC converter. *Power Systems Design Europe* [Online]. Available: http://www.powersystemsdesign.com/design_tips_nov06.pdf
2. Robert W. Erickson and Dragan Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. (New York: Springer Science+Business Media LLC, 2001).
3. John Betten and Robert Kollman. (Jan. 25, 2006). No need to fear: SEPIC outperforms the flyback. *Planet Analog* [Online]. Available: http://www.planetanalog.com/showArticle.jhtml?articleID=177103753

Related Web sites

power.ti.com
www.ti.com/sc/device/TPS61170

Table 1. Computations for SEPIC design example

DESIGN EQUATION	COMPUTATION	SELECTED COMPONENT/RATING
Passive Components		
(1)	$D(max) = \frac{12\ V + 0.5\ V}{12\ V + 9\ V + 0.5\ V} = 0.58$	N/A
(2) and (3)	$\Delta I_L = I_{IN}' \times 30\% = \frac{0.3\ A \times 12\ V}{9\ V \times 90\%} \times 30\% = 0.44\ A \times 30\% = 0.13\ A$	N/A
(4)	$L1a = L1b = \frac{1}{2} \times \frac{9\ V \times 0.58}{0.13\ A \times 1\ MHz} = 20.1\ \mu H$	Coiltronics DRQ73: 22 µH, 1.6 A, and 110 mΩ
(5)	$I_{L1a(Peak)} = 0.44\ A \times \left(1 + \frac{30\%}{2}\right) = 0.51\ A$	
(7)	$C_{OUT} \geq \frac{0.3\ A \times 0.58}{0.1\ V \times 1\ MHz} = 1.74\ \mu F$	4.7-µF, 25-V X5R ceramic
Active Components		
(12)	$I_{Q1(Peak)} = 0.44\ A + 0.3\ A + 0.13\ A = +0.87\ A$	TPS61170 with 0.96-A-rated switch. Capable of dissipating 825 mW at 70°C.
(14)	$I_{Q1(RMS)} = \frac{0.44\ A}{\sqrt{0.58}} = 0.58\ A$	
(13)	$P_{D\_Q1} = (0.58\ A)^2 \times 0.3\,\Omega \times 0.58 + 0.87\ A \times (9\ V + 12\ V + 0.5\ V) \times 10\ ns \times 1\ MHz = 246\ mW$	
—	$P_{D\_D1} = 0.3\ A \times 0.5\ V = 150\ mW$	MBA140: 1 A, 40 V

Figure 6. SEPIC design with 9- to 15-V V_{IN} and 12-V V_{OUT} at 300 mA

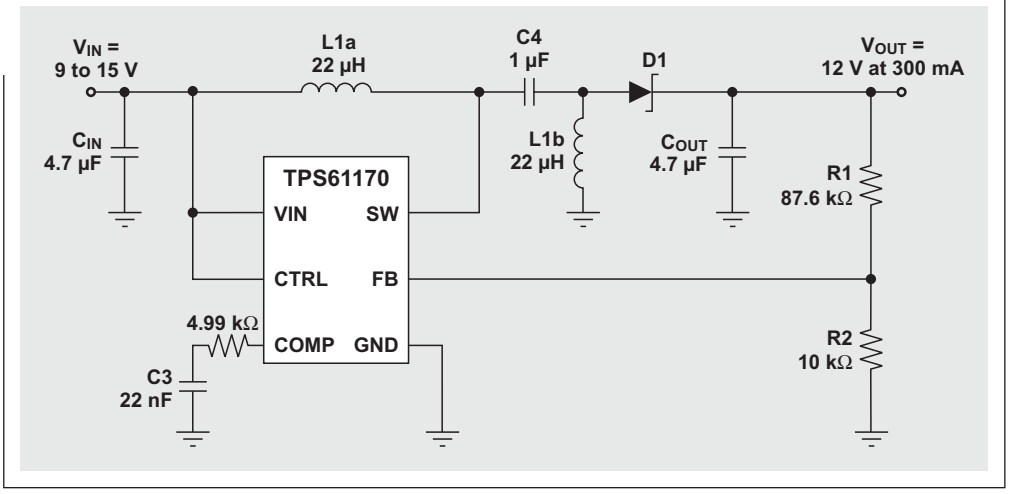


Figure 7. Efficiency of example SEPIC design

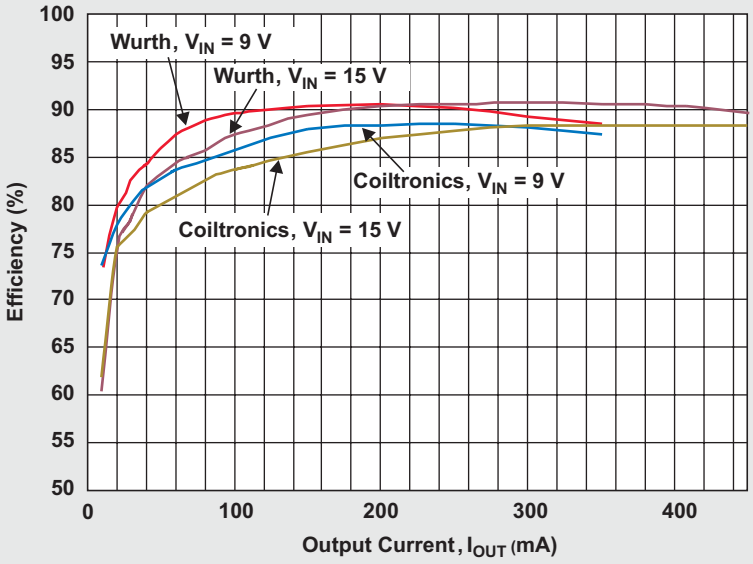
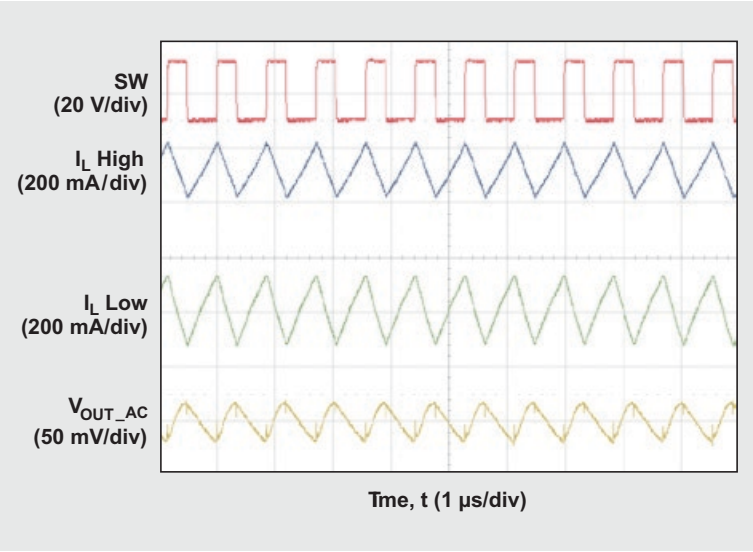


Figure 8. Operation at V_{IN} = 9 V and I_{OUT} = 200 mA



Input impedance matching with fully differential amplifiers

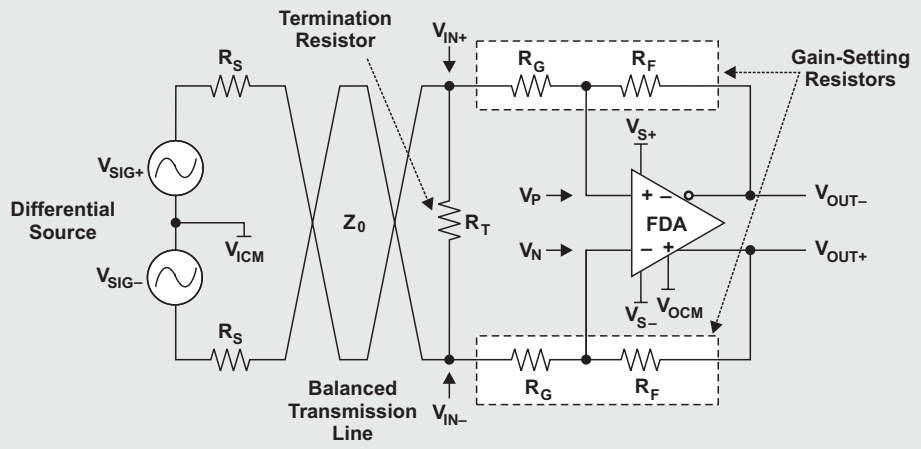
By Jim Karki
Member, Technical Staff, High-Performance Analog

Introduction

Impedance matching is widely used in the transmission of signals in many end applications across the industrial, communications, video, medical, test, measurement, and military markets. Impedance matching is important to reduce reflections and preserve signal integrity. Proper termination results in greater signal integrity with higher throughput of data and fewer errors. Different schemes have been employed; source termination, load termination, and double termination are the most commonly used. Double termination is generally recognized as the best method to reduce reflections, while source and load termination have the advantage of increased signal swing. With source and load termination, either the source or the load (not both) is terminated with the characteristic impedance of the transmission line. With double termination, both the source and the load are terminated with that impedance. No matter what impedance-matching scheme is chosen, the termination impedance to implement must be accurately calculated.

In the last few years, fully differential amplifiers (FDAs) have grown in popularity; and, while similar in theory to inverting operational amplifiers, they have important differences that need to be understood when input impedance matching is considered. This article shows how to analyze the input impedance of an FDA. Circuit analysis is performed to aid understanding of the key design points, and a methodology is presented to illustrate how to approach the design variables and calculate component values. A spreadsheet and TINA-TI™ SPICE models are available as design aids.

Figure 1. FDA with differential source



TERM	DEFINITION
R_G, R_F	Gain-setting resistors for the amplifier
R_S	Impedance of the signal source, which should be balanced
R_T	Used when $2R_G$ is higher than the required input termination impedance
V_{ICM}	Common-mode voltage of the signal source
V_{OCM}	Output common mode of the FDA
$V_{S\pm}$	Power supply to the amplifier
$V_{Sig\pm}$	Differential input-signal source
Z_0	Characteristic impedance of the balanced transmission line from the source to the amplifier input

FDA circuit overview

FDAs are broadband, DC-coupled amplifiers for balanced differential signals and have a unique ability to convert broadband, DC-coupled, single-ended signals into balanced differential signals.

The input-impedance analysis of FDAs is very similar to that of two inverting operational amplifiers. The key difference is that with two inverting operational amplifiers, the input common-mode voltage is controlled by the voltage applied to the positive input; while with FDAs, the output common-mode voltage is controlled via a second loop contained within the amplifier. If the input is differential, the analysis is just as easy for an FDA as for an inverting op-amp circuit, but more difficult when the input is single-ended.

For maximum performance, the FDA must be balanced, which again is easier to analyze if the input is differential.

Due to this, we will first look at the input impedance in the differential case and then use that as a starting point to consider the single-ended case.

The fundamentals of FDA operation are presented in Reference 1. Please refer to it for voltage definitions, gain equations, derivations, and terminology.

Analysis of differential-signal input

A differential drive and termination into an FDA is shown in Figure 1. An FDA works using negative feedback around the main loop of the amplifier, which tends to drive the error voltage across the input terminals, V_N and V_P, to zero, depending on the loop gain.

For analysis, it is convenient to assume that the FDA is an ideal amplifier with no offset and infinite gain. Looking at the input of the amplifier differentially and using the virtual-short concept (Figure 2) from an inverting-amplifier topology, we can express the input impedance as $Z_{IN} = R_T \parallel 2R_G$.

For an example of how to select the value of R_T, let's look at a differential source driving a twisted pair to the FDA. $Z_0 = 100\ \Omega$ is common for twisted-pair cables. For double termination, we want the source to provide $R_S = 50\ \Omega$ on each side for 100-Ω differential output impedance, and we want the input of the FDA to present a 100-Ω differential load. If $R_G = 402\ \Omega$, we then need R_T to be 114.2 Ω; so we select the nearest standard value, 115 Ω, for R_T.

The gain of the circuit from the differential source is

$$\frac{V_{SIG\pm}}{V_{OUT\pm}} = \left(\frac{R_T \parallel 2R_G}{R_T \parallel 2R_G + 2R_S}\right)\left(\frac{R_F}{R_G}\right). \quad (1)$$

If we assume that the input impedance matches the source impedance, then

$$\frac{V_{SIG\pm}}{V_{OUT\pm}} = \left(\frac{1}{2}\right)\left(\frac{R_F}{R_G}\right). \quad (2)$$

It is standard practice to take the gain from the terminated input, in which case

$$\frac{V_{IN\pm}}{V_{OUT\pm}} = \left(\frac{R_F}{R_G}\right). \quad (3)$$

It is recommended that R_F be limited to a range of values for best performance. A resistance value that is too high will add excess noise and possibly interact with parasitic board capacitance to reduce the bandwidth of the amplifier; a value that is too low will load the output, causing increased distortion. Therefore, we need to pick a range of desired values for R_F and calculate R_G for the desired gain. For example, the THS4509 performs best with R_F in the range of 300 to 500 Ω. So, depending on the gain we want from the FDA, there will come a point where $2R_G$ equals the required termination of the transmission line. In this case, no R_T resistor is required.

In design, the target gain and Z_0 are set by the system design. We select the value of R_F first, then calculate R_T and R_G to match the gain and make $Z_{IN} = Z_0$. This is easily done by setting up the equations in a spreadsheet. To see an example Excel® worksheet, click on the Attachments tab or icon on the left side of the Adobe® Reader® window. Open the file FDA_Input_Impedance.xls, then select the Differential Input worksheet tab.

Figure 2. Balanced input impedance

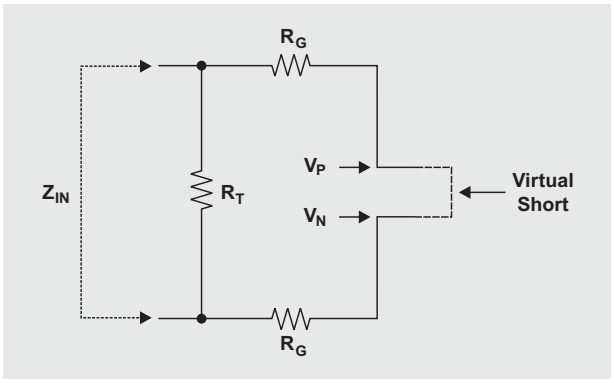
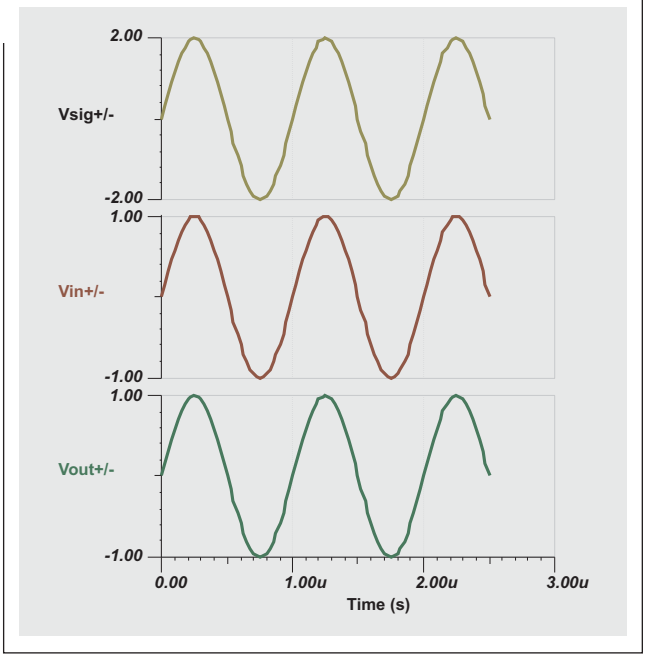


Figure 3. TINA-TI simulation of FDA waveforms with differential input impedance



SPICE simulation is a great way to validate the design. To see a TINA-TI simulation circuit of the example just given, click on the Attachments tab or icon on the left side of the Adobe Reader window. If you have the TINA-TI software installed, you can open the file FDA_Diff_Input_Impedance.TSC to view the circuit example. To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button.

There are numerous ways to find the input impedance in SPICE, but from the simulation waveforms shown in Figure 3, we see the expected input and output voltages for double termination with equal impedances.

Analysis of single-ended signal input

In Figure 4, the differential source circuit shown in Figure 1 is modified for a single-ended, DC-coupled source. To keep balance in the circuit, the source is converted to a single-ended source referenced to V_{ICM}; R_T is split into two resistors of equal value with the center point tied to ground; and the negative input is tied to V_{ICM} via R_S.

Another scenario is when the source is an RF, IF, or CATV-type class-A amplifier that is designed with intrinsic output impedance. With this type of amplifier, AC coupling of the outputs is usually required via a DC-blocking capacitor to avoid disturbing the DC bias point of the amplifier. In this case, R_T on the positive side and $R_{EQ} = R_G + R_S \parallel R_T$ on the negative side (where R_S is the output impedance of the RF/IF/CATV amplifier) should be tied to ground via a DC-blocking capacitor of the same size. This is shown in Figure 5. Note that in this configuration the FDA will self-bias input and output pins to the common-mode voltage set by the V_{OCM}.

In actual implementation, the source may be DC-coupled (Figure 4) and have a common-mode reference that is not ground. In this case, care must be taken to tie R_S to the same common reference for balance. Also note that DC current will flow in R_T when tied to ground. When a source is DC-coupled with a ground-referenced source, R_S and R_T on the negative side should be tied to ground.

The last scenario makes the circuit analysis easier and will provide the solution for the other scenarios as well.

Figure 4. FDA with single-ended source

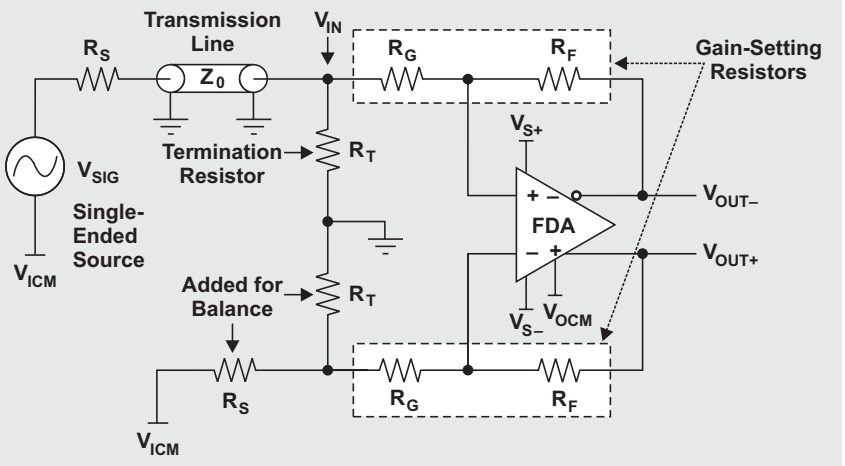


Figure 5. FDA with AC-coupled RF/IF/CATV amplifier input

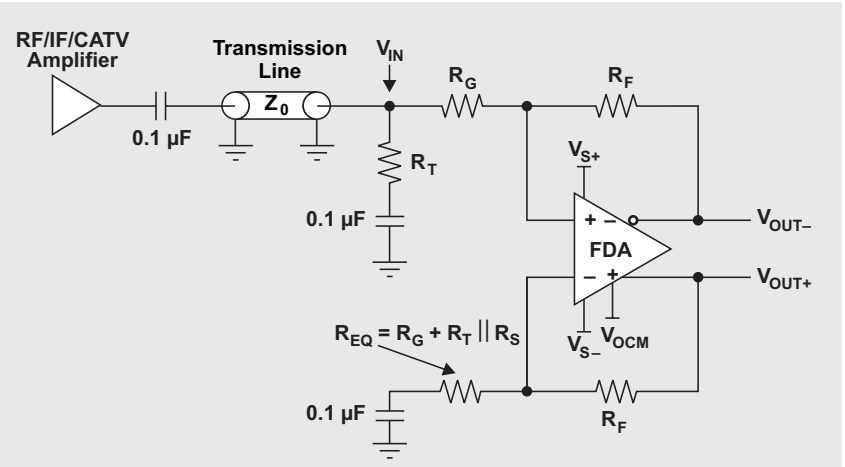


Figure 6 shows the case where the source is ground-referenced and R_S and R_T are combined with R_G into one resistor of equivalent value, $R_{EQ} = R_G + R_T \parallel R_S$, which is tied to ground. We will base the analysis of the input impedance on this circuit.

With single-ended input, only one side of the FDA is actively driven, and the other side is grounded (or tied to some reference as discussed earlier). With this scenario, the input pins of the amplifier are not fixed at a DC voltage but will have an AC component. So even though the error voltage across the inputs is driven to zero by the action of the amplifier, we can no longer use the virtual-short concept to derive the input impedance. Instead we must use an alternate, more complex method.

The first step in analyzing the circuit is to break it along the center vertical axis into positive and negative input sides. Then the positive side is converted to its Thevenin equivalent so the circuit can be analyzed and a solution can be developed. Finally, the components on the negative side are balanced to make sure the amplifier gives balanced output. In the positive side of the circuit shown in Figure 7,

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} \parallel R_T = Z_A \parallel R_T. \quad (4)$$

The Thevenin equivalent of the positive side is shown in Figure 8. In this circuit,

$$I_{IN} = \frac{V_{IN} - V_{OUT-}}{R_F + R_G}. \quad (5)$$

We can treat V_{IN} as a summing node, or solve the node equation to get

$$V_{IN} = \frac{V_{SIG}\left(\frac{R_T}{R_S + R_T}\right)(R_G + R_F) + V_{OUT-}(R_S \parallel R_T)}{R_G + R_F + R_S \parallel R_T}. \quad (6)$$

At this point we make use of Equation 12 for output voltage from page 10 of Reference 1, with simplification and some slight changes in nomenclature. In the analysis we need to find V_{OUT-} in relation to V_{IN}, so β_+ will be used here in place of β_1 for the feedback factor in the Thevenin equivalent of the positive side. For the feedback factor of the negative side, β_- will be used in place of β_2. To clarify, the different terms that arise for the feedback factors are artifacts of the analysis, and in reality the circuit will have balanced feedback factors as long as $R_{EQ} = R_G + R_T \parallel R_S$. Let's also zero out V_{OCM} because it is a DC level, and zero out $V_{IN}-$ because we grounded the input to the negative side of the amplifier.

With these changes in nomenclature, and substituting the Thevenin equivalent shown earlier, we can derive the equation for only the amplifier's AC or signal response to V_{OUT-}, which we will call $V_{OUT-\ (AC\ only)}$:

$$V_{OUT-\ (AC\ only)} = \frac{-\left[V_{SIG}\left(\frac{R_T}{R_S + R_T}\right)\right](1 - \beta_+)}{\beta_+ + \beta_-}, \quad (7)$$

where

$$\beta_+ = \frac{R_G}{R_F + R_G}, \text{ and } \beta_- = \frac{R_G + (R_S \parallel R_T)}{R_F + R_G + (R_S \parallel R_T)}.$$

Figure 6. FDA with DC-coupled, single-ended source referenced to ground

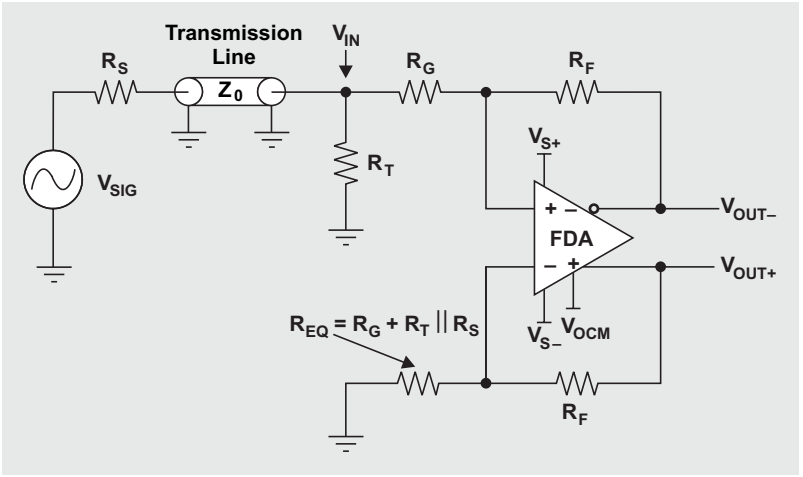


Figure 7. Positive side of FDA circuit

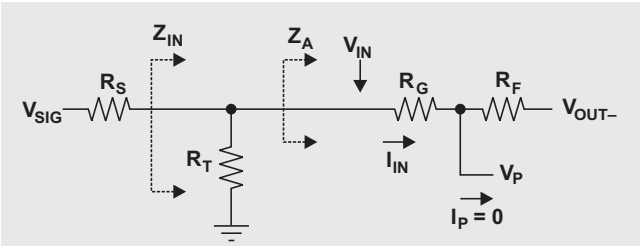
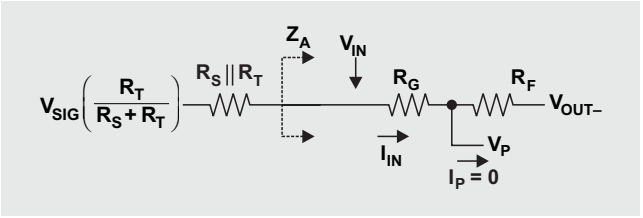


Figure 8. Thevenin equivalent of positive side



With a significant amount of algebra and substitution, we solve for Z_A and then use Equation 4 to find Z_{IN}:

$$Z_A = \frac{(R_G + R_F)(\beta_+ + \beta_-)}{\beta_- + 1} \quad (8)$$

The gain from the terminated input to the differential output, assuming the circuit is balanced, is

$$\frac{V_{OUT\ (Differential)}}{V_{IN}} = 2\left(\frac{R_F}{R_G + R_S \parallel R_T}\right)\left(\frac{R_T}{R_S + R_T}\right). \quad (9)$$

The output DC common mode is set by the input to V_{OCM}.

It would be useful to have a closed-form equation to solve for R_T to satisfy both Equations 8 and 9, but none could be found. One solution is to guess values and iterate, but sometimes that fails to find a solution. A more practical approach is to modify the equations and solve using Equations 10 and 11.

$$\frac{1}{R_T} = \frac{1}{Z_0} - \left[\frac{1 - GF}{2(1 + GF)}\right]\left(\frac{2GF}{2R_F - Z_0GF}\right), \quad (10)$$

where Z_0 is the desired termination, G is the target gain from terminated input to output, and F is a factor less than 1 that depends on the gain and value of R_F. The result is fed into Equation 11 to solve for R_G:

$$R_G = \left[\frac{2R_TR_F}{G(Z_0 + R_T)}\right] - Z_0 \parallel R_T \quad (11)$$

In design, the target gain and Z_0 are set by the system design; and, as noted earlier, it is recommended that R_F be limited to a range of values for best performance. So we select the value of R_F first and then try values for F until $Z_{IN} = Z_0$. This is easily done by setting up the equations in a spreadsheet that can simultaneously calculate with incremental values, and then selecting the appropriate values. To see an example Excel worksheet, click on the Attachments tab or icon on the left side of the Adobe Reader window. Open the file FDA_Input_Impedance.xls, then select the Single-Ended Input worksheet tab.

For an example of how to select the value of R_T, let's look at a single-ended source driving a coax to the FDA with $Z_0 = 50\ \Omega$. For double termination, we want the source to provide $R_S = 50\text{-}\Omega$ output impedance, and we want the input of the FDA to present a 50-Ω single-ended load. Assuming that we want a gain of 1 from the terminated input and that $R_F = 402\ \Omega$, we can use the spreadsheet to calculate the nearest standard values for $R_G = 392\ \Omega$, $R_T = 54.9\ \Omega$, and $R_{EQ} = 422\ \Omega$, which gives us $Z_{IN} = 49.73\ \Omega$ and a gain of 1.006 V/V.

Again we use SPICE simulation to validate the design. To see a TINA-TI simulation circuit of the example just given, click on the Attachments tab or icon on the left side of the Adobe Reader window. If you have the TINA-TI software installed, you can open the file FDA_Single_Ended_Input_Impedance.TSC to view the circuit example. To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button.

There are numerous ways to find the input impedance in SPICE, but from the simulation waveforms shown in Figure 9, we see the expected input and output voltages for double termination with equal impedances.

Reference

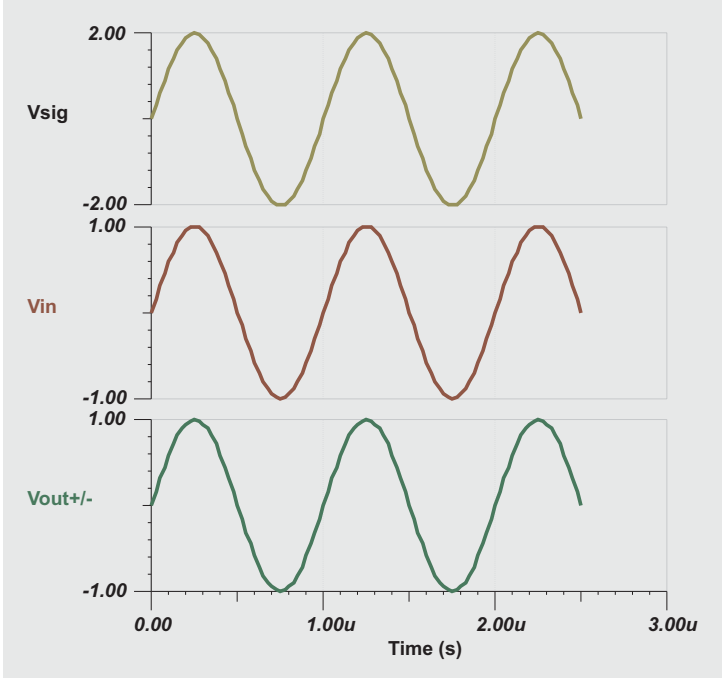
For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. Jim Karki, "Fully Differential Amplifiers," Application Report	sloa054

Related Web sites

amplifier.ti.com
www.ti.com/tina-ti

Figure 9. TINA-TI simulation of FDA waveforms with single-ended input impedance

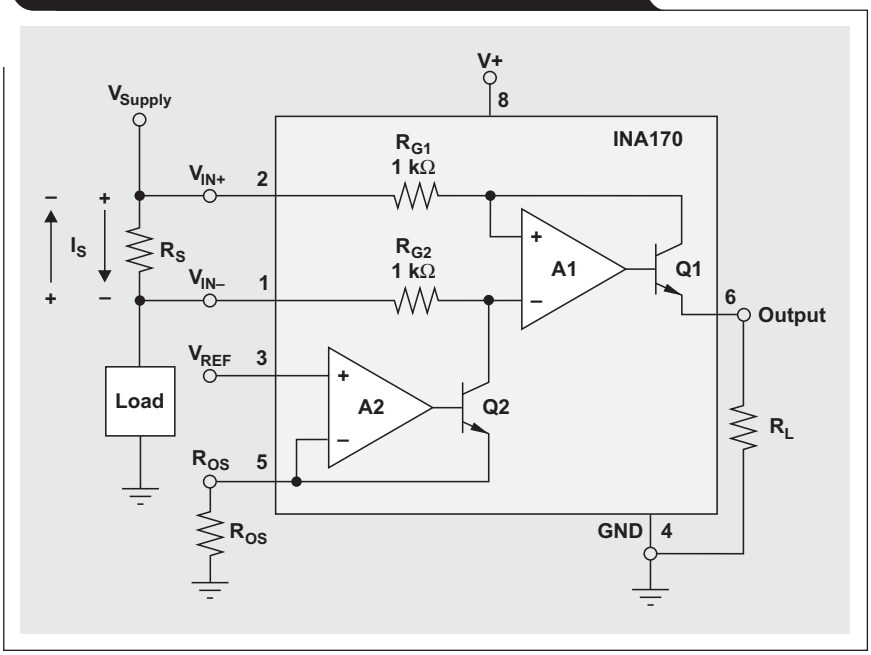


A dual-polarity, bidirectional current-shunt monitor

By Thomas Kuehl
Senior Applications Engineer

Current-shunt-monitor ICs are an extension of the instrumentation amplifier family of products. They provide an easy method of monitoring circuit current and possess similarities to the sensitive analog voltmeter and external shunt resistor commonly used to measure current in the past. The analog voltmeter registered a small voltage drop that developed when current passed through a shunt resistor. With a current-shunt monitor, the voltmeter has been replaced by a specially adapted instrumentation amplifier that amplifies the voltage developed across the shunt resistor. An output measure is provided that is proportional to the current through the resistor. Analog voltmeters were commonly designed for a full-scale voltage of 50 or 100 mV, and the current-shunt monitor operates with comparable input-voltage levels. Instead of an analog meter-scale indication, the current-shunt monitor provides a voltage or current output level, or a digital output code, that directly corresponds to the measured current level.

Figure 1. The INA170 connected for bidirectional current monitoring



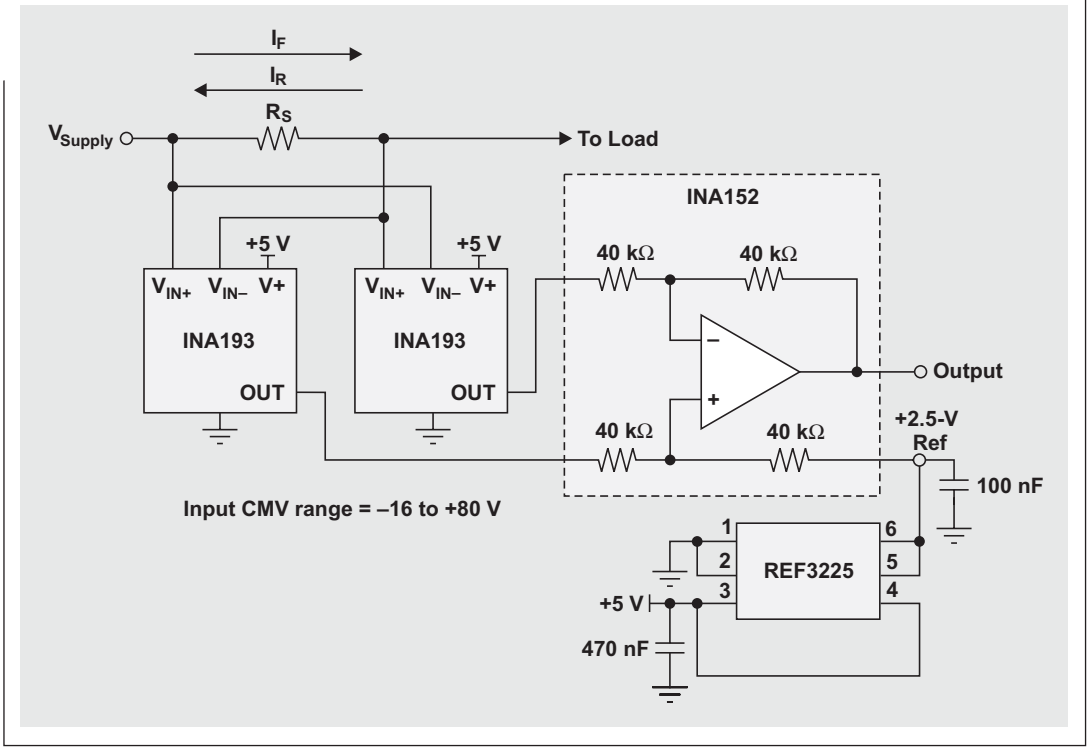
A variety of current-shunt monitors are available that are designed for high-side or low-side circuit connection, with some offering different user functions. Often the voltage ranges of the current-shunt-monitor supply and the common-mode input are independent of each other. This allows the current-shunt monitor to be operated from a convenient supply-voltage level independent of the input voltage. Many applications need only monitor current flowing in one direction, and a current-shunt monitor such as the INA138/168 provides this capability. A monitor intended for single-direction, or unidirectional, current flow is referred to as a unidirectional current-shunt monitor. Other applications require a bidirectional current-shunt monitor where the circuit current can flow and be monitored in either direction.

An example of a bidirectional current-shunt monitor is the INA170. It is powered by a single supply voltage of +2.7 to +40 V, while the input common-mode voltage (CMV) may be any voltage between +2.7 and +60 V. The input CMV is the external voltage that is applied to the current-shunt-monitor input and provides current to the output load. When the current through the shunt resistor is zero, both inputs of the current-shunt monitor are ideally at the same CMV potential; but when a current flows through the shunt resistor, a differential voltage is developed and the inputs become separated by that amount. This voltage difference is amplified by the gain factor of the current-shunt monitor.

The bidirectional property allows the INA170 to monitor current between two voltage potentials that are more positive or negative relative to each other. A simple illustration of a bidirectional-current-flow system is a motor that draws current from a battery when operating at a constant speed or accelerating, but then acts as a generator, returning current to the battery during deceleration. Figure 1 shows the INA170 connected for bidirectional current monitoring.

Thus, two important current-shunt-monitor operating parameters are the unidirectional or bidirectional input voltage characteristic and the CMV range. The operational CMV range often extends from near 0 V to a specified maximum positive voltage, but some current-shunt monitors include a negative voltage range as well. For example, the INA193 through INA198 current-shunt-monitor family provides a CMV range of –16 to +80 V. These devices are unidirectional; so even if the input voltage is a negative voltage, the output has to be more negative for current to

Figure 2. Two INA193 ICs configured as a bidirectional current-shunt monitor



flow in the correct direction. Two of the unidirectional current-shunt-monitor ICs may be interconnected to form a bidirectional current-shunt monitor with a CMV range that extends from –16 to +80 V. The addition of the INA152 instrumentation amplifier and +2.5-V reference completes the circuit. A circuit schematic for the INA193 bidirectional current-shunt monitor is shown in Figure 2.

Recently, a customer described an application where monitoring a DC motor's current was necessary. It was an automotive application, and the system supply was available to power a current-shunt monitor. The customer wanted to know the current levels when the motor was running normally in the forward direction and in reverse where a negative, back EMF developed. The circuit shown in Figure 2 is appropriate for this application; but the customer wanted to keep the number of components and the cost to a minimum, even if some precision had to be sacrificed. This called for a different approach.

Earlier it was mentioned that current-shunt monitors are an extension of instrumentation amplifiers. Also included in the family are difference amplifiers, which consist of an instrumentation-grade operational amplifier and four or more precisely matched resistors. The difference amplifier amplifies the difference in voltages applied to the two inputs by a fixed gain. Gain and common-mode rejection of the difference amplifier are optimized by precise laser trimming of four thin-film resistors included on the integrated circuit die. Difference amplifiers with a fixed gain of 1:1, 10:1, and 100:1 V/V are commonly available; however, there is a unique product—the INA159—that has a fixed gain setting of 0.2 V/V. Its primary role is to serve as a level-translation amplifier between sensors having a bipolar output voltage with a range of ±10 V, and a modern analog-to-digital converter having a unipolar input range of 0 to 5 V. The INA159 is a true difference amplifier that can sense a differential voltage of either polarity. Its input CMV range extends from –12.5 to +17.5 V when powered from a single +5-V supply. These features allow the INA159 to be employed as a dual-polarity, bidirectional current monitor. An additional instrumentation or operational amplifier needs to be included after the INA159 to increase the overall gain of the monitor circuit.

Figure 3. INA159 dual-polarity, bidirectional current-shunt-monitor circuit

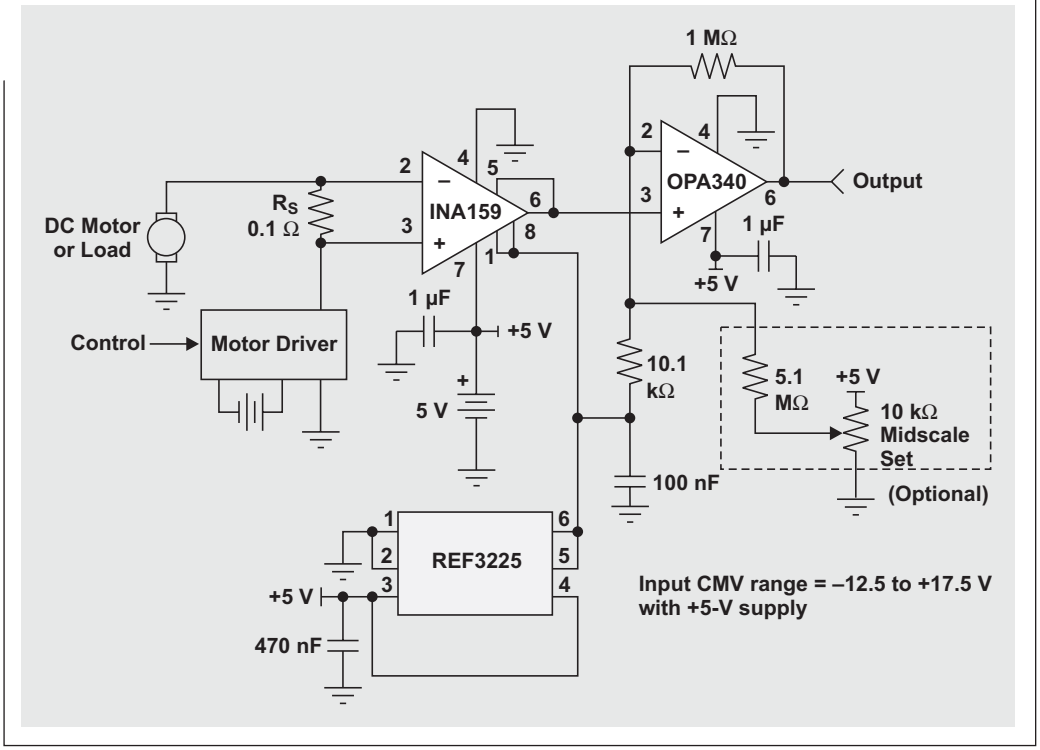


Figure 3 shows the circuit of the INA159 current-shunt-monitor stage, followed by an OPA340 CMOS operational-amplifier gain stage. The OPA340 was selected because its near rail-to-rail input and output swing ranges allow the circuit's output voltage to approach 0 and 5 V at the extremes. The INA159 gain is +0.2 V/V, while the OPA340 gain is set to +100 V/V, for an overall circuit gain of +20 V/V. A higher OPA340 closed-loop gain could be used to increase sensitivity, but the DC errors and bandwidth would suffer. Also, the shunt resistor R_S, could be increased from 0.1 Ω to a larger value. This would increase the INA159 output, but the consequences of the larger voltage drop and higher resistor power dissipation should be evaluated before doing so.

The output voltage delivered from the INA159 current-shunt-monitor circuit is centered at a level of about +2.5 V. This is the approximate voltage level at the OPA340 output when no current is flowing through R_S. Figure 4 shows an oscilloscope image of the INA159 current-shunt monitor's output response when the input circuit is being driven by a 24-V_{PP}, 1-kHz sine wave. This input-voltage waveform is recorded as the upper trace image. The resistive load in the input circuit is 12 Ω, resulting in peak current levels of ±1 A. The lower trace is that of the OPA340 output voltage swinging from 0.5 to 4.5 V, indicating a peak current of approximately ±1 A. A center-scale, manual zeroing circuit is included in the OPA340 stage. It can be excluded if an exact 2.5-V center-scale voltage is not necessary. The INA159 and OPA340 combined exhibit a bandwidth of well over 100 kHz, making this circuit usable for a wide variety of AC-current-monitoring applications.

Figure 4. Input/output waveforms of current-shunt-monitor circuit

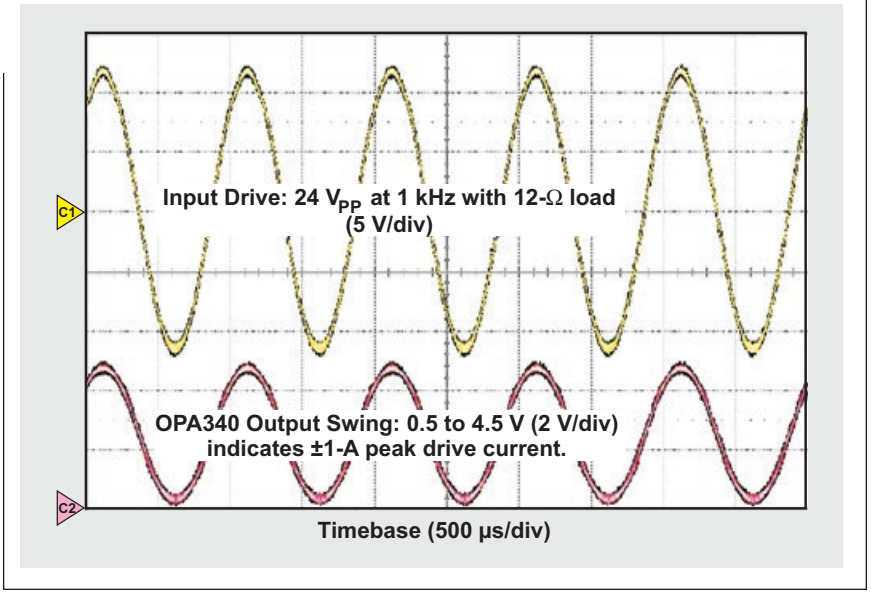


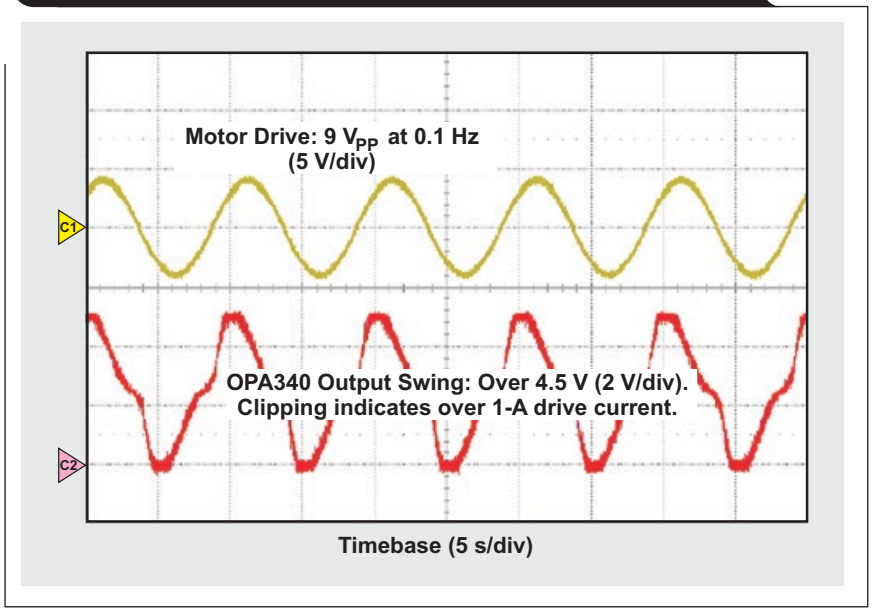
Figure 5 shows oscilloscope images of the INA159 current-shunt monitor monitoring the current of a DC pancake motor under load. The motor is being driven by a slow 9-V_{PP}, 0.1-Hz sine wave such that the armature direction follows the sine function, reversing direction every half cycle. This input drive voltage, shown as the upper trace, had to be adjusted to keep the motor from drawing more than 1 A of current. The lower trace shows the OPA340 output voltage where the peak motor current exceeds 1 A. Some evidence of clipping is seen at the OPA340 output as output-voltage-swing limits. With proper sizing of components, the circuit can be optimized for monitoring this particular motor's current levels. Nonetheless, this illustrates the utility of the INA159 in a motor-current-monitoring application.

Accuracy of the INA159 current-shunt monitor was measured at a little better than 4.5%. Standard 1% resistors were used, with no special selection being made. The circuit accuracy could be improved by replacing the OPA340 circuit with a precision, single-supply instrumentation amplifier such as the INA326. However, the AC bandwidth will decrease and the cost will be higher.

Related Web sites

amplifier.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with INA138, INA152, INA159, INA168, INA170, INA193, INA326, or OPA340

Figure 5. Input/output waveforms of current-shunt-monitor circuit of DC motor



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