

# Tips and tricks for high-speed, high-voltage measurement

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## Introduction

High-voltage circuits that also have high-speed devices, such as the recently introduced gallium nitride (GaN) and silicon carbide (SiC) power FETs, are posing measurement challenges to power conversion designers. Lower-voltage GaN FETs (<100 V), when paired properly to low-inductance gate drivers, can be switched in as little as 1 ns. High-voltage 600-V GaN FETs, and even higher-voltage 1200-V SiC FETs with special low-inductance layout and high-current drivers, also can be switched at 1-MHz rates with rise and fall times of under 20 ns. During design validation, it is a challenge to manually probe such high-voltage circuits safely in compliance with standards like the Environmental Safety and Health (ESH) guidelines. Another consideration is the requirement to protect test personnel from accidentally touching energized areas with dielectric safety barriers and the use of personal safety equipment such as rubber gloves and eye protection. These safety concerns make probing even more difficult.

This article describes a few high-speed and high-voltage probe circuits and methods to measure probe performance. The objective is to show how to bring high voltages down to safe levels with good DC accuracy and high AC fidelity, and then be able to route these signals over coax into 50-Ω equipment.

## Measurement review

Measuring the voltage of a circuit with a probe loads it both resistively and capacitively, and at high frequencies, even inductively. Loading the circuit also adds distortion and ringing to the original signal. The concept is similar to the Heisenberg uncertainty principle, which is about the quantum nature of an electron's position and momentum and reveals something about the science of electrical

measurement. The basic conclusion is that any attempt to measure voltage or current actually changes it.

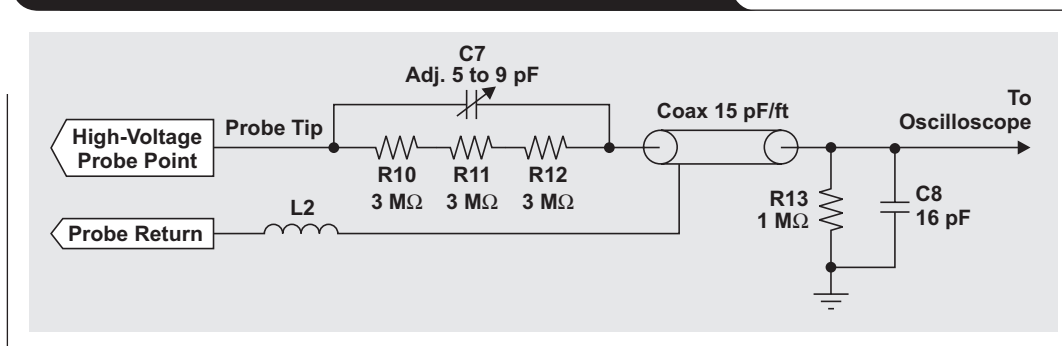
Measuring current with a current probe adds loop area and inductance, as well as distortion and time delays that can complicate estimates for instantaneous power dissipation ( $V \times I$ ). Measuring currents by measuring the voltage across a low-value shunt resistor is also a common approach. However, the inductance of the resistor must be considered when frequencies are above 10 MHz, or rise and fall times below 30 ns are present. At the megahertz switching frequencies possible with wide-bandgap power conversion and with the short rise and fall times present, it is important to revisit probe circuits and some of their limitations.

Figure 1 shows a simplified schematic of a 10:1 10-MΩ, 500-MHz scope probe. Resistors R10, R11 and R12 provide a 9-MΩ resistance in the tip of the probe in parallel with a variable compensation capacitor (C7). At DC, the 10-to-1 divide ratio is obtained by the 1-MΩ DC input resistor of the scope (R13) and the 9-MΩ resistance in the tip. To give 1% or better accuracy in voltage measurement, the circuit to be measured must have a source impedance of 100 kΩ or less. Active probes can have higher input impedances, but typically are limited to tens of volts<sup>[1]</sup>.

## Wide-bandgap power FETs

Recently introduced wide-bandgap power semiconductor devices such as SiC and GaN FETs are helping designers meet next-generation efficiency and power-density requirements. These wide-bandgap devices support higher breakdown voltages across a smaller area than traditional silicon (Si) devices. Designers of these devices are reducing capacitances and geometries to improve speed through the channels. The high mobility of GaN and the lateral structure of GaN power FETs gives rise to

Figure 1. Simplified schematic of an oscilloscope probe



higher capabilities of carrier concentration and lower on-resistance ( $R_{DS(on)}$ ) values when compared to Si devices of the same size. These features allow GaN FETs to be about one-third the size of Si FETs, yet have equivalent voltage and current carrying capability.

Reverse recovery charge ( $Q_{rr}$ ) is one of the dominant power-loss mechanisms of Si power-FET switching. Both GaN and SiC FETs are majority-only carrier devices. GaN FETs have no body diode, which means they have no reverse recovery charge ( $Q_{rr}$ ). SiC FETs do have a body diode like Si devices, but with lower stored reverse charge. When validating designs with recently released GaN and SiC power devices, it is important to quantify the losses in the specific application or power-converter architecture. Also, trade-offs should be evaluated for devices that require different approaches for gate-drive circuitry, controller parameters, and system-performance goals.

Measuring the voltage waveforms on the drain, gate and source with sufficient accuracy and bandwidth is critical. It is also important to monitor these waveforms over temperature as wide-bandgap devices perform differently than Si devices. One key parameter of any switching FET is  $R_{DS(on)}$ . The  $R_{DS(on)}$  of Si FETs is known to approximately double from 25°C to 125°C. SiC devices have much less increase in  $R_{DS(on)}$  and are specified to operate to 200°C or higher. GaN FETs also have temperature dependence, as well as an OFF-state, voltage-dependent on-resistance mechanism called dynamic  $R_{DS(on)}$ . Si or SiC FETs have not been shown to have this complex effect. GaN's dynamic  $R_{DS(on)}$  has been reported to change as soon as several hundred nanoseconds after turn on to several minutes, depending on the cause of the change<sup>[2]</sup>.

Figure 2 shows a simple power-factor correction (PFC) boost topology<sup>[3]</sup>. For universal 85- to 270-VAC applications, the drain signal on Q1 can be as high as 400 V or higher with line surges. In the case of a GaN FET-based design, the OFF-to-ON waveform can have a  $dv/dt$  of >150 V/ns, and a fall time of approximately 3.5 ns. The simple relationship of signal bandwidth (BW) =  $0.35/t_{fall}$  gives an estimate of 100 MHz. To achieve less than 2%

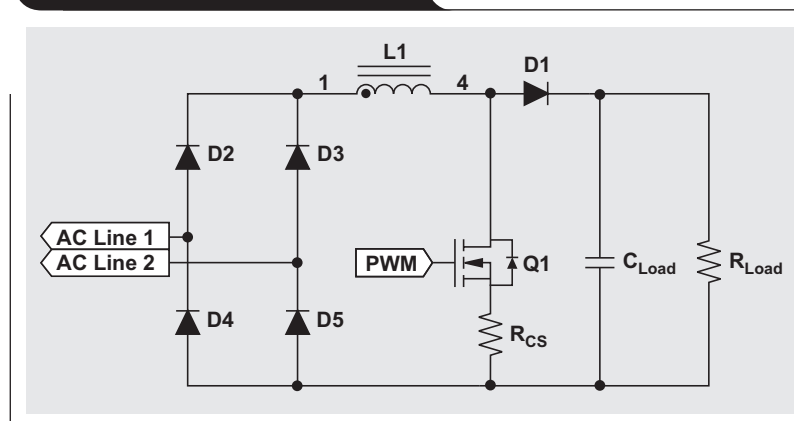
measurement error, the probe network and signal chain should have a bandwidth of 5 times this, or 500 MHz.

Referring back to Figure 1, note that without the compensation capacitor (C7), the 9-M $\Omega$  probe-tip resistance in front of the approximately 50 pF of cable capacitance that is in parallel with the 16 pF of scope input capacitance forms a low-pass filter with a bandwidth of only about 250 Hz, which is two million times lower than needed. To compensate, C7 in parallel with the 9-M $\Omega$  resistance is tuned to add a zero in the frequency response. This action cancels out the pole and provides a flat frequency response.

Another way to look at this is that C7 maintains the 9-times impedance ratio of the probe tip to the impedance of the cable and scope input across a wide bandwidth, until parasitic inductance and transmission line effects start to dominate. Unfortunately, 9 times the ratio of impedances means that there will never be an impedance match between the probe tip and the scope input. If you try to build this circuit, as I did, using off-the-shelf 50- $\Omega$  coax as the cable, it will perform very poorly. What comes into play, at approximately  $1/(\text{round-trip travel time})$  along the cable, is a very strong reflection or ringing due to the 9-times impedance mismatch.

A little research on my part, including tearing open an old probe and doing some old school reverse engineering, revealed a secret, which is the basis for my first tip and trick. The center conductor of the scope probe cable is resistive. I measured about 300  $\Omega$  between the output of the tip and the input to the Bayonet Neill-Concelman (BNC) adapter box, where the compensation is actually done. Like magic, adding loss to the path between the tip and the scope attenuates reflections and gives a flat response. I later discovered that this was patented by Tektronix in 1956<sup>[4]</sup>. Since patent lifetimes are about 20 years, this one has long since expired and is freely open for reuse.

Figure 2. PFC boost converter



### Back to circuit loading

At 500 MHz, without the lossy transmission line, the input impedance of the cable at the output of the probe is only about 5 Ω. As described in the patent, adding loss increases the cable input impedance and allows for a smaller value of probe-tip capacitance for compensation. Adjusting the compensation capacitor to be approximately 7 pF gives the probe an impedance of about 45 Ω at the tip that is used to touch the circuit. Such a low probe impedance could degrade a voltage measurement from a signal with greater than a few ohms of series impedance due to loading.

GaN FETs, like Si FETs, exhibit a  $C_{oss}$  that is a function of drain voltage, but are typically two-to-four times lower than Si FETs. One commercially available 600-V, 150-mΩ GaN FET reports a  $C_{oss}$  of approximately 40 pF at 400 V, and a commercially available 600-V, 190-mΩ Si super-junction FET reports a  $C_{oss}$  of 100 pF at 100 V, similar to a 1200-V SiC FET at 100 V.

The 7-pF capacitance of the probe tip, without loss in the line in the simple probe shown Figure 1, should be reduced to 1 pF or less to provide minimal signal loading for GaN and SiC FET testing.

### Reduce probe capacitance

Reducing capacitance can be accomplished in multiple ways. One trick is to use twinax cables and actively drive the shield for lower-frequency signals. Another option is to reduce the length of the cable as much as possible and then adding an active low-capacitance, wideband amplifier with high input impedance. In order to use an active amplifier and still maintain the capability for high-voltage measurement, adding a wideband, low-capacitance voltage attenuator is also required. The VCA824 from Texas Instruments is an example of a wideband, fully-differential

amplifier with high input impedance that can drive 50-Ω lines. It has an input common-mode range of ±1.5 V and a >700-MHz small-signal bandwidth, as well as an input impedance of 1 pF in parallel with 1 MΩ. Using this amplifier for drain voltages as high as 600 V will require a 1000:1 voltage attenuator that is flat from DC to >500 MHz and an input capacitance of less than 2 pF.

The impedance and power dissipation of this attenuator needs to be taken into consideration. Here are the competing requirements. Ideally, the impedance will be high enough to prevent overloading the circuit and reduce power dissipation. Implementing the attenuator with a 1-MΩ resistive impedance keeps the power dissipation to less than 400 mW when probing up to 600 V. Keeping the impedance lower gives a wider bandwidth while driving the parasitic board capacitance and amplifier's input capacitance.

Figure 3 shows an improved probe circuit that provides a 1000:1 divide ratio and only takes about 1 inch of signal-path length. The free on-line trace-impedance calculator tool<sup>[5]</sup> provided an estimate of the parasitic capacitance. For example, a 1-oz microstrip line, 6-mils wide and 4 mils above a ground plane with FR-4 (er 4.0), is about 2.7 pF per inch. To further reduce parasitic capacitance from the resistor dividers, an RF engineering trick was used to mount the 2-W-capable, 2512 SMT resistors on their sides. This minimizes the area of the signal-path conduction over ground. Also, the 1000:1 divide ratio was broken into two sections: 2:1 and 500:1. The input capacitance of this embedded probe is approximately 1.5 pF.

The 200 kΩ of DC resistance ( $R2 + R3$ ) results in a fairly high power dissipation, 1.8 W at 600 V, but allowed using approximately 1-pF compensation capacitance and get over 500 MHz of frequency response.

Figure 3. Schematic of improved high-voltage probe

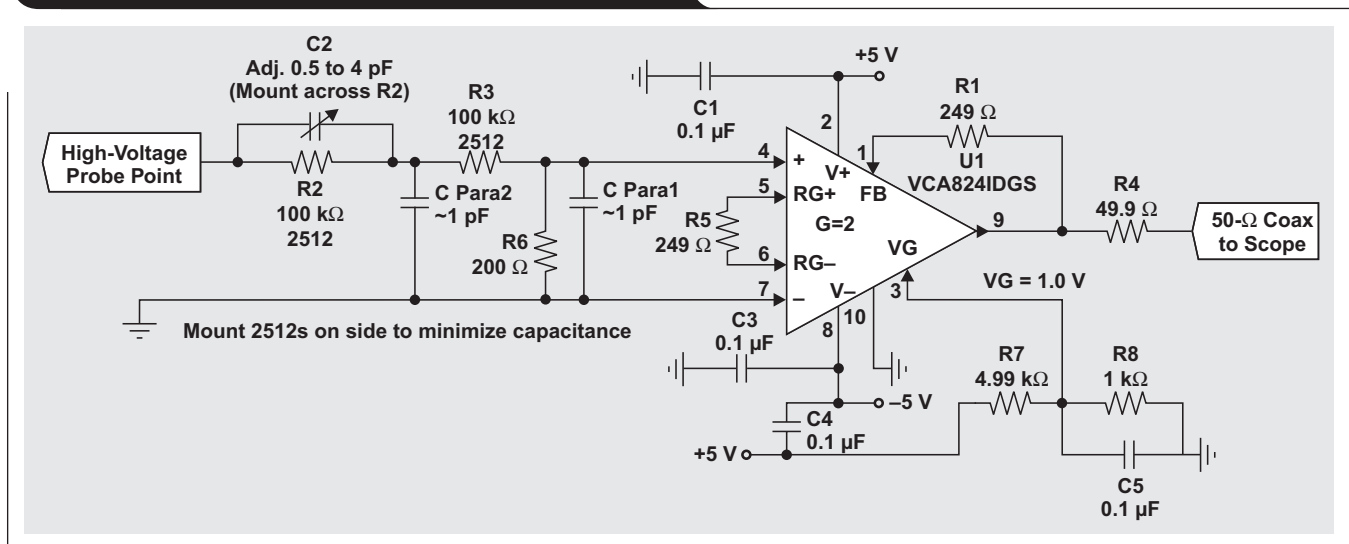
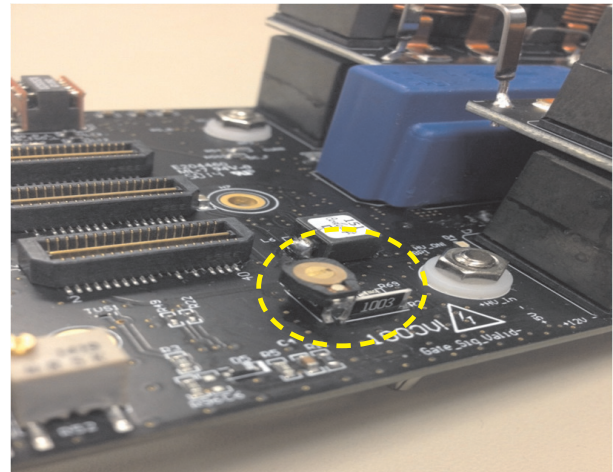


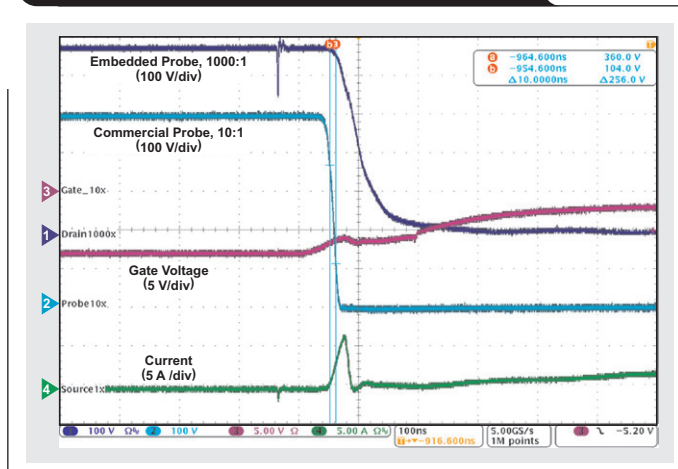
Figure 4 shows the circuit board with the side-mounted 2512's and the tuning cap in parallel.

Performance results are shown by two plots of the drain voltage output to the scope in Figures 5 and 6. The blue plot is from a 10:1 commercial scope probe. The purple plot is from a network that is buffered by the VCA824 and another TI wideband mux, the OPA4872, which is driving 10 feet of 50-Ω coaxial cable. The plot in Figure 5 is before tuning and the plot in Figure 6 is after tuning.

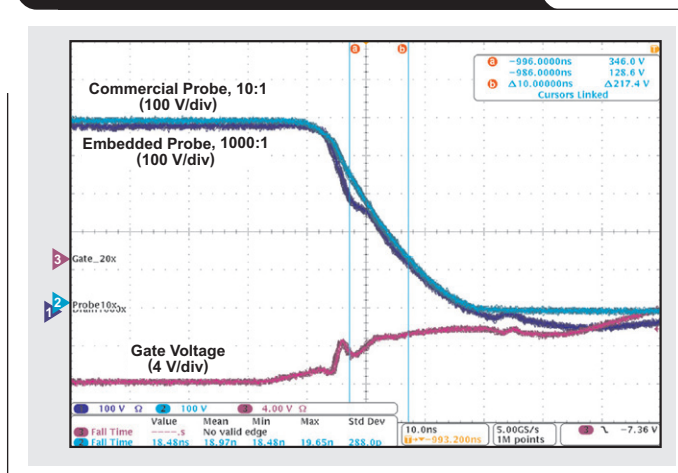
**Figure 4. Embedded high-voltage probe implementation**



**Figure 5. Comparison of probes before compensation/tuning**



**Figure 6. Comparison of probes after tuning compensation cap**



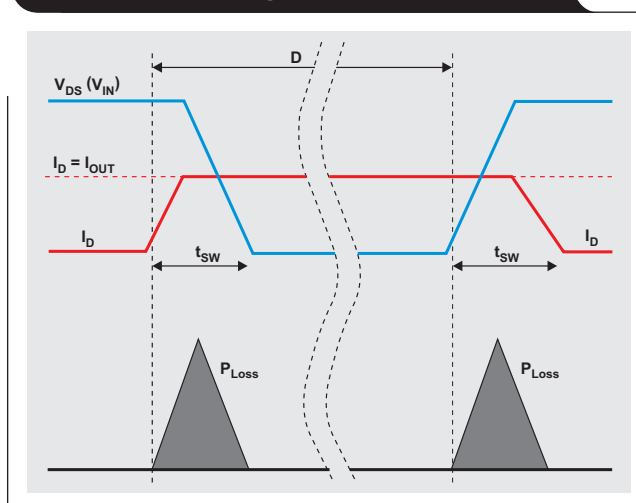
After compensation, the waveform from the embedded probe on the drain was used to estimate switching losses. Figure 7 shows how the turn-on and turn-off losses can be calculated. The total loss per cycle is the area under both triangular VI curves. To reduce measurement error, it is important to have good voltage accuracy as well as good current accuracy and skew matching (<2 ns) between both the voltage and current waveforms.

To accurately measure device current, another VCA824 amplifier was used to differentially measure the (Kelvin-connected) voltage across a current-sense resistor,  $R_{CS}$ , between the FET source and ground. Using a wide-body 6432, low-inductance (<200 pH) resistor with a value of  $0.100\ \Omega$  provided a current-measurement range of  $\pm 15\ \text{A}$ . The green trace in Figure 5 shows the source-current waveform derived from the differential voltage measurement multiplied by 10. Note that the triangular 6-A current spike at FET turn on is due to the device's gate and drain charge. Figure 5 also shows the gate-to-ground waveform as the red trace. Skew matching was accomplished by using equal-length routes from the device to the buffer amps and then equal-length runs of  $50\text{-}\Omega$  coax to the scope.

## Conclusion

In summary, it was shown how an easy-to-implement, embedded-probe circuit can measure voltages up to 600 V, with rise and fall times as short as 3.5 ns. To minimize capacitive loading, a 1-inch  $50\text{-}\Omega$  microstrip line, along with two  $100\text{-k}\Omega$ , 2-W resistors and one  $200\text{-}\Omega$  resistor to ground, is used to implement a wideband 1000:1 attenuator. This configuration drives the fully-differential VCA824 amplifier that offers high input impedance, a >700-MHz bandwidth and a  $\pm 1.5\text{-V}$  input common-mode range. Also shown was how the device current can be measured with the differential VCA824 using a Kelvin connection across a  $0.1\text{-}\Omega$  resistance between the device's source and ground. With skew-matched voltage and current waveforms, a designer can use the oscilloscope's waveform math to multiply and integrate them to provide accurate estimates of device losses.

**Figure 7. Switching power-loss estimation**



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2. Donghyun Jin and Jesús A. del Alamo, "Mechanisms responsible for dynamic ON-resistance in GaN high-voltage HEMTs," Proceedings of the 2012 24th International Symposium on Power Semiconductor Devices and ICs, June 2012.
3. "A 300-W, Universal Input, Isolated PFC Power Supply for LCD TV Applications," *Reference Design*, Texas Instruments.
4. Electrical probe US 2883619 A, US Patents.
5. Microstrip Impedance Calculator, Multi-Teknik.

## Related Web sites

Gallium Nitride (GaN) Solutions:

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