How to improve PFC light-load efficiency

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Introduction

Although the efficiency of power supplies has improved significantly, most efforts focus on improving efficiency at medium to heavy loads. However, light-load efficiency is becoming more and more important. For example, the 80-Plus Titanium efficiency standards not only require 96% efficiency at a 50% load, but 90% efficiency at a 10% load and 94% efficiency at a 20% load.

Maintaining high efficiency at light-load conditions is extremely important in most electronic and electrical appliances, where the digital loads spend the majority of their time in idle mode. Servers or applications that require highly-reliable power sources will employ a redundant power-supply system that is comprised of two (or more) power-supply units. Each power supply works at a light load most of the time; therefore, light-load efficiency is more meaningful than heavy-load efficiency.

This article describes how to improve the light-load efficiency of an AC/DC power supply with a power factor correction (PFC) front end. This front-end stage, hereafter referred to as the PFC, forces the input current to follow the input voltage such that the electronic load appears to be a pure resistor. A PFC is required for ≥75-W power supplies.

Reducing the switching frequency and bulk voltage at light loads

Power loss in a PFC consists of switching losses, gate-driving losses, conduction losses, magnetic core losses and diode reverse-recovery losses. Conduction losses, magnetic core losses and diode reverse-recovery losses are related to power-stage materials. Switching losses and gate-driving losses are proportional to the switching frequency, as shown in Equations 1 and 2:

$$P_{SW\_LOSS} = 0.5 \quad V_{OUT} \quad I_L \quad (t_R + t_F) \quad f_S \qquad (1)$$

$$P_{GATE\_LOSS} = Q_{GATE} \quad V_{GATE} \quad f_S \qquad (2)$$

where f_S is the switching frequency, t_R is the rise time and t_F is the fall time.

Reducing the switching frequency at light loads reduces both switching losses and gate-driving losses and thus improves efficiency.

Equation 1 also shows that switching losses are proportional to the PFC output voltage. Thus, reducing the bulk voltage can also increase efficiency—including the subsequent DC/DC converter efficiency. In some cases, it's possible to configure the PFC as a voltage follower where the output follows the input. V_{OUT} is high at high line and a much lower value at low line, as long as it is still higher than the input-voltage peak and within the operational range of the subsequent DC/DC converter.

In applications with a required holdup time, the energy stored in the bulk capacitor is proportional to the bulk voltage. But because reducing the bulk voltage will reduce the holdup time, reducing the bulk voltage is not applicable in such cases.

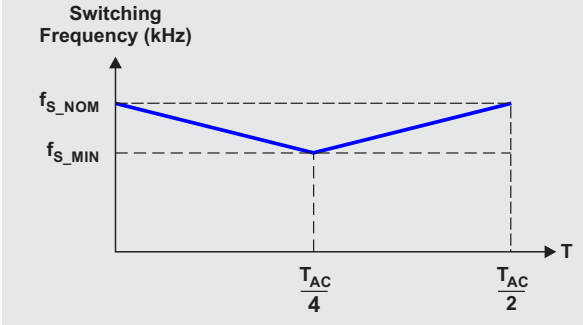
Dither switching frequency within an AC half cycle

Although reducing the switching frequency is a simple and effective way to improve efficiency, it may cause the PFC to enter discontinuous conduction mode (DCM). In DCM, the current-loop bandwidth drops significantly, and the inductor current no longer follows the current reference very well. Since the current is discontinuous, a single sample—no matter where it is in the switching period—does not equal the average current. When it is used as a current feedback signal in an average current-mode-controlled PFC, the PFC input current will be a distorted sine wave. DCM operation can also cause current spikes[1] and affect total harmonic distortion (THD).

To improve efficiency without entering DCM, consider a frequency-dithering approach. When reducing the switching frequency, the AC zero-crossing region always enters DCM first; the AC peak region is the last to enter DCM. Knowing this, let the PFC operate at its nominal switching frequency at the AC zero-crossing. Then the switching frequency is gradually decreased until the AC voltage reaches its peak; and from there, the switching frequency is gradually increased. The switching frequency will return to nominal when the AC voltage reaches the zero-crossing again.

Figure 1 shows the switching frequency profile in an AC half cycle. The minimum switching frequency is selected such that the PFC is still in continuous conduction mode (CCM). The reduced switching frequency reduces the switching and gate-driving losses, thus improving efficiency. Because the PFC remains in CCM, there will be no THD issues caused by DCM.

Figure 1. Dither switching frequency in an AC half cycle

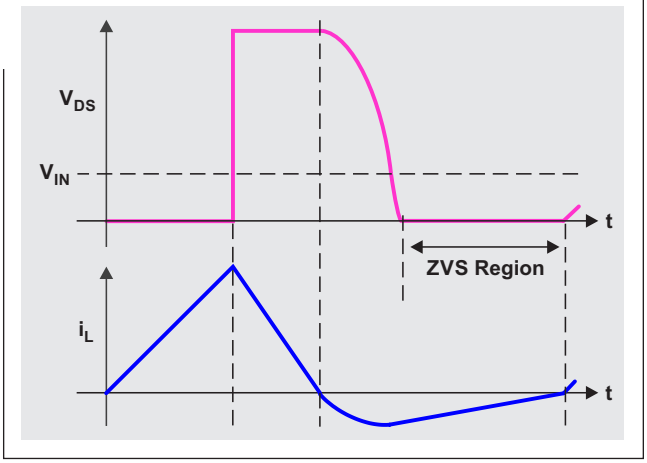


The frequency dithering is not the same as the widely used spread-spectrum frequency dithering technique to reduce electromagnetic interference (EMI) noise. In that technique, the switching frequency is swept back and forth around the nominal value. Because the average switching frequency does not change, the average efficiency is not improved.

Multimode control with zero-voltage switching

At light loads, a CCM PFC may enter DCM. In DCM, when the metal-oxide semiconductor field-effect transistor (MOSFET) turns off, the boost inductor current starts to decrease. Once the boost inductor current declines to zero, the boost inductor resonates with the PFC MOSFET parasitic capacitance. If the instantaneous AC voltage is lower than one-half the PFC output voltage, the MOSFET's V_{DS} can resonate to 0 V and be clamped by the MOSFET body diode. Turning the MOSFET on at that moment will achieve zero-voltage switching (ZVS), as shown in Figure 2.

Figure 2. ZVS control at light loads



Since the MOSFET turns on when the inductor current reduces to zero, the PFC now works as if it is in critical conduction mode (CrM). The switching frequency is not constant any more—it increases. ZVS significantly reduces switching losses and improves efficiency.

ZVS is achievable when the line is low. At a high line voltage, however, when the instantaneous AC voltage is higher than one-half the PFC output voltage, the MOSFET's V_{DS} will never resonate to 0 V—ZVS is not possible. In this case, the MOSFET can be controlled so that it will turn on when V_{DS} resonates to the valley, also known as valley switching. Valley switching has fewer switching losses compared to hard switching; thus, it also helps improve efficiency. When the load increases to a medium or heavy load, the PFC goes back to CCM with a constant switching frequency. This control method is called multimode control.[1]

If the PFC has a totem-pole PFC structure, the ZVS CrM control can be extended to the whole input voltage range. An instantaneous AC voltage that is lower than one-half the PFC output voltage will achieve natural ZVS, as explained above. When the instantaneous AC voltage is higher than one-half the PFC output voltage, the turn-on time of the synchronous switch is extended for a short period after the inductor current declines to zero, which generates a small amount of negative inductor current. Once the synchronous switch turns off, the voltage on the switch node will discharge to zero because of this negative current. Turning the main switch on at this moment achieves ZVS.[2]

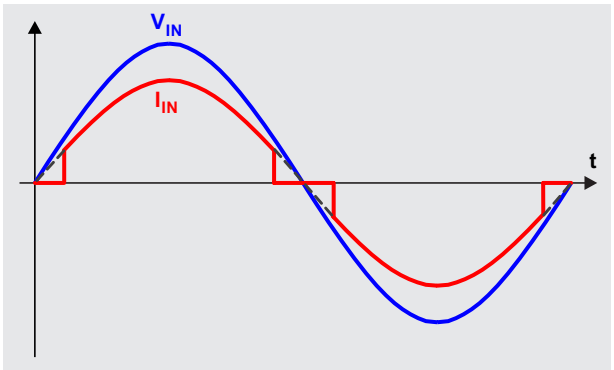
PFC turnoff at the AC zero-crossing area

The current waveform of a well-controlled PFC is a sinusoidal wave. Its magnitude is very small at the AC zero-crossing area, which means that very little power is delivered to the load in this region. Disabling the PFC operation during this region has very little effect on PFC power delivery; thus, the bulk voltage ripple will hardly change. Although very little power is delivered in this region, the switching and gate-driving losses still exist; therefore, it is not worth turning on the PFC.

To improve light-load efficiency, turn off the PFC during the AC zero-crossing area. The current waveform will look like Figure 3. The larger the AC zero-crossing region when turning the PFC off, the higher efficiency that can be achieved.

The current waveform in Figure 3 shows the flat region at the AC zero-crossing area, which will affect THD. However, since the majority of the waveform is still maintained as sinusoidal, the THD is not too bad. This method is effective for applications where THD is not very critical at light loads, or has a big margin. The greater the THD margin, the longer the period at the AC zero-crossing area where the PFC can be turned off, and the higher efficiency can be achieved.

Figure 3. Turning off the PFC at the AC zero-crossing area



Phase shedding for multiphase PFC systems

A well-known power-saving method for multiphase PFC systems is called phase shedding. At light loads, there is no need to run all of the phases; turning off one phase will still provide enough power to the load. In the meantime, all switching and driving losses drop to zero when that phase is off, thus improving overall system efficiency.

Alternative operation for redundant power systems

In a redundant power system, a few power supply units run in parallel to provide power to the load, with each unit providing a portion of the total load. Figure 4 shows a 1+1 redundant system where each power supply is capable of powering the entire load. If one fails, the other power supply must provide all of the power. The transition should be seamless so as not to interrupt the normal use of the load. This requires keeping both units on all the time, making the phase shedding method inapplicable.

Now consider a different approach for "both units on all the time." Each power-supply unit includes a PFC and a DC/DC converter. Keeping all of the units on means that each DC/DC converter needs to be on all the time—but not necessarily the PFC. The PFC can occasionally be off as long as the bulk voltage does not trigger the DC/DC converter brownout protection. Thus, an alternative operation mode can be used for redundant power systems during light loads.

Assuming that the redundant power system is a 1+1 system, during light loads, the PFC of the first power-supply unit only turns on during a positive AC cycle and the PFC of the second power-supply unit only turns on during a negative AC cycle, as shown in Figure 5. Both DC/DC converters are always on, regardless of load level. Since each PFC only operates at an AC half cycle, the switching and driving losses drop by half, improving overall efficiency. Although the input current for each unit is a half sine wave, the total AC input current is a whole sine wave and THD is not affected.

It's possible to extend this method to N+N redundant power systems. By letting N units' PFCs only turn on during a positive AC cycle and other N units' PFCs only turn on during a negative AC cycle; all of the DC/DC converters are always on. The total input current is a whole sine wave with balanced magnitude on the positive and negative AC cycles.

Burst mode

When a PFC operates at extreme light loads or in standby mode, low THD is usually not a requirement. To improve efficiency, the PFC can operate in burst mode, turning on and off for short periods. Since the load is very small, alternating turn-on and turn-off won't increase the bulk voltage ripple much; therefore, it won't affect the subsequent DC/DC converter operation. Among all different burst methods, an AC cycle-skipping burst mode[3] not only improves efficiency, but also maintains low THD and good power factor during bursts.

Figure 4. 1+1 redundant power system

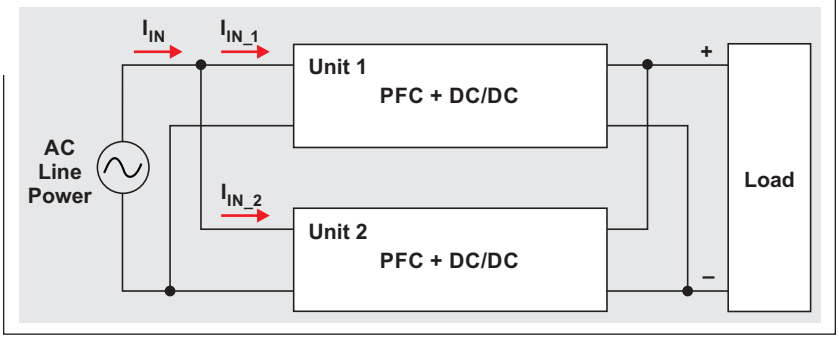
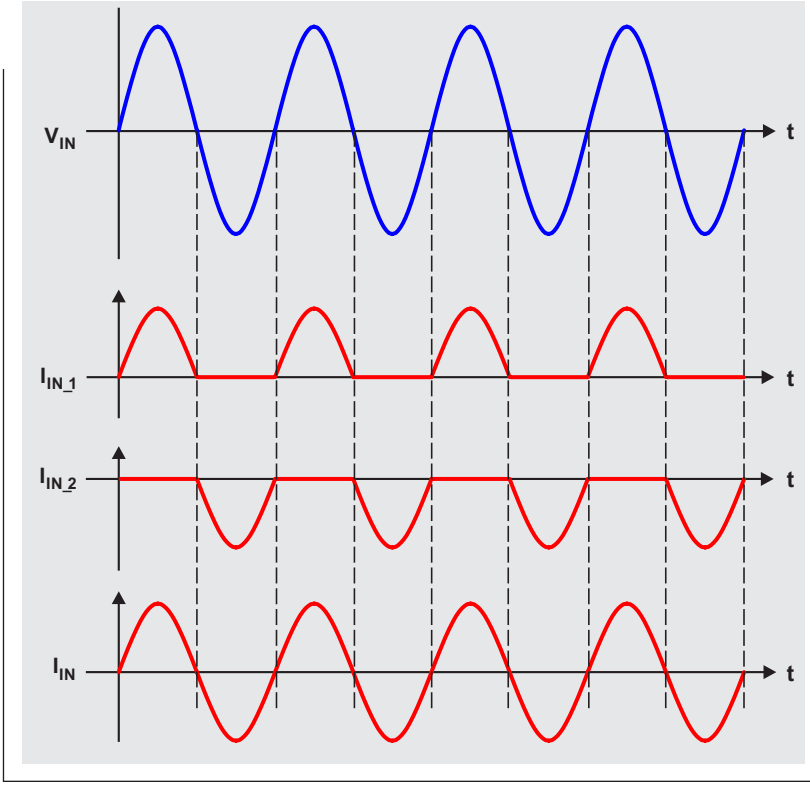


Figure 5. Current waveform for a 1+1 redundant power system at light loads



Conclusion

PFC light-load efficiency can be improved by special control methods discussed in this article. These methods can also be combined to achieve even better efficiency. All of the methods discussed in this article are easily implemented with a digital controller like the Texas Instruments UCD3138. Many of the methods can also be integrated into analog PFC controllers.

References

1. Bosheng Sun and Zhong Ye, "PFC THD Reduction and Efficiency Improvement by ZVS or Valley Switching," TI application report (SLUA644), April 2012.
2. Bin Su, Junming Zhang and Zhengyu Lu, "Totem-Pole Boost Bridgeless PFC Rectifier with Simple Zero-Current Detection and Full-Range ZVS Operating at the Boundary of DCM/CCM," IEEE Transactions on Power Electronics 26(2): February 2011.
3. Bosheng Sun, "AC cycle skipping improves PFC light-load efficiency," TI Analog Applications Journal (SLYT585), 3Q 2014.

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