Comparing Power-Supply Architectures for a 12-bit ADC

Powering any data converter, such as an analog-to-digital converter (ADC) or digital-to-analog converter (DAC), requires a clean, low-noise power supply. Traditionally, engineers used low-dropout (LDO) linear regulators because this topology introduces no switching noise onto the supply voltage. However, LDOs are the least-efficient power-supply type due to their linear operation.

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To overcome this, engineers added dc-dc step-down (buck) converters before the LDOs to increase the conversion efficiency. This architecture adds extra semiconductor devices and passive components, and increases the total power supply cost.

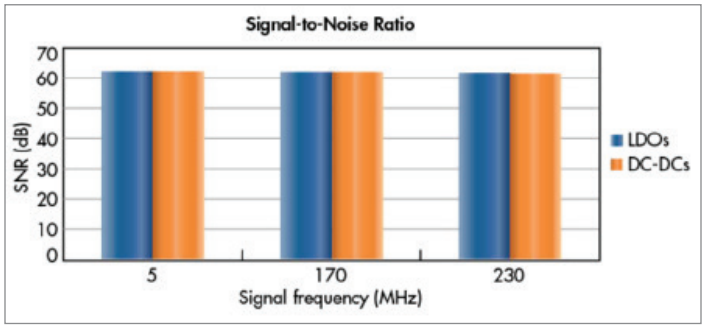
While noisier than LDOs, many modern dc-dc converters do have low-enough noise as to not decrease the data converter's performance. A dc-dc converter-only design, not using any LDOs, is shown to power a 12-bit ADC without losing any performance. The article compares its noise performance, efficiency, power loss, and cost against the other two power-supply architectures.

Powering the ADS5407

Texas Instruments' ADS5407 is a 12-bit ADC used for applications such as test and measurement and data acquisition.[1] It requires a 3.3-V analog supply with 239 mA of current, as well as a 1.8-V supply with 418 mA of current for the analog, digital, and clock domains. Typical input voltage is 5 V in many industrial systems. These three voltages allow LDOs, step-down dc-dc converters, or both to be used to power this ADC.

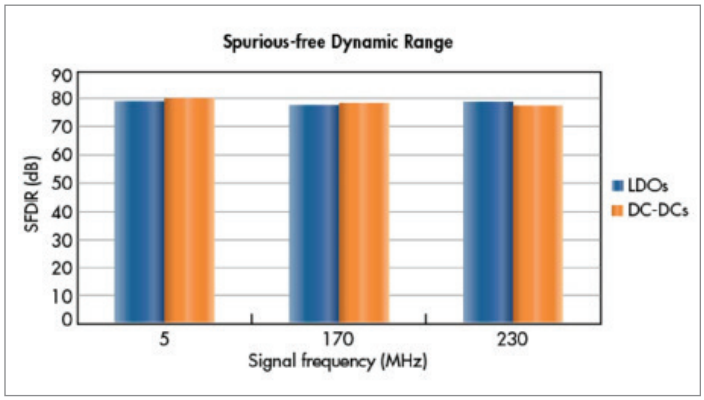
The Linear-Regulator Approach

Two LDOs are required to convert the 5-V input voltage to the 3.3- and 1.8-V voltages. The simplified efficiency of any LDO is VOUT/VIN. And the simplified power loss in any LDO is the voltage across the LDO multiplied by the current. Therefore, the 3.3-V LDO's efficiency is 66% with 406 mW of power loss, and the 1.8-V LDO's efficiency is 36% with 1.34 W of power loss. Overall, 47% efficiency with 1.746 W of total loss is achieved.



The LDOs provide acceptable noise performance for the ADC and serve as the baseline case for comparison. LDOs are usually the lowest-cost solution for a 12-bit data converter due to the low device cost, as well as low number and cost of passive components. Higher-resolution data converters typically require much-higher-performance LDOs, which are more expensive.

The low level of efficiency limits the run time for battery-powered equipment, while the total power loss poses thermal challenges in equipment with higher ambient temperatures or smaller sizes. However, the low cost enables low-end applications, which aren't concerned with efficiency or temperature rise, and applications that don't utilize the full capabilities of the ADC (and thus have lower power consumption).



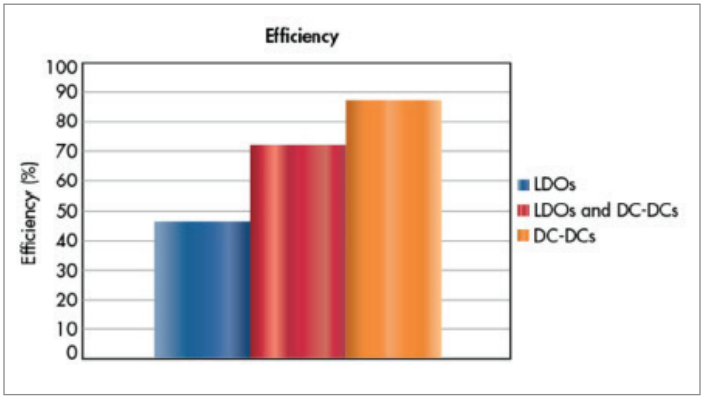
The Linear-Regulator + Step-Down DC-DC Approach

Step-down dc-dc converters are added to increase efficiency, while LDOs are placed after them to filter out the switching noise created. Typically, 0.5 V of headroom above the output voltage is required at the LDO's input to provide sufficient noise rejection. Therefore, the voltage across each LDO is 0.5 V. Less headroom may be used, but then the noise performance may not be sufficient for the ADC. Assuming 85% efficiency for the 2.3-V dc-dc, 90% efficiency for the 3.8-V dc-dc, the combined efficiency is 72% and power loss is 599 mW.

Since LDOs are used after the dc-dc converters with sufficient voltage headroom, the noise performance is the same as the LDO case. This architecture is the most costly, because it requires the most power-supply devices and associated passive components. The added cost enables a decent overall efficiency for portable equipment with a manageable power loss.

The Step-Down DC-DC Approach

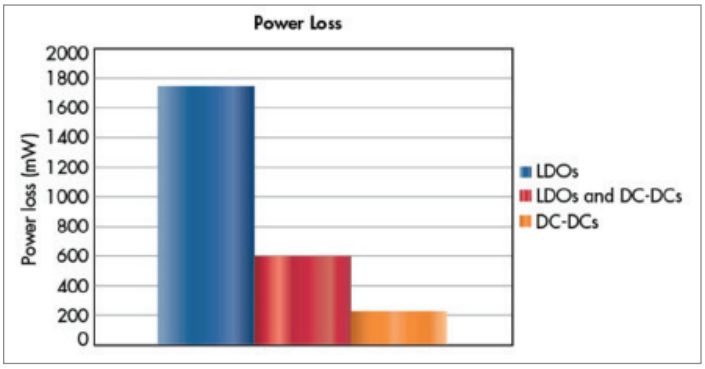
The most efficient solution is to use just dc-dc converters and no LDOs. Using the same 85% efficiency estimate for the 1.8-V rail and 90% efficiency for the 3.3-V rail, overall efficiency is 88%. This corresponds to a power loss of just 220 mW.



Modern, low-noise dc-dc converters can power data converters with no reduction in performance.[2] This requires specific testing, which adds a minimal amount of development time. **Figures 1** and **2** show the signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) test results for the two LDO architectures, LDOs only and LDOs plus dc-dcs, and the dc-dc-only architecture. Three different input signal frequencies are tested in order to validate a wide range of ADS5407 operation.

The minimal difference in measured results shows that the tested dc-dc converters, the TPS62231 and TPS62237, don't reduce the ADC's performance. In these tests, the circuitry after the power supply, ferrite beads, and decoupling capacitors remained the same for each configuration. This portion of the test setup is a control variable in order to evaluate changing a single variable—the power-supply type.

Figures 3 and **4** compare the efficiency and power loss, respectively, of the three different architectures. Using only dc-dcs decreases the power loss by over 85%. This greatly reduces thermal challenges in the end equipment, which might otherwise require expensive heat sinks and so on.



Using just dc-dc converters is sometimes more expensive than using just LDOs, due to the generally higher device cost and additional passives that are required. This depends on the exact LDO and dc-dc required by the specific data converter.

However, the higher efficiency and corresponding lower power loss may save cost in other areas. For example, dc-dc converters generally don't require heat sinks and allow for a lower-power—and thus lower-cost—5-V input power supply to be used due to their reduced power consumption.

Conclusion

The table shows a comparison of the noise performance, efficiency, power loss, and cost for three power-supply architectures. When some basic testing is possible, the dc-dc-only architecture shows the best overall performance except in those designs that require absolute lowest cost.

OVERALL COMPARISON OF DIFFERENT POWER-SUPPLY ARCHITECTURES

Architecture	Noise performance	Efficiency	Power loss	Cost
LDOs	Sufficient	Poor	High	Low
LDOs and DC-DCs	Sufficient	Average	Average	High
DC-DCs	Sufficient*	Good	Low	Low-medium

*with basic testing

References

1. Product folders: ADS5407, TPS62231, TPS62237

2. TI Design: http://www.ti.com/tool/pmp9767

3. Source URL: http://electronicdesign.com/analog/comparing- power-supply-architectures-12-bit-adc

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