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A New Approach to Validate GaN FET Reliability to Power-line Surges Under Use-conditions

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***Abstract*— The robustness of FETs to power-line surges has a tremendous impact on field reliability and is an important consideration for the adoption of new technologies like GaN. The methodology for silicon FETs, however, is not suitable for GaN because of the low avalanching energy capability of present-day GaN FETs. However, GaN FETs have better transient overvoltage capability than Si FETs, providing the ability to operate through surge without avalanching. This paper defines, for the first time, a methodology for the surge rating of GaN FETs using their superior transient overvoltage capability. It leads to a device-level surge parametric specification, an important consideration for the design of surge-robust power supplies using GaN. GaN FETs are shown to be robust to power line surges under actual operating conditions for the first time. This seminal work results in a comprehensive methodology for surge-robust power supply design with GaN.**

***Index Terms*—power system reliability, semiconductor device reliability, surges, gallium nitride, power system transients**

I. INTRODUCTION

Power distribution systems are affected by both environmental and equipment-related events that cause transient over-voltages or line-surge conditions. The ability of devices to withstand such surges is important since it has a significant impact on field-reliability [1]. In traditional power supply applications like power factor correction (PFC) circuits, much of the line surge is attenuated by other components, like spark gaps, metal-oxide varistors (MOV's), EMI filters, and bus capacitances. The residual surge energy reaching the power FET is dissipated by means of avalanche, making the avalanche rating of the device important.

The traditional paradigm, however, is based upon the properties of silicon power MOSFETs. These FETs do not have much headroom above their maximum voltage rating. As a result, when a power line surge strikes, the FET breaks down by the impact-ionization phenomena, or *avalanche breakdown*. Over the years, the industry has engineered the FETs to do this robustly, and the avalanche rating has become associated with power-line surge protection.

GaN has avalanche capability [2] but the FETs are presently not avalanche robust. The current GaN device structure does not support high avalanche energy. An avalanching capability is not necessary for surge robustness if the FETs can withstand the surge voltage. GaN FETs are built with considerable transient overvoltage capability, and should be able to operate through surge *without avalanching*. The validation of this property is important for the reliable field-operation of GaN-FET power stages.

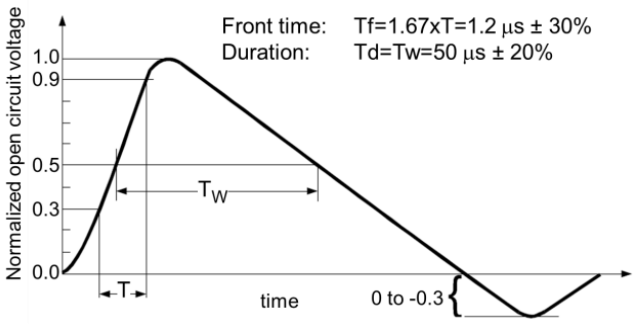

Fig. 1: IEC 61000-4-5 standard CWG 1.2/50 μs open-circuit surge waveform shape to simulate a line disturbance. The front time is 1.2 μs, and duration (above 50% of the peak value) is 50 μs.

II. BACKGROUND

Power line surges are caused by lightning strikes, load switching, capacitor bank switching, equipment faults etc. [1], [3] The methodology for surge testing is well developed and is described by the IEC 61000-4-5 standard [4], which specifies the surge generator output into both open and short circuits. The open-circuit voltage-surge waveform shown in Fig. 1 is called the (combination wave generator) CWG 1.2/50 μs waveform. Another aspect is the number of surge strikes needed for the test. The VDE 0884-11 [5] standard specifies the application of 50 surge strikes, of which 25 are of polarity one, followed by 25 of polarity two.

GaN FETs are known to possess transient overvoltage capability, as seen by several manufacturers' datasheets. For example, 600V-class FETs have transient drain-source voltage ratings, $V_{DS(TR)}$, of 750-800 V [6]-[8]. A question often asked is whether $V_{DS(TR)}$ is a surge rating, and if not, what is it? It is important to understand converter operation in order to answer this question.

The $V_{DS(TR)}$ test is conducted with the device off, and is a test to validate FET reliability to drain-voltage ringing at turn-off, such as caused by parasitic inductance [9]. In soft-switched topologies, the main FET is off at high drain voltages, so the rating may apply if the soft-switching operation is maintained through surge. This is yet to be proven, though. Hard-switching, however, is more stressful than soft-switching [10]-[12]. During surge, there will be many hard-switching cycles at elevated voltage, since the surge waveform lasts for over 100 μs. It is also likely for the switching current to increase during the surge strike. In addition, the FET is also powering a load. This additional device stress needs to be considered in a surge rating. Many GaN applications like PFC's, inverters, motor drives and

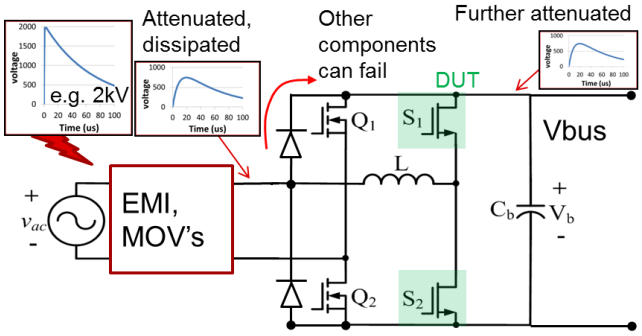

Fig. 2: Schematic of a PFC stage, showing the attenuation of the waveform and the system-dependence of the surge voltage reaching the device.

buck/boost converters are hard-switched, making hard-switched surge validation very relevant.

III. Test Design Considerations

Traditional surge-testing for silicon-based power supply applications involves firing surge strikes at specified voltages from 0.5 kV up to 4 kV, depending upon the desired rating level [4], [13]. The power supply is typically designed with surge protection components like spark gaps and MOV's that attenuate and dissipate the surge strike. In addition, other components like EMI filters and power-supply capacitances further attenuate the surge voltage. The residual surge waveform reaching the FET is thereby power supply design dependent. In addition, the surge strike can cause system-level failures by stressing other components like bypass diodes and capacitors. The aspects above are illustrated in Fig. 2, which shows a schematic of a PFC stage.

Fig. 2 illustrates an important consideration. Every company will have a different system-level approach to power supply design and surge mitigation. Since the traditional test specifies the surge voltage at the generator, the voltage reaching the power FET will be system dependent. One is therefore unable to define the voltage at the FET. The ability to do so is important for a device-level surge-voltage parametric for GaN FETs. The parameter should allow the use of different voltage limiting components such as MOV's, EMI filters, bypass diodes, and bus capacitances to achieve a reliable surge solution for GaN FETs. It should also be readily usable in circuit simulation and enable a power supply engineer to design a reliable solution for surge.

The datasheet parameter needed, $V_{DS(SURGE)}$, is the drain-source voltage the GaN FET survives when actively switching the load current (not "OFF") during a surge strike. We arrived at a value of 720 V from system-level considerations and customer feedback. As shown in Fig. 3, $V_{DS(SURGE)}$ defines the maximum operating bus voltage during surge and $V_{DS(TR)}$ specifies headroom for ringing. For example, $V_{DS(TR)}$ for the LMG3410 GaN product is 800 V [6], giving 80 V headroom over the $V_{DS(SURGE)}$ rating.

IV. Test Circuit and Biasing

The selection of a suitable test-vehicle circuit is an important consideration. It needs to be simple and enable application of a defined surge voltage to the device under test (DUT), while minimizing the failure risk of other components. Our test-vehicle circuit is based upon a buck

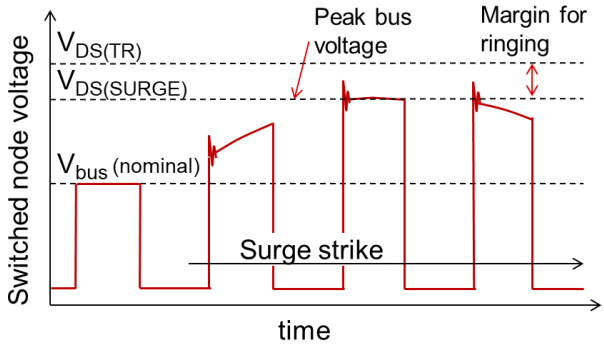

Fig. 3: Figure illustrating the two datasheet parametrics needed to fully surge-rate a device: $V_{DS(SURGE)}$, the maximum bus voltage allowable during surge, and $V_{DS(TR)}$, to specify additional headroom for ringing.

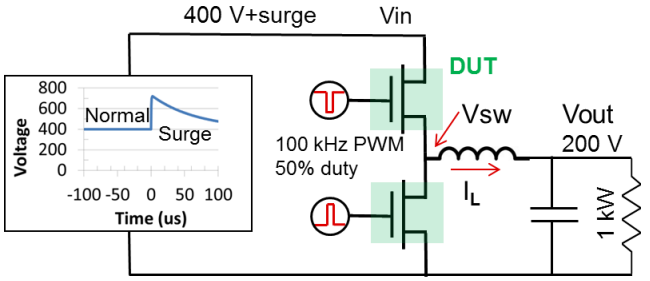

Fig. 4: Surge test-vehicle schematic topology. The circuit biases the device at a 400 V operating point and applies surges while the devices are actively running, in order to replicate the real operating condition of a surge.

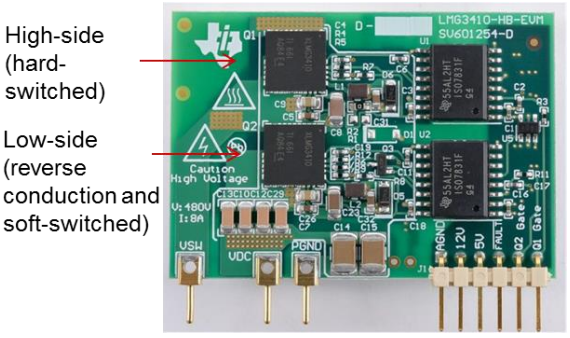

Fig. 5: TI-GaN EVM half-bridge card used for the device test. It plugs into the surge-tester motherboard. The use of a half-bridge allows surge testing for both polarities: hard-switching turn-on and reverse conduction.

converter. This allows a surge waveform with specified peak voltage to be applied directly to the DUT while switching as it does in the power supply. The circuit eliminates other failure-prone components e.g. bypass diodes, MOV etc. Additionally, by use of GaN DUTs for both high and low-side devices, surge-reliability is validated for both polarities of operation, i.e. hard-switching of the high-side and reverse-conduction of the low-side. The low-side device also sees soft-switched transitions. The schematic is shown in Fig. 4. The half-bridge uses the EVM card, shown in Fig. 5.

In order to implement a realistic stress, the half-bridge circuit was biased with 400 V input and switched at 100 kHz with 50% duty cycle. The slew rate was set to 50 V/ns for reasonable I-V overlap (hot-electron stress) by using the slew-rate control resistor, R_{DRV} [6]. The temperature was monitored by using thermocouples attached to the top of the

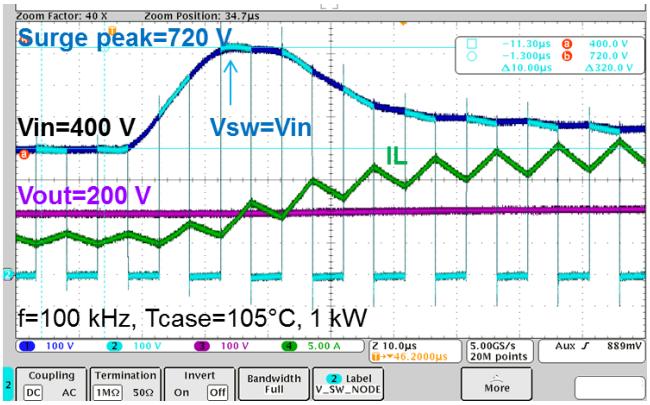

Fig. 6: Surge waveforms, showing the test-point parameters labeled in Fig. 4. The input bus voltage surges from the operating point of 400 V to the target spec of 720 V. The switched node waveform is overlaid on the input waveform to show the switching. It shows that the 720 V surge stress is applied directly to the GaN FETs while switching.

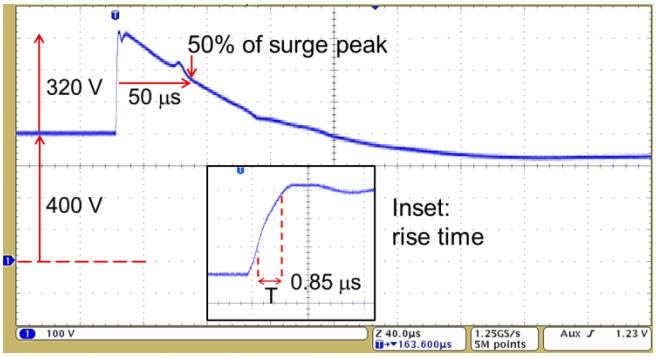

Fig. 7: Measurement of the open-circuit surge waveform for a 720 V peak output with 400 V DC component. The front time is 1.42 µs and duration is 50 µs, in accordance with the IEC 61000-4-5 definitions in Fig. 1.

device QFN cases and the temperature of the high-side device maintained at 105°C. The converter was loaded at 1 kW by configuring an e-load as a constant resistor.

The scope capture in Fig. 6 shows the system response to a surge event that provides a 720 V surge bus voltage. The waveforms correspond to the input and output parameters, V_{in}, V_{sw}, V_{out}, I_L as labelled in Fig. 4. The overlaying of both input bus voltage (V_{in}) and switched node voltages (V_{sw}) is a good visual to show the surge stress directly applied to the GaN devices. Fig. 6 shows that the switched node "high" voltage follows the input voltage, and confirms that the FETs are subject to a peak surge voltage of 720 V while switching.

The voltage surge also causes the inductor current to increase due to the increased V_{in} and the constant 50% duty cycle. The inductor value was chosen such that the current increased from about 5 A to 20 A. This also validates device robustness to a 400% transient current surge resulting from the voltage increase of the surge waveform.

The waveform reaching the DUTs is different from the CWG 1.2/50 µs shape shown in Fig. 1 due to loading by the circuit. The strike is according to the standard, since the shape is defined for the open circuit voltage and short circuit current waveforms of the surge generator [4], [13]. Our surge generator is calibrated, plus we additionally validated the

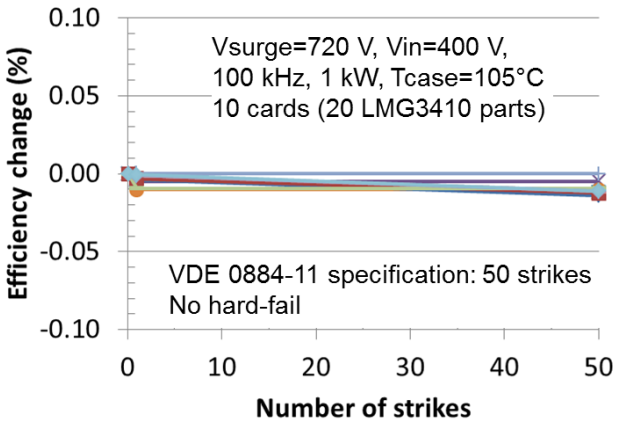

Fig. 8: The 50-strike surge test, validating that devices do not show efficiency degradation or hard-failure, and continue to power a 1 kW load.

shape of the surge waveform under open circuit generator conditions, as shown in Fig. 7. The figure shows a 320 V surge coupled with 400 V DC through a coupling-decoupling network (CDN), resulting in a peak surge voltage of 720 V. The surge waveform meets the specifications of front time and duration.

V. Surge Stress-test Results

The surge stress test consists of applying 50 strikes of the IEC61000-4-5 CWG 1.2/50 µs waveform to the running test circuit. There are two potential failure modes that could arise from the surge stress. First is an increase in dynamic $R_{DS(ON)}$, caused by an increased amount of electron trapping, driven by both the high voltage and high current hard-switching transitions. Second is device hard-failure from exceeding the device Safe Operating Area (SOA).

The results of the stress test on twenty devices (10 half-bridges) sampled from two production lots are shown in Fig. **8**. Half-bridge cards (Fig. 5) were run in the test-vehicle circuit of Fig. 4 using the test conditions of Fig. 6. The circuit was run with the surge coupled in through a CDN, such that the peak surge voltage at the device reaches 720 V with the operating bus voltage at 400 V DC. The surge-generator voltage setting was 435 V to account for loading. Efficiency measurements were done for the unstressed device, after one strike, and after the 50 strike test. The efficiency was calculated by dividing the output power by the input power, and referenced to the efficiency prior to stress. Surges were fired at two strikes per minute, and the system was stabilized for 30 mins before recording measurement values.

Fig. 8 shows that the efficiency is virtually unchanged after the 50-strike test, showing that dynamic $R_{DS(ON)}$ did not increase. In addition, none of the devices showed hard-failure. This is significant, because it demonstrates that GaN has superior transient overvoltage capability, which enables it to switch through surge. The ability to switch through surge allows well-defined operation during surge as compared with devices that avalanche.

VI. Surge-Robust Design with GaN

The surge-voltage specification, $V_{DS(SURGE)}$, makes it straightforward to design a robust power supply with GaN. This is because the schematic for a surge generator is

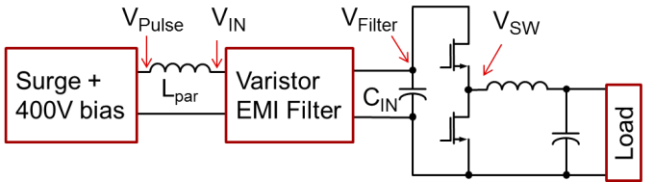

Fig. 9: Schematic of the buck converter used for simulation

specified in the standard [1], [4], [13], [14] and can be implemented in a simulator. This allows component values to be selected such that the bus voltage at the device remains below 720 V during surge. As an example, we show the simulation results for a buck converter (Fig. 9).

The circuit was simulated by setting the generator to an open-circuit voltage of 4 kV. This is the highest defined voltage of the IEC surge standard [13] specified by classes 4 and 5 to represent outdoor and overhead power-line interconnections [4]. The simulated open-circuit generator waveform is shown in the inset of Fig. 10. Both open and short-circuit waveforms meet the IEC61000-4-5 specification of 1.2/50 µs and 8/20 µs respectively. The generator was used to apply a surge strike to the circuit of Fig. 9.

The waveforms in Fig. 10 demonstrate a surge-robust GaN power supply design under a 4 kV surge-generator setting. Component value selection is straightforward; however, it is also important to ensure system-level robustness by using components that work correctly at the peak surge conditions. The primary components considered to suppress the surge are: parasitic input inductance L_{par} (0.5 µH), a 420 V varistor to clamp the input surge, the EMI filter and the input bus capacitance C_{in} (47 uF). As can be seen in Fig. 10, the 4 kV surge has a peak of 800 V (V_{Pulse}) at the output of the generator. The voltage reduction is due to the impedance loading from the power supply. The varistor clamps the input voltage (V_{IN}) to 604 V and the EMI filter inductance and bus capacitance smooth the voltage (V_{Filter}) reaching the GaN half-bridge.

The peak surge voltage reaching the FET, V_{Filter}, is less than 570 V, well below the 720 V surge rating of the FETs. The result shows that it is straightforward to limit the peak surge voltage at the FET, even for severe surge conditions.

VII. Conclusion

A comprehensive methodology for achieving surge-robust GaN-FET power-supplies has been presented for the first time. This includes several aspects: the definition of a test condition, the specification of a parameter ($V_{DS(SURGE)}$), the determination of a test-vehicle circuit for surge-robustness validation, the first validation of surge robust GaN, and the incorporation of the above aspects into a simulation approach for the surge-robust design of GaN power supplies.

The parametric specification, $V_{DS(SURGE)}$, is defined as the maximum operating bus voltage during surge. Our GaN FETs were validated to be robust to power line surges for a surge bus-voltage of 720 V. Parts ran well through the 50-strike specification without hard-fail or efficiency degradation. Our testing shows that GaN FETs have the transient overvoltage capability to switch through surge.

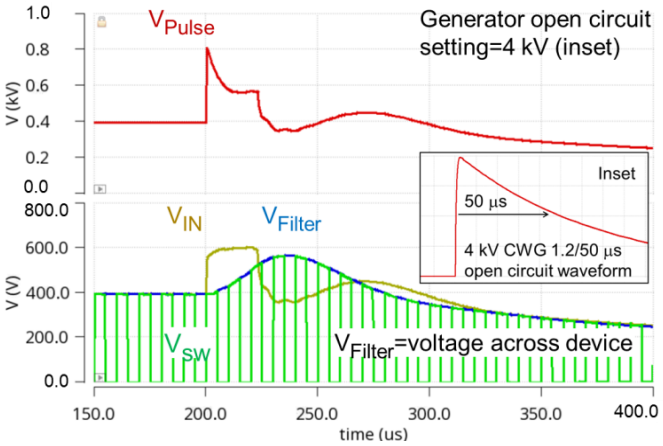

Fig. 10: Simulation of a 4kV surge setting applied to a power supply. The peak device voltage is less than 570V, well below the device surge rating. This illustrates the design of a surge-robust GaN power supply.

The parameter, $V_{DS(SURGE)}$, enables the power supply designer a straightforward method to design a surge-robust GaN power supply. With proper component selection the peak bus voltage during a surge event can easily be kept below the device 720 V surge specification. This parameter also complements the higher-voltage $V_{DS(TR)}$ parameter by providing headroom for ringing during turn-off transients.

It is not necessary for GaN FETs to be avalanche rated in order to be surge-robust in power supplies.

References

[1] D. Powell, B. Hesterman, "Introduction to Voltage Surge Immunity Testing", *presented at the IEEE Power Electronics Society Denver Chapter Meeting*, Sept. 2007

[2] O. Aktas, I. C. Kizilyalli, "Avalanche Capability of Vertical GaN p-n Junctions on Bulk GaN Substrates, *IEEE Elec. Dev. Lett*, v. 36, no. 9, p. 890, 2015

[3] F. Martzoff and G. Hahn, "Surge Voltages in Residential and Industrial Power Circuits", *IEEE Trans. on Power Apparatus and Systems*, v. 89, p. 1049, 1970

[4] IEC 61000-4-5 International Standard, Electromagnetic compatibility (EMC) - Part 4-5: *Testing and measurement techniques – Surge immunity test*, Edition 3.0, 2014

[5] VDE 0884-11, "Semiconductor devices – magnetic and capacitive coupler for basic and reinforced isolation", Ed. 1.0

[6] LMG341xR070 datasheet, available at *www.ti.com*

[7] GS66506T datasheet, available at *www.gansystems.com*

[8] TPH3212PS datasheet, available at *www.transphormusa.com*

[9] Application Note 0008, "Drain Voltage and Avalanche Ratings for GaN FETs", available at *www.transphormusa.com*

[10] S. R. Bahl, D. Ruiz, and D. S. Lee, "Product-level Reliability of GaN Devices ", *IEEE Int. Rel. Phys. Sym.*, p.4A-3-1, 2016

[11] I. Rossetto *et. al*., "Evidence of Hot-Electron Effects During Hard Switching of AlGaN/GaN HEMTs", *IEEE Trans. Electron Devices*", p. 3734, 2017

[12] S. R. Bahl *et. al*., "Application Reliability Validation of GaN Power Devices", *IEEE Int. Elec. Dev. Meeting*, p. 544, 2016

[13] Application Report SLVA711, "IEC 61000-4-x Tests for TI's Protection Devices", 2015, available at *www.ti.com*

[14] D. Miller, R. Kennel, M. Reddig, M. Schlenk, "Surge Immunity Test Analysis for Modern Switching Mode Power Supplies", *IEEE Intl. Tele. Energy Conf. (INTELEC)*, 2016

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