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TI Designs High Speed: Verified Design
Schematic and Layout Recommendations for the GSPS ADC

TEXAS INSTRUMENTS

TI Designs High Speed

TI Designs High Speed designs are analog solutions created by TI's analog experts. Verified Designs offer the theory, part selection, simulation, complete PCB schematic & layout, bill of materials, and measured performance of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

Design Resources

Design Zip File	Simulations, PCB, Gerber, BOM
ADC10D1000	Product Folder
ADC10D1500	Product Folder
ADC12D1000	Product Folder
ADC12D1600	Product Folder
ADC12D1800	Product Folder
ADC12D500RF	Product Folder
ADC12D800RF	Product Folder
ADC12D1000RF	Product Folder
ADC12D1600RF	Product Folder
ADC12D1800RF	Product Folder

Design Description

This reference design is a guide to the schematics and layout for the system designer using a GSPS ADC in their system. Use this reference design along with the datasheet — the datasheet is always the final authority. Also, the ADC1xDxxxx(RF)RB Reference Board provides a useful reference design. All design source files for the Reference Board as well as the CAD/CAE symbols for the ADC are available on the product web page for download. For the purpose of this document, *ADC* or *GSPS ADC* refers to the ADC12D1800RF, ADC12D1600RF, ADC12D1000RF, ADC12D800RF, ADC12D500RF, ADC12D1800, ADC12D1600, ADC12D1000, ADC10D1500, ADC10D1000, ADC12D1600QML, and ADC10D1000QML.

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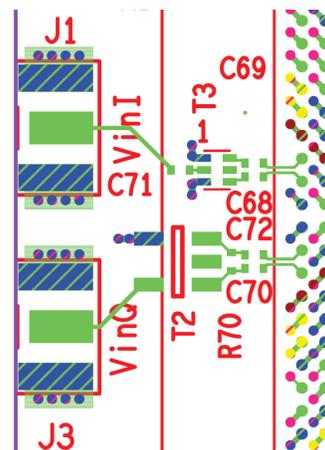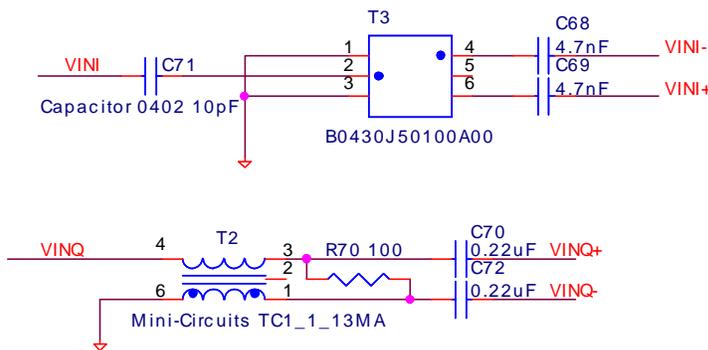
Example Balun Circuits for Analog Inputs

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1   Analog Inputs: VinI and VinQ

The circuit design which drives the analog inputs is highly dependent upon which mode the ADC is in (Non-DES, DESI, DESQ, DESIQ, or DESCLKIQ) and the choice of amplifier or balun. Recommendations for how to drive the different modes are the subject of an existing study, and are not extensively covered in this document.

In the case of any mode, considering the input impedance is important: each I- and Q-input is terminated by a calibrated, internal 100-Ω differential impedance, as shown in the Equivalent Circuit from the datasheet (Figure 1). For matching purposes, the output impedance of whichever circuit is driving the analog inputs should also be 100-Ω differential. The traces to the analog inputs should also be 100-Ω differential and coupled. Many designers are familiar with adding a filter to deal with kick-back noise from the track-and-hold circuitry. However, because this ADC is internally terminated and buffered, a filter for this purpose is not necessary on the GSPS ADCs.
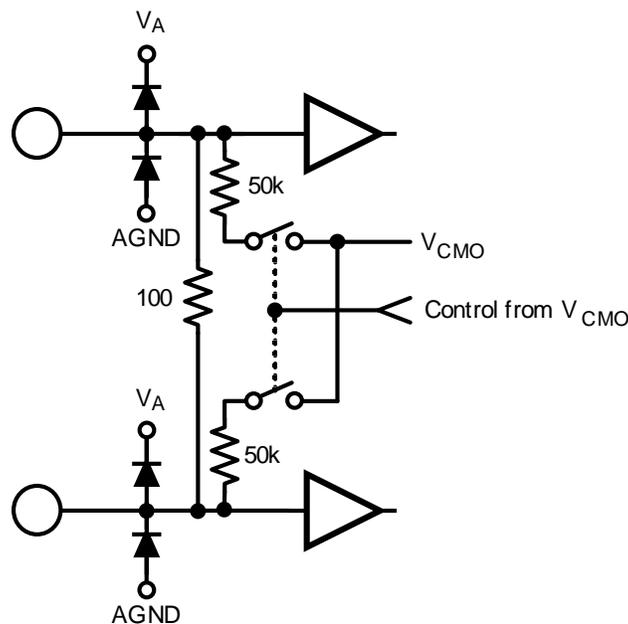
Figure 1. Analog-Input Equivalent Circuit

This ADC configures into AC-coupled or DC-coupled mode. In the case of AC-coupled mode, placing AC-coupling capacitors at the each input pin is required. These capacitors form a simple highpass filter at the input with Equation 1.

$$fc = 1 / (2 \times \pi \times R \times Cvin)$$

where

- R = 50 Ω
- Cvin = the capacitor value chosen   (1)

The analog inputs are one of the most sensitive inputs to pay attention to in order to achieve good performance. For layout, TI recommends to place components as close to the ADC as possible. A long differential trace is an opportunity for standing waves, which cause gain ripple. Also, although the input is differential, which tends to reject common mode noise, a long trace is still an opportunity to couple noise into the analog inputs. Special care must be taken in order to avoid coupling the sampling clock or the power planes into the analog inputs.

For example, the board schematics in Figure 2 show the I-channel being driven by an Anaren B0430J50100 balun and the Q-channel being driven by the Mini-Circuits TC1-1-13MA+ balun, in Figure 2. In both cases, the signal is AC-coupled, but the Mini-Circuits balun has much larger caps to compensate for the inductance of the wire-wound balun. The Mini-Circuits balun is actually 1:1, so it requires an extra 100 Ω across the ADC input to maintain impedance matching for a 50-Ω source. The Anaren balun has a 1:2 impedance ratio, which is already ideal.
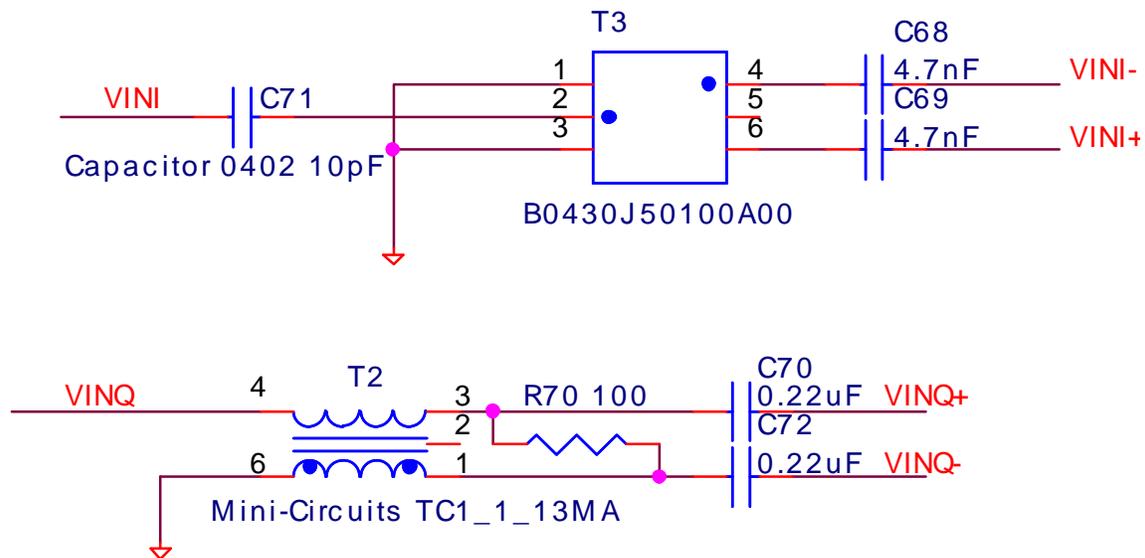
Figure 2. Balun Driving Analog-Input Schematics

Layout is shown in Figure 3. Note how the balun and caps are placed as close the ADC as possible, and there are no other signals nearby which potentially interfere with the analog inputs. The layout is made to be symmetrical.
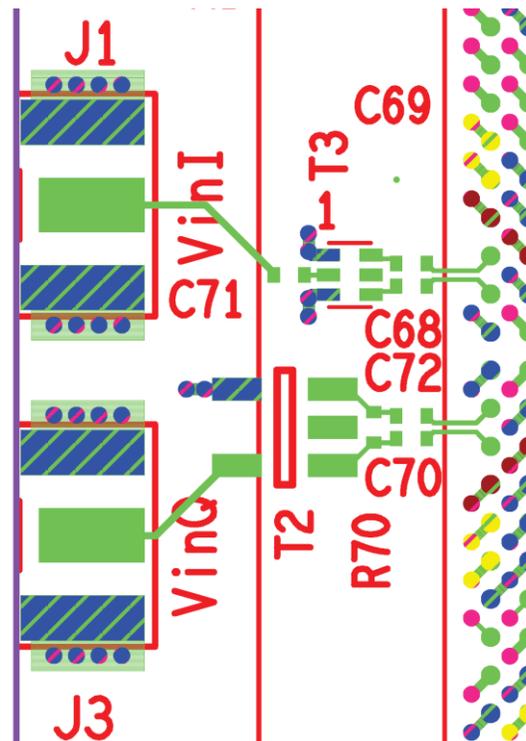

Figure 3. Balun Driving Analog-Input Layout

When driving the ADC in Non-DES Mode, such as dual-channel mode, a common question is how to maintain the polarity of the signals driving the I- and Q-channels. A portion of the Connection Diagram shows that the inputs swap polarity: VinI+, VinI−, VinQ−, VinQ+, see Figure 4. Two identical circuits which are driving these inputs, such as two amplifiers or two baluns, have the same polarity at the output of each, such as Out1+, Out1−, Out2+, Out2−.

H	**VinI+**	**V_TC**
J	**VinI-**	**GND_T**
K	**GND**	**V bias**
L	**GND**	**V bias**
M	**VinQ-**	**GND_T**
N	**VinQ+**	**V_TC**

Figure 4. Analog-Inputs Connection Diagram

There are a number of options for swapping the polarity at the output of one of the channels to match the ADC. For example, if differential amplifiers are used to drive the ADC, then the negative input at one amplifier is driven to invert the signal polarity, see Figure 5.
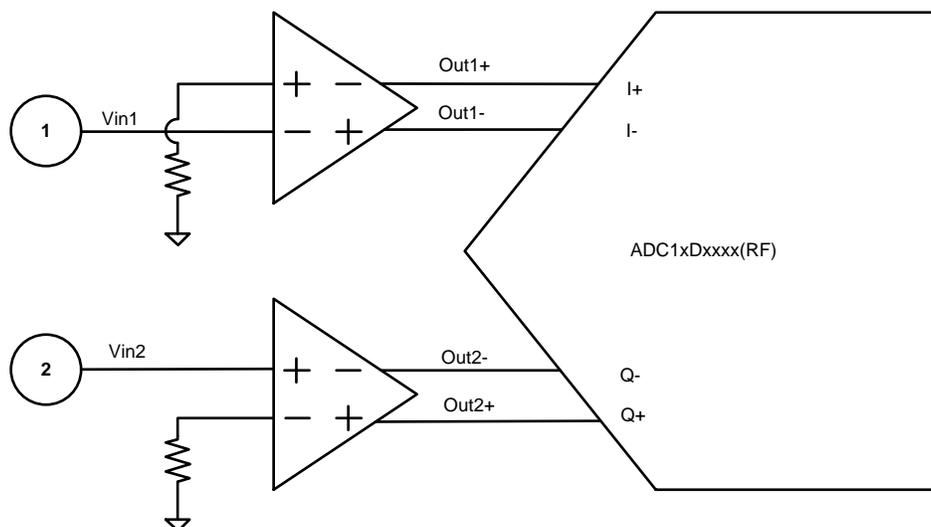
Figure 5. Driving the ADC With Differential Amplifiers to Maintain Polarity

If the negative input is not available, such as in the case of many baluns, the simple brute force way to swap the polarity is to achieve this via the routing. However, crossing the positive (+) and negative (−) input signals requires the use of a different layer, which requires the use of vias. This results in an impedance mismatch at one channel, as well as a mismatch between channels and is not recommended. A cleaner solution is to invert the digital signal of one channel once it has been captured by the FPGA (or ASIC). Note that the ability to invert one channel is not a feature on the ADC.

2 Sampling Clock: FCLK

The sampling clock must always be AC-coupled, so the only consideration here is the value of capacitor. Similar to the analog inputs, the sampling clock is terminated by 100-Ω differential impedance, so the choice of capacitor determines the highpass cutoff frequency:

$$fc = 1 / (2 \times \pi \times R \times C_{FCLK})$$

where

- R = 50 Ω
- C_{FCLK} = the capacitor value chosen   (2)

The traces are 100-Ω differential, coupled impedance to match the clock input. Similar to the analog inputs, this is a sensitive, high-speed signal and special care must be taken in order to avoid coupling the analog inputs or power planes into the sampling clock.

The example from the ADC1xDxxxx(RF)RB uses 4.7-nF caps, which results in a highpass fc = 677 kHz. Chose another value as long as it does not interfere with the sample clock frequency. In the case of a single-ended clock, converting the signal to differential is necessary. TI recommends the Anaren B0430J50100AHF which covers {400 MHz, 3000 MHz}, see the example from the Reference Board in Figure 6. The AC-coupling caps and balun are placed as close as possible to the ADC.
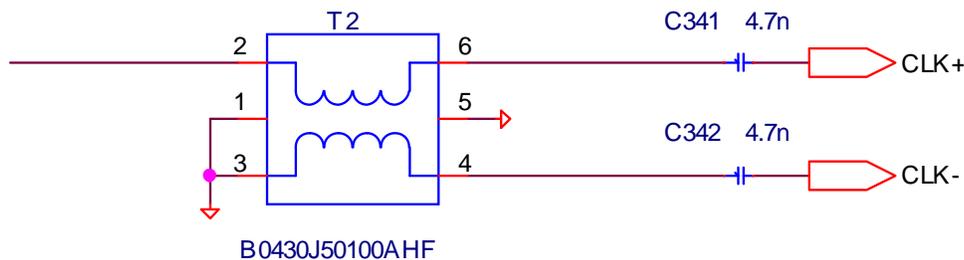

Figure 6. Driving the Sampling Clock on the ADC1xDxxxx(RF)RB

3 Synchronization I/O: RCLK, RCOut1/2, and DCLK_RST

There are two features on the GSPS ADC which are used to synchronize multiple ADCs in a system; AutoSync and DCLK Reset. The AutoSync feature is the subject of another applications note; see *AN-2132 Synchronizing Multiple GSPS ADCs in a System: the AutoSync Feature* (SNAA073) for details. In case only one ADC is used in the system, the synchronization I/O is unused and terminates as shown in Table 1.

Table 1. Unused Synchronization Pin Recommendations

Pin(s)	Unused Termination
RCLK+/-	Do not connect
RCOUT1+/-	Do not connect
RCOUT2+/-	Do not connect
DCLK_RST+	Connect to GND via 1kΩ resistor
DCLK_RST-	Connect to V_A via 1kΩ resistor

In case AutoSync is implemented in the system, TI recommends to AC-couple the reference clocks, see Figure 7. Note that the connections here are shown as single-ended, but are actually differential pairs. For example, 4.7-nF capacitors are also used here. AC-coupling the reference clocks prevents any DC bias issues. Also, having these capacitors in place allows the system designer to conveniently disconnect the reference clocks during system debug.
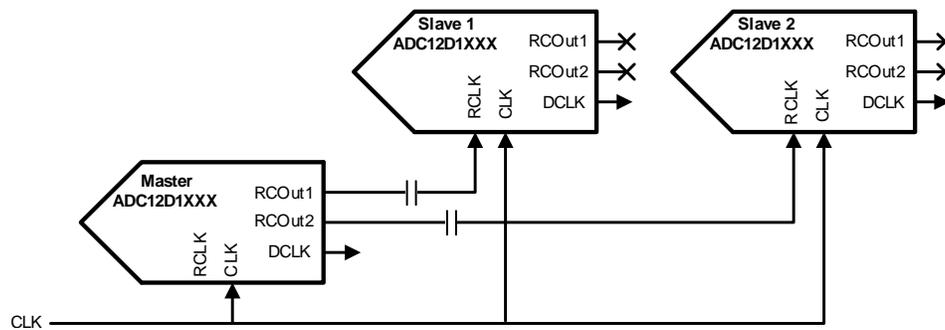
Figure 7. AC-Coupling the AutoSync RCLKs

4 Control Pins

The ADC runs in Extended Control Mode (through the SPI) or Non-ECM (pin-control mode). Some of the control pins on the ADC are active in both ECM and Non-ECM, see the datasheet for details. This reference design only focuses on how to drive the control pins, if they are active and in use.

4.1 Control Pins: Vcmo and Vbg

TI recommends to tie Vbg and Vcmo directly to V_A or GND. Vcmo and Vbg are unique among the control pins in that they are also capable of sourcing and sinking up to 100 uA. This capability means that tying control pins to the power or ground rail via a 1 kΩ, 3.3 kΩ, or 10 kΩ resistor, as is common practice, can lead to an incorrect, ambiguous voltage driving these pins. For example, if Vcmo is tied to GND (to AC-couple the inputs) via a 10-kΩ resistor, the voltage at the pin is V = 10 kΩ × 100 µA = 1 V instead of the desired 0 V.

Vbg selects a higher or lower common-mode voltage for the LVDS outputs. For short traces from ADC to FPGA (or ASIC), the lower voltage is recommended because it consumes less power, and the higher voltage is not shown to result in better signal integrity. For most cases where the ADC and FPGA are located on the same board, the lower voltage is appropriate.

4.2 Control Pin: CalDly

The setting of CalDly is used to determine whether the longer or shorter delay is selected before running the power-on calibration. For this reason, TI recommends to set the CalDly pin via a 1-kΩ resistor to V_A or GND, so that the setting i determined when the power rail of the ADC comes up. If CalDly is set by an FPGA after the ADC powers up, then the value is set after it was used, which is not best practice system design. On the 8-bit ADCs, a problem occurs if the value of CalDly is toggled after power-up, which causes the ADC runs an additional calibration. This potential problem is not an issue on the 10- and 12-bit ADCs, but the best practice is still to set the CalDly pin via a resistor to V_A or GND.

4.3 Control Pin: CAL

The CAL pin is active in both ECM and Non-ECM. The value of this pin is OR'd with the CAL bit from the SPI register, so in case calibration is initiated via the bit in the SPI register, the CAL pin is tied via a 1-kΩ resistor to GND.

4.4 Control Pins: DES, PDI, PDQ, TPM, NDM, FSR, DDRPh, ECEb, and FSR

If the ADC is in Non-ECM (pin control mode), then the control pins must be driven and not left floating. If simply driven directly by the power rails, the control pins are tied to V_A or GND via a 1-kΩ resistor. TI recommends to place, but not populate the other option, see Figure 8 for an example, in case the setting of a pin must be changed during system debug. PDI, PDQ, and ECEb have a 50-kΩ internal pull-up to V_A, as shown in the Equivalent Circuit diagrams in the datasheet. This pull-up means that a 1-kΩ resistor is sufficient to over-drive the default selection. Also, if these control pins are left floating, the default mode of the ADC is Non-ECM with both channels powered down.
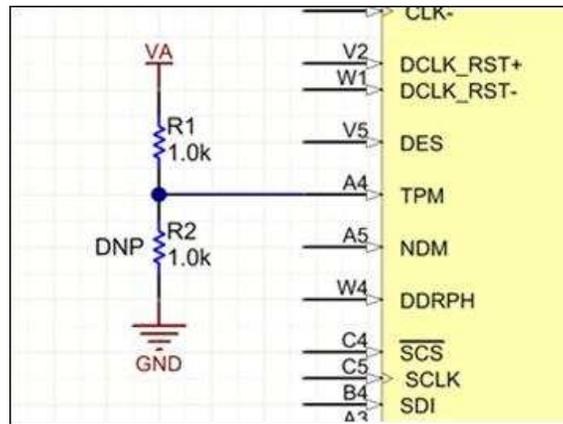
Figure 8. Example of Control Pin Set by Rails

If the control pins are driven by the FPGA, TI recommends to place 10-kΩ resistors close to the outputs of the FPGA, see Figure 9. The 10 kΩ are present in case the FPGA comes up before the ADC; the resistors limit the amount of current which is driven into the ADC control pins to prevent damage. Also, for the ADC1xDxxxx(RF)RB, in case the jumpers are used to set the control pins, the FPGA outputs will not be damaged. On the reference board, there are 50-Ω series resistors at the ADC control pins. These are left-over from when the board was in development and are not necessary in a customer design. In most cases these pins are driven by the 1.8-V FPGA bank. Level translating to the 1.9-V control pins is not necessary because 1.8 V is still above V_{IH} for the control pins. As stated in the datasheet, $V_{IH} = 0.7 \times V_A$.
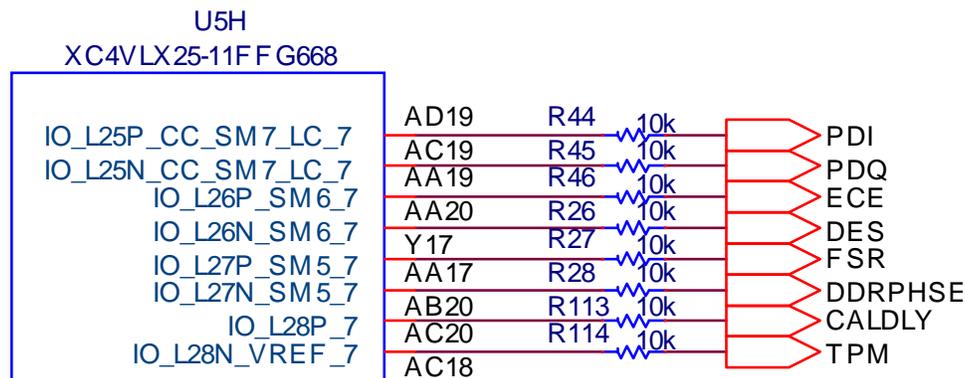

Figure 9. FPGA Driving the Control Pins on the ADC1xDxxxx(RF)RB

5   Outputs Pin: CalRun, ORI and ORQ

CalRun is an output which is high while the calibration is running. In many applications, this signal is routed to the FPGA, so the system can know when the ADC operation is offline calibrating. The over-range outputs, ORI and ORQ, are high when either channel is over-ranged. Because these signals are 1.9 V, but a typical FPGA bank is 1.8 V, there are a couple options. One is to make a simple voltage divider out of two resistors to level shift the signal from 1.9 V to 1.8 V; a level shifter is probably unnecessarily complex since the signal only needs to be shifted to a lower voltage. Another option is to simply drive the FPGA directly, if its inputs can tolerate a slight 0.1 V over-voltage; the ADC1xDxxxx(RF)RB uses this solution. In case the ADC12D2000RF is used, its V_A is 2 V which would be a higher 0.2 V. TI recommends to implement a voltage divider level shifter.

6 Serial Interface: SCSb, SCLK, SDI, and SDO

The Serial Interface signals are generally driven by a 1.8-V bank on the FPGA, see the ADC1xDxxxx(RF)RB for an example. In addition to source files such as schematics and BOM, the FPGA source code for the RB is also available on the product folder. Note that these signals have an internal pull-up, so including an additional one on the board is not necessary.

7 Temperature Diode: Tdiode+/-

The temperature diode provides the internal junction temperature of the ADC, which is monitored by an FPGA. In addition to the ADC, the application monitors additional devices such as ambient temperature, FPGA junction temperature, and junction temperature of other devices. As an example the ADC1xDxxxx(RF)RB uses the LM95233 to monitor ADC, FPGA, and ambient temperature. Noisy system signals, such as clocks are kept away from the Tdiode+/- traces, which must be routed as a differential pair to improve noise immunity.

Table 2. Temperature Sensor Recommendations

Number of External Devices Monitored	Recommended Temperature Sensor
1	LM95235
2	LM95233, LM95213
4	LM95234, LM95214

8 Not-Connected Pins: NC and DNC

DNC stands for *Do Not Connect* and means exactly that. These pins are used for internal test purposes and must not be driven or grounded.

NC stands for *Not Connected* and means that the pin is not bonded out. Therefore the voltage that these pins are connected to is not important; they can also be left floating.

9 External Resistors: Rtrim and Rext

The Rtrim and Rext resistors are used during the calibration process, which is why they must be 0.1% precision resistors. The Rtrim resistor trims the analog and sampling clock inputs to 100-Ω differential. The datasheet limits for the analog input impedance are ensured based on the 0.1% precision resistor at Rtrim. Choosing a resistor with less precision also introduces the same variation into the analog input impedance. The Rext resistor is used during the calibration; altering the value or precision of this resistor alters internal bias currents (such as power consumption) and performance. These resistors are placed as close to the ADC as possible. They must be kept away from noisy system clocks to avoid coupling into the resistors during the calibration, which is a sensitive operation.

10 Power and Grounding

All supply buses for the ADC are sourced from a common linear-voltage regulator. See the portion of the schematic from the ADC1xDxxxx(RF)RB as an example, in Figure 10. This source ensures that all power buses to the ADC turn on and off simultaneously. This single source is split into individual sections of the power plane, with individual decoupling and connection to the different power supply buses of the ADC. Because of the low voltage yet relatively high supply current requirement, the optimal solution is to use a switching regulator to provide an intermediate low voltage, which is then regulated down to the final ADC supply voltage by a linear regulator. This solution is also demonstrated in the ADC1xDxxxxRFRB. TI recommends to have one 100-nF capacitor for each power-ground pin pair. The capacitors are surface-mount multi-layer ceramic-chip capacitors similar to Panasonic part number ECJ-0EB1A104K.
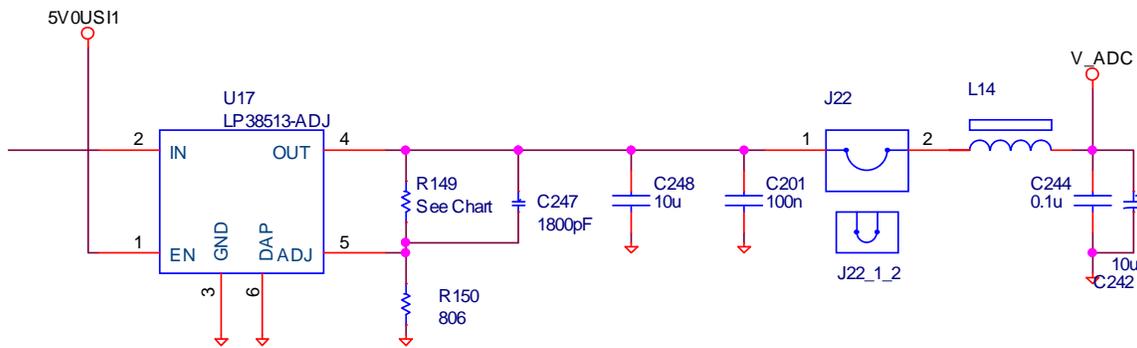
Figure 10. LDO Supplies ADC Power On the ADC1xDxxxx(RF)RB

Power for the ADC is provided through a broad plane which is located on one layer adjacent to the ground planes. Placing the power and ground planes on adjacent layers provides low-impedance decoupling of the ADC supplies, especially at higher frequencies. The output of a linear regulator feeds into the power plane through a low impedance multi-via connection. The power plane is split into individual power peninsulas near the ADC. Each peninsula feeds a particular power bus on the ADC, with decoupling for that power bus connecting the peninsula to the ground plane near each power-ground pin pair. This technique is difficult to use with many printed circuit CAD tools. To avoid this dfficulty, use 0-Ω resistors to connect the power source net to the individual nets for the different ADC power buses. As a final step, remove the 0-Ω resistors and plane, and connect the peninsulas manually after all other error checking is complete. Another option is to include a ferrite bead from the LDO output (V_ADC) to each supply (V_{TC}, V_A, V_E, V_{DR}).
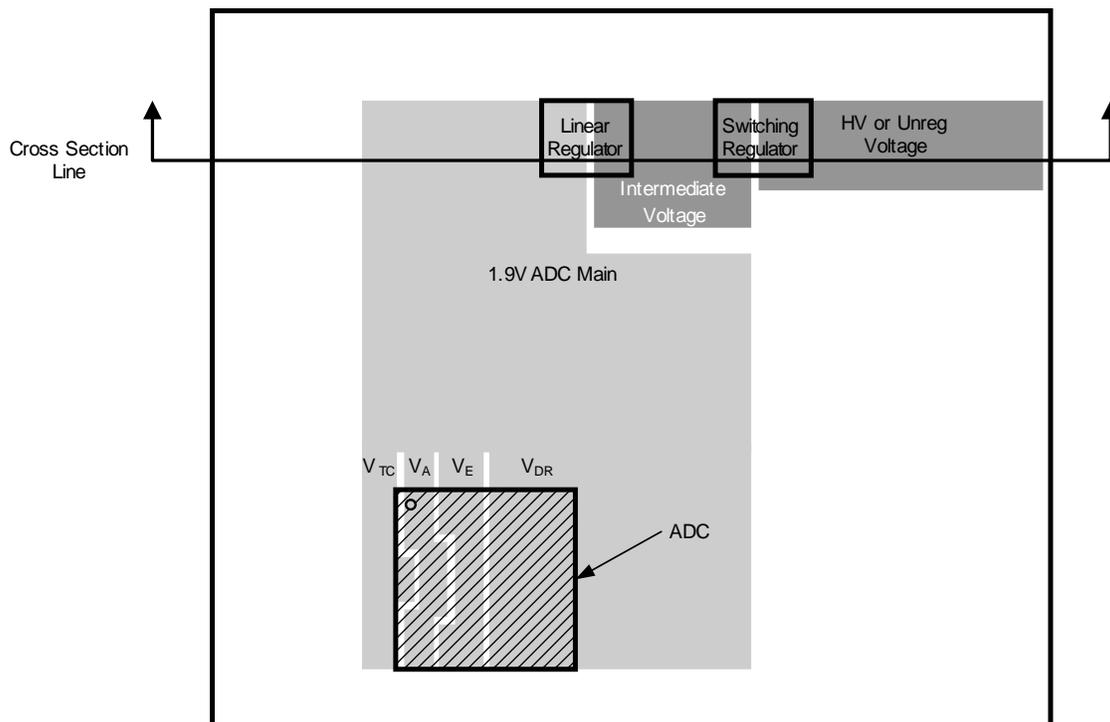

Figure 11. ADC Regulators and Power Planes

Use continuous full-ground planes to minimize the impedance for all ground return paths.. Provide the shortest possible image or return path for all signal traces. Because of the GSPS ADC is capable of high speeds, a continuous ground plane is recommended versus the typical setup featuring a ground plane for each of the analog and digital signals. A continuous ground plane is recommended because high speed signals easily couple to unexpected locations despite separate ground planes. Rather, TI recommends to control noise coupling of ground return currents by careful placement of components, and routing signals such that the return currents of critical signals do not interfere with one another.

The ADC1xDxxxx(RF)RB uses continuous ground planes (except where clear areas are needed to provide appropriate impedance management for specific signals), see Figure 12. Power is provided on one plane, with the ADC main supply being split into multiple zones or peninsulas for the specific power buses of the ADC. Decoupling capacitors are connected between these power-bus peninsulas and the adjacent ground planes using vias. The capacitors are located as close to the individual power-ground pin pairs of the ADC as possible. In most cases, this setup features the capacitors to be located on the opposite side of the PCB to the ADC.
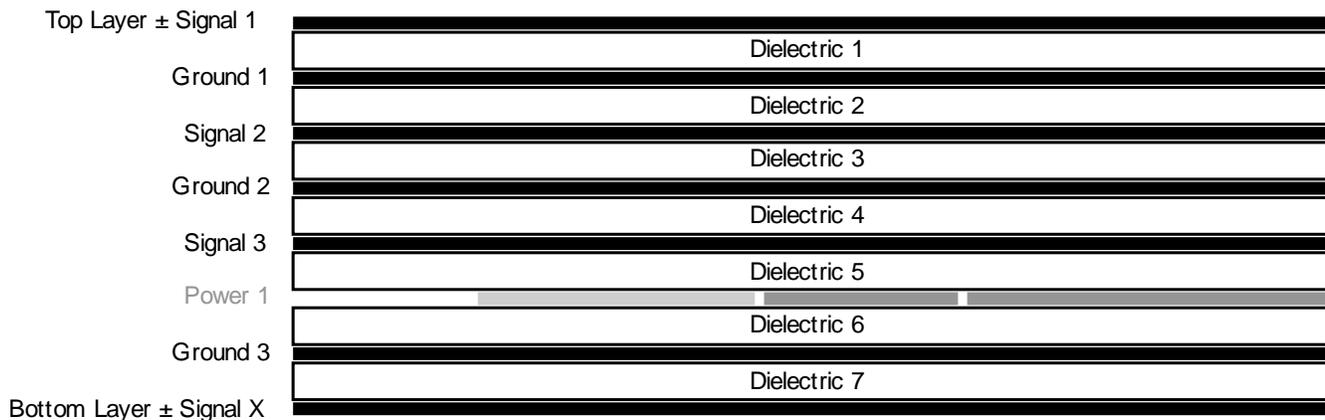

Figure 12. ADC1xDxxxx(RF)RB Stack Up

11   Bias Voltage: VbiasI and VbiasQ

As described in the datasheet, decouple the VbiasI and VbiasQ pins individually with a 100-nF capacitor via a low-resistance low-inductance path to GND. To decouple the pins, place the 100-nF capacitors close to the ADC. Also, do not connect the capacitors together at the ADC. For a correct example, see the portion of the ADC1xDxxxx(RF)RB schematic in Figure 13:
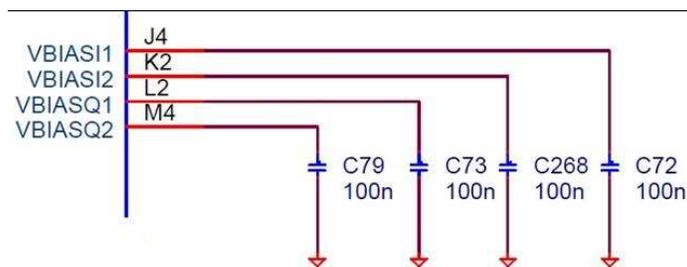

Figure 13. VbiasI and VbiasQ in ADC1xDxxxx(RF)RB

12   Data and DCLKs

The Data (DQd, DId, DQ, and DI) as well as the Data Clocks (DCLKI and DCLKQ) are LVDS signals and should be terminated at the receiver with 100-Ω differential impedance. Note that many FPGAs have an internal 100-Ω impedance, so before placing an additional 100 Ω, check the FPGA specifications. Route each positive-negative pair as a coupled, differential pair. Avoid routing the Data and DCLKs close to any sensitive analog signals.

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