Analog Engineer's Circuit

Programmable comparator circuit with buffered digital potentiometer

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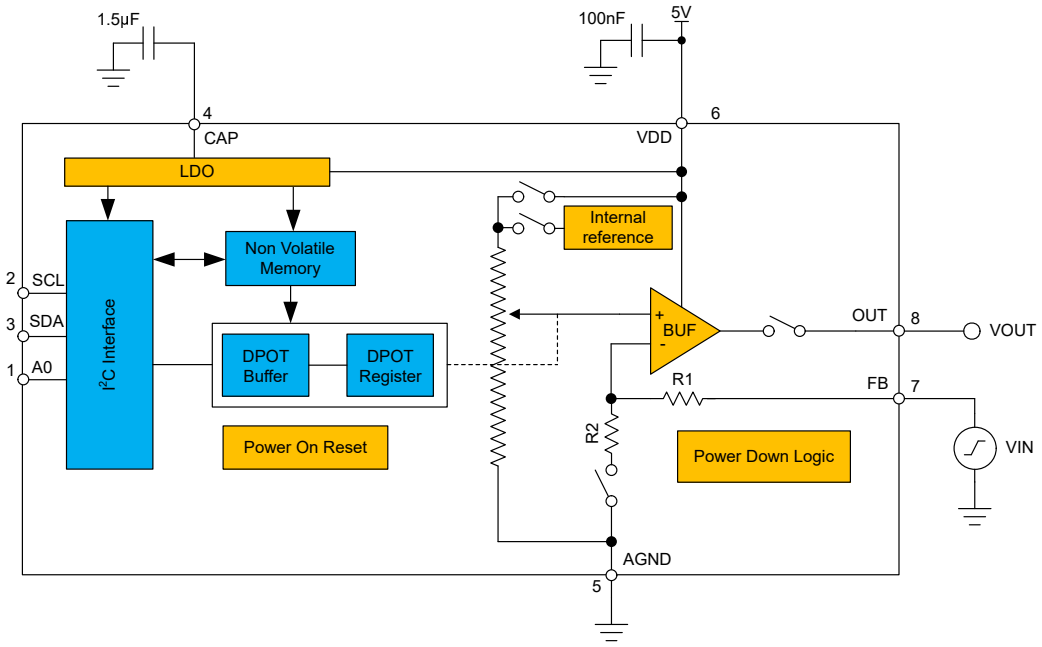
Design Objective

Key Input Parameter	Key Output Signal	Recommended Device
0-V to 5.5-V analog input, programmable threshold voltage	Digital output of a comparator	TPL1401

Objective: *Create a comparator with an adjustable threshold using a buffered digital potentiometer.*

Design Description

This design uses a buffered digital potentiometer (digipot) to create a comparator with a programmable threshold value. A digipot with a buffered wiper provides higher load regulation. In this design, the integrated buffer will act as a comparator and the output of the digipot will act as the threshold for the comparator. Using a 256-tap digipot such as the TPL1401 allows for 8 bits of programmability for the comparator. The TPL1401 integrated buffer has an exposed feedback path via the feedback pin (FB) which will act as the voltage input to the comparator. All register settings can be saved using the non-volatile memory (NVM) on the TPL1401, meaning that the device can be used without a processor, even after a power cycle. This programmable comparator circuit can be used in applications such as appliances pumps and fans, cordless vacuum cleaners, video doorbells, or automotive battery management systems (BMS).



Design Notes

1. The *TPL1401 256-Tap, High-Accuracy, Digital Potentiometer With Buffered Wiper Data Sheet* recommends using a 100-nF decoupling capacitor for the VDD pin, and a 1.5µF or greater bypass capacitor for the CAP pin. The CAP pin is connected to the internal LDO. Place these capacitors close to the device pins.
2. An external reference of 1.8V to 5.5V can be applied to the VDD pin of the device. In addition, there is an internal precision 1.21-V reference with ×1.5, ×2, ×3, and ×4 gain options. If using a noisy supply, it is best to use the internal reference instead of VDD as the reference because noise on the reference translates directly to noise on the output of the TPL1401.
3. The input signal should not exceed VDD. Also, the maximum threshold voltage is limited by the reference voltage used. If necessary, larger input voltages can be scaled using a voltage divider, and the threshold voltage can be adjusted accordingly.
4. In this design, the 5-V VDD supply input is used as the reference. The threshold value is set to 2V using the DPOT_POS field of the DPOT_POSITION register. The code programmed to this field, in decimal, is calculated using:

$$DPOT\_POS = \frac{V_{THRESH}}{V_{REF} \times GAIN} \times 256$$

With a 5-V reference, unity gain, and a threshold value of 2V, the equation becomes:

$$DPOT\_POS = \frac{2V}{5V} \times 256 = 102.4d$$

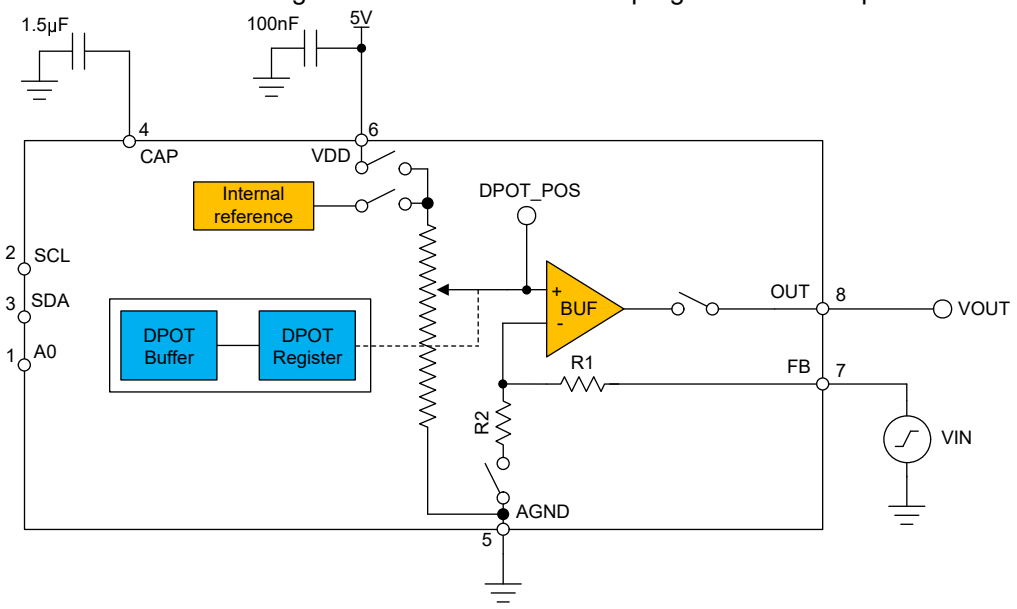
This is rounded down to 102d, to give a threshold of 1.992V.

Using a 5-V reference and the 8-bit TPL1401, the LSB size, or step size between each code, is about 19.5mV. Using lower reference voltages decreases the LSB size and thus increases the resolution of the threshold value. Using a smaller reference limits the upper limit of the threshold value, but as discussed earlier, input voltages can be scaled down if necessary.

5. The TPL1401 can be programmed with the initial register settings described in the Register Settings section using I2C. The initial register settings can be saved in the NVM by writing a 1 to the NVM_PROG field of the PROTECT register. After programming the NVM, the device loads all registers with the applicable values stored in the NVM after a reset or a power cycle.

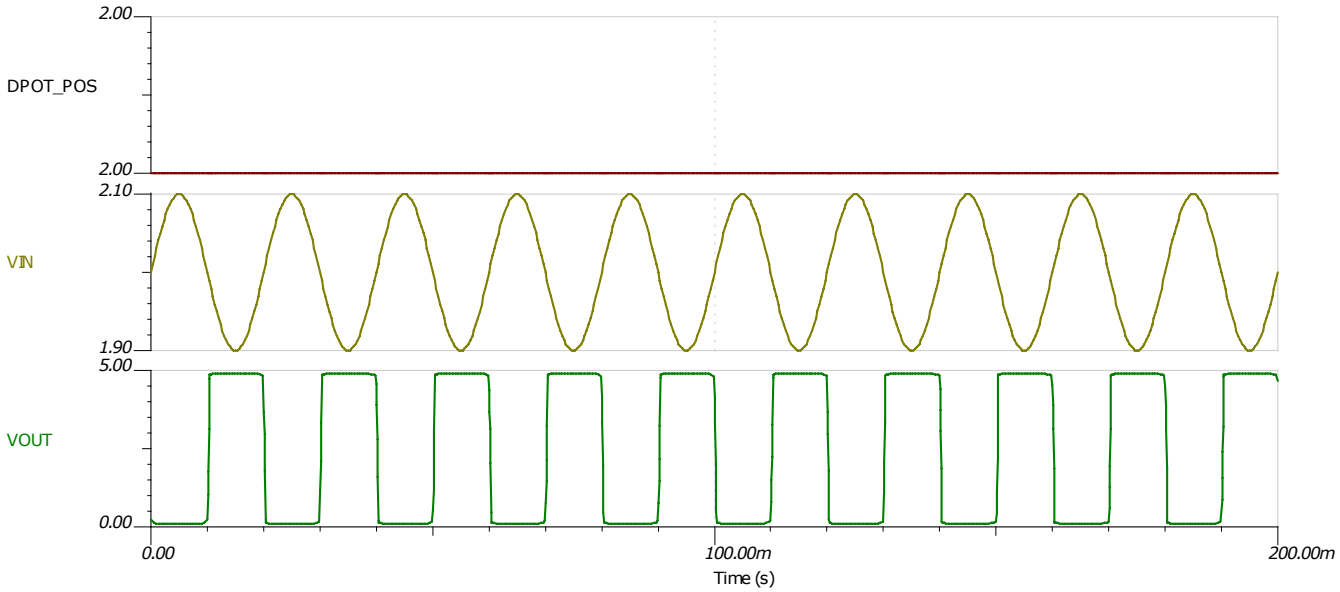
Design Simulations

This schematic is used for the following simulation of the TPL1401 programmable comparator.



Transient Simulation Results

This simulation shows the TPL1401 output responding to a 200-mVpp input sine wave which is biased around the 2-V threshold value.



Register Settings

Register Configuration for the TPL1401 Programmable Comparator

Register Address	Register Name	Setting	Description
0xD1	GENERAL_CONFIG	0x01E0	[15:14] 0b00: Always write 0b00
			[13] 0b0: Write 0b1 to lock the device. Unlock by writing 0b0101 to DEVICE_UNLOCK_CODE field in the PROTECT register
			[12:5] 0x0F: Always write 0x0F
			[4:3] 0b00: Powers up the device output
			[2] 0b0: Disables the internal reference
			[1:0] 0b00: Sets the reference to VOUT gain 1.5×
0xD3	PROTECT	0x0010	[15:12] 0b0000: Write 0b0101 to unlock the device
			[11:10] 0b00: Don't care
			[9] 0b0: Write 0b1 to load all registers with factory reset values
			[8:6] 0b000: Always write 0b000
			[5] 0b0: Write 0b1 to reload applicable registers with existing NVM settings
			[4] 0b1: Write 0b1 to store applicable register settings to the NVM
			[3:0] 0b0000: Write 0b1010 to reset registers with existing NVM settings or default settings
0x21	DPOT_POSITION	0x0660	[15:12] 0b0000: Don't care
			[11:4] 0x66: 8-bit data updates the digipot output
			[3:0] 0b0000: Don't care

Pseudo Code Example

The following shows a pseudo code sequence to program the initial register values to the NVM of the TPL1401. The values given here are for the design choices made in the Design Notes.

Pseudo Code Example for the TPL1401 Programmable Comparator

```
//SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
//Power-up the device, internal reference disabled
WRITE GENERAL_CONFIG(0xD1), 0x01, 0xE0
//Write digipot code 12-bit aligned)
WRITE DPOT_POSITION(0x21), 0x06, 0x60
//Write settings to the NVM
WRITE PROTECT(0xD3), 0x00, 0x10
```

Design Featured Devices

Device	Key Features	Link
TPL1401	256-tap high-accuracy digital potentiometer (digipot) with buffered wiper	ti.com/product/TPL1401

Find other possible devices using the Parametric search tool.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, TPL1401 Evaluation Module
- Texas Instruments, *TPL1401 Evaluation Module User's Guide*
- Texas Instruments, TPL1401 FAQ
- Texas Instruments, Precision Labs - DACs

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