Application Note

Cascaded LMX1204 Phase-Error Analysis

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ABSTRACT

The LMX1204 device is a high-frequency clock distribution device. The device is designed for distributing a clock or local oscillator source to multiple transceiver channels. Each device supports four outputs. The devices can be cascaded when more channels are needed with negligible performance impact. The Cascaded LMX1204 Reference Design uses two layers of the LMX1204 device to facilitate 16 outputs. This report measures and analyzes the phase response between the outputs to illustrate typical phase error response with a realistic device and layout configuration.

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Trademarks

1 Introduction

The LMX1204 is a high-frequency clock distribution device that supports up to 12.8 GHz. The device supports four outputs (each with a SYSREF output) and an additional low-frequency output designed for clocking an FPGA. The LMX1204 is designed for distributing a high-frequency clock to multiple RF sampling devices used in phased-array systems. In cases where more outputs are needed, the LMX1204 devices can be cascaded to multiply the number of outputs with negligible impact to clock quality. For the large phased-array systems, maintaining tight timing between the outputs is critical to make sure received signals line up properly.

The LMX1204 Reference Design cascades two layers of the LMX1204 device to distribute a clock to 16 outputs. Figure 1-1 shows a block diagram of the reference design. The cascaded approach is designed for clocking an array of AFE7950 RF sampling transceivers that support a 64T64R array system as depicted in Figure 1-2.

This note outlines measurements on an LMX1204 Reference Design designed to analyze the phase-error response in a typical configuration. This document is not intended to be a full characterization of the LMX1204 device itself as this reference design includes interconnecting traces and a bank of 0.5-m RF cables on the output. Use this application note as a general guideline for typical performance variation in a realistic configuration.

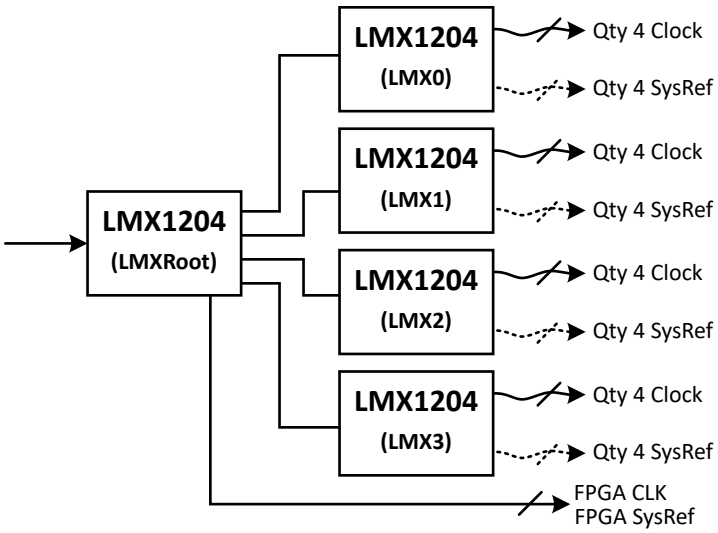

Figure 1-1. Cascaded LMX1204 Reference Design

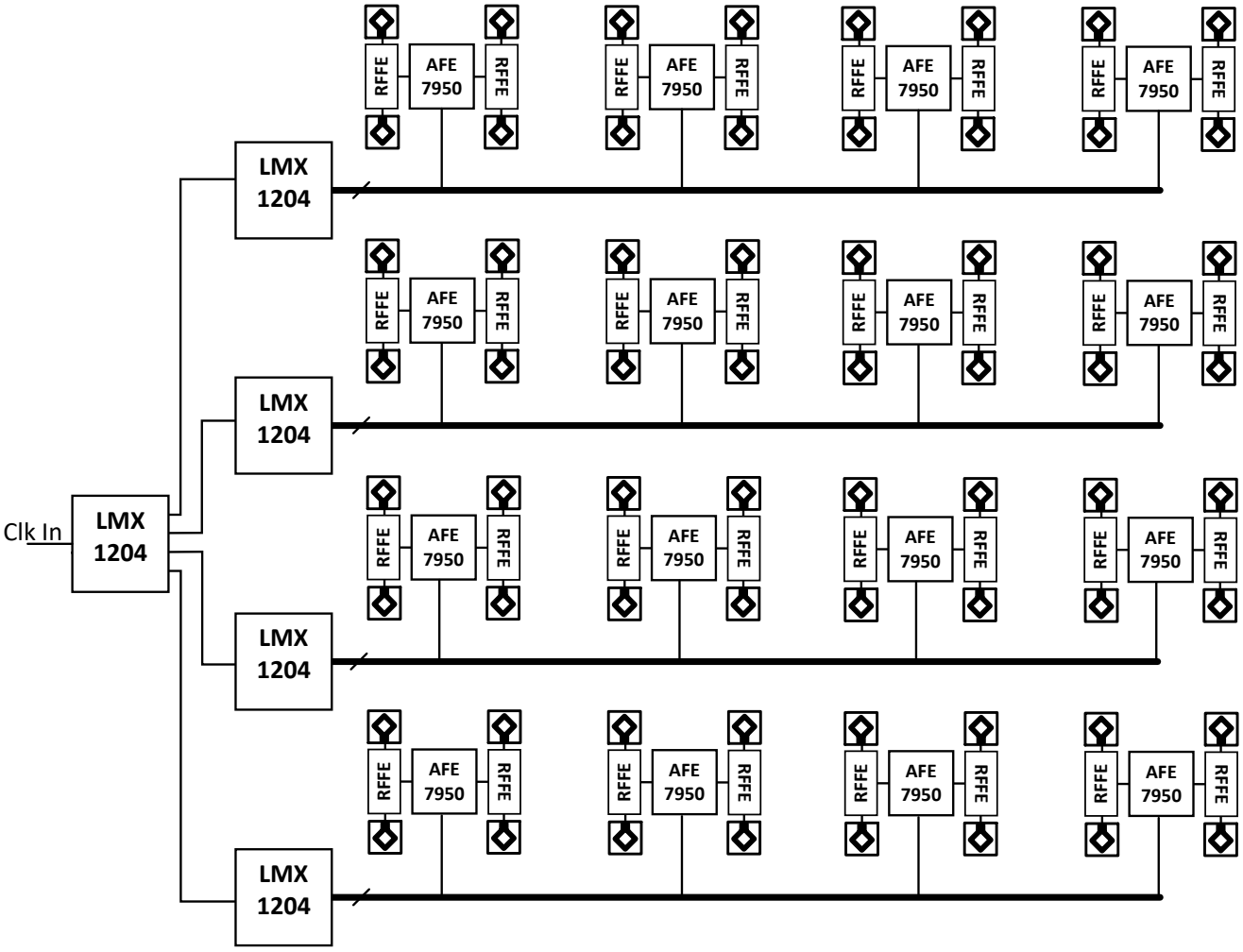

Figure 1-2. Cascaded LMX1204 Clocking AFE7950 RF Sampling Transceivers in 64T64R Array

2 Test Setup

The test setup uses a *Network Analyzer* to accurately measure the phase response through the distribution channels. Each port is calibrated to eliminate the contribution of the input source cable. The frequency range is set to 4 GHz to 8 GHz. The maximum frequency was limited by the upper frequency limit of the network analyzer. Figure 2-1 illustrates the test setup.

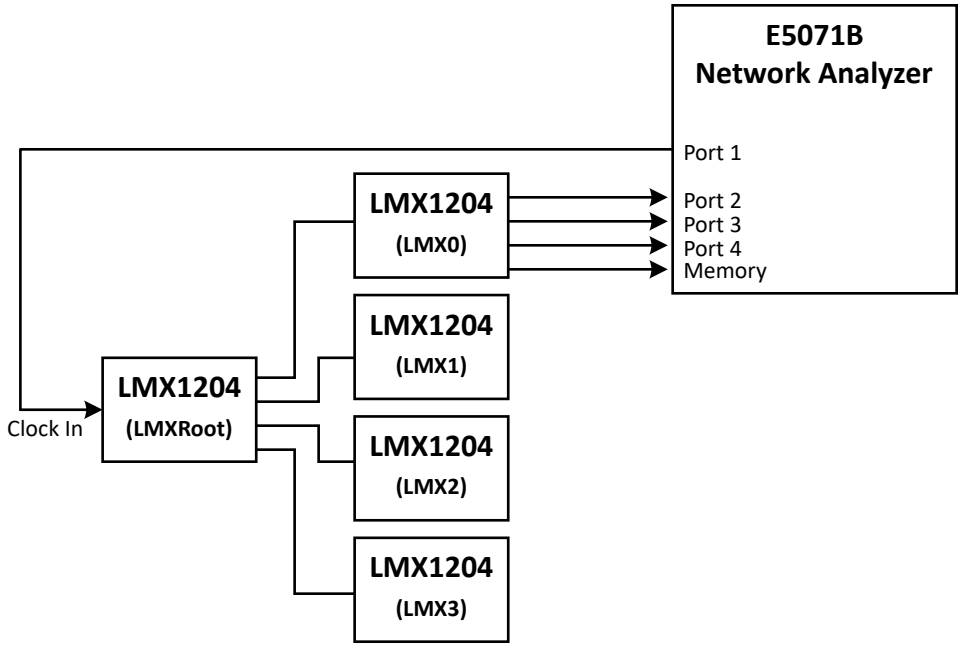

Figure 2-1. Cascaded LMX1204 Test Setup

3 Measurement Results

3.1 Input/Output Return Loss

Figure 3-1 shows the input and output return loss of the cascaded LMX1204 reference design. Both responses show return loss performance less than –10 dB indicating a good 50-Ω match and transmission lines on the board.

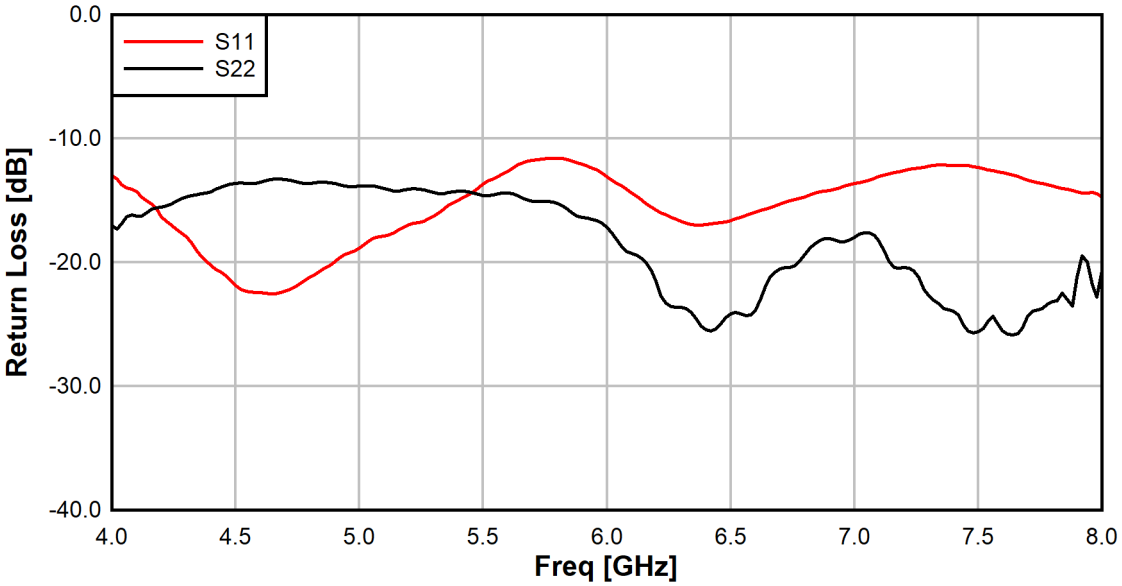

Figure 3-1. Input/Output Return Loss

3.2 Group Delay

Figure 3-2 shows the group delay through the reference design. The group delay response is proportional to the slope of the phase response. Group delay is a convenient way to visualize deviation from linear phase. For this reference design, the group delay is around 3.7 ns ±0.4 ns. The response between device outputs is very consistent.

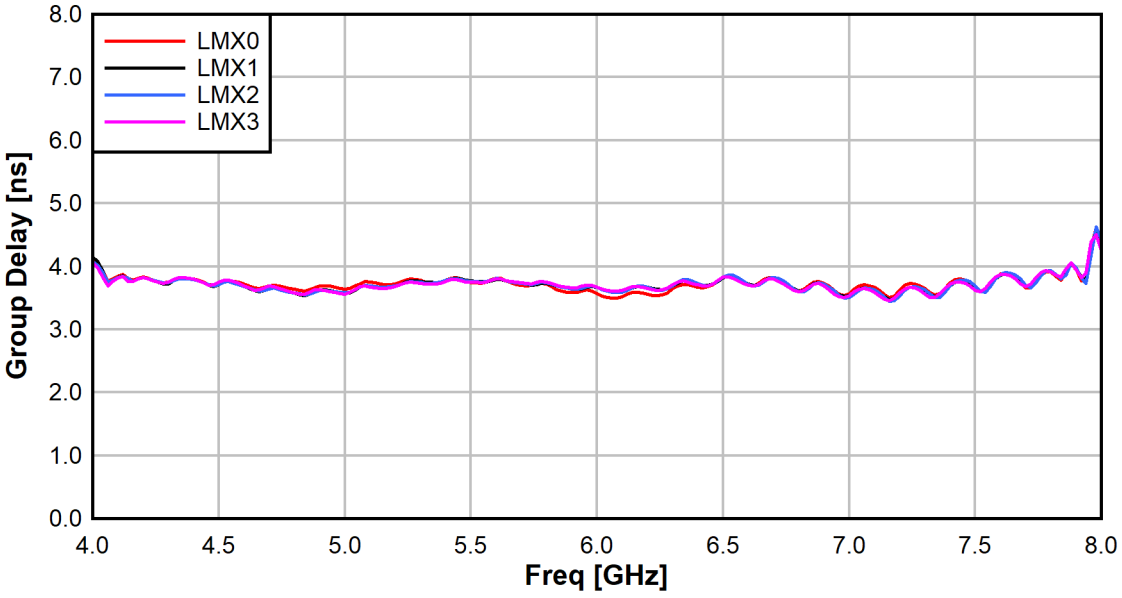

Figure 3-2. Group Delay Response

3.3 Phase Error Within One LMX1204 Device

Figure 3-3 shows the phase error relative to the average phase within one LMX1204 device across the 4 channels. Within a single device, the phase response is very consistent across each of the channels. Based on information from the LMX1204 data sheet, the expected skew between channels in one device is less than 2 ps. In this case, there is variation within the device in addition to tolerance variations within the output traces and RF cables.

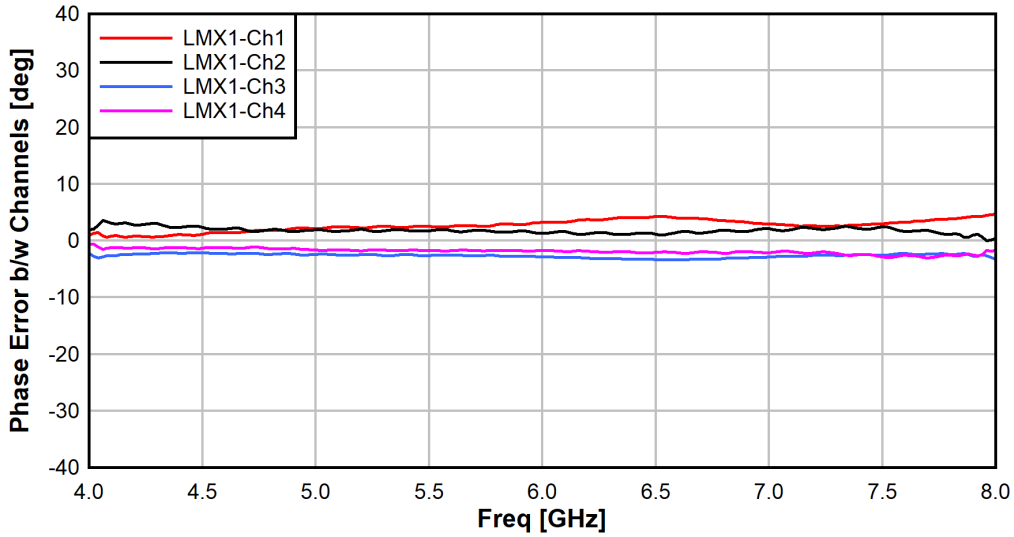

Figure 3-3. Phase Error Across Channels of one LMX1204 Device

3.4 Phase Error Across all LMX1204 Channels

Figure 3-4 shows the phase error relative to the overall average between all output channels of the lower level LMX1204 devices comprising a total of 16 channels. This variation includes output trace and cables as the previous case in addition to the root LMX1204 device variation and feed traces. The phase error in this situation is also very consistent across all channels with LMX0 device being a small outlier. This is likely due to trace routing on the board and having to transition between the top and bottom layer for that device.

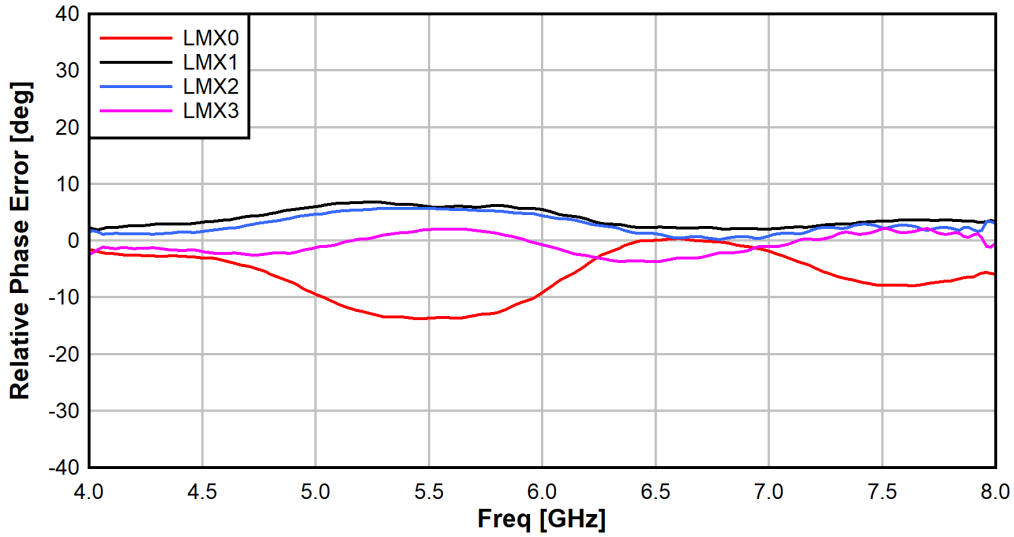

Figure 3-4. Relative Phase Error Across Channels Over Multiple LMX1204 Devices

4 Conclusion

The cascaded LMX1204 reference design illustrates excellent phase balance for clock distribution paramount for clocking high-speed data converters or driving transceiver local oscillator (LO) inputs. Within a given LMX1204 device, the phase error is generally within ±5 degrees. Between multiple devices, the phase error is generally within ±15 degrees.

In some applications, it can be more convenient to think about the error or mismatch between channels in terms of timing error as opposed to phase. The phase error can be converted to a time skew parameter at a given frequency using Equation 1.

$$\tau_{skew} = \frac{\varphi_{err}[deg]}{360 \times f} \quad (1)$$

As an example, at 8 GHz, a 10-degree phase error translates to a skew error of 3.4 ps.

5 References

1. Texas Instruments, *LMX1204 Low-Noise, High-Frequency JESD Buffer/Multiplier/Divider* data sheet

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