

Figure 2. Block Diagram for the MASH_SEED Location in $\Sigma\Delta$ modulator(MASH)

Figure 3 from the PLLatinum sim tool shows different spur classifications at the output of PLL.

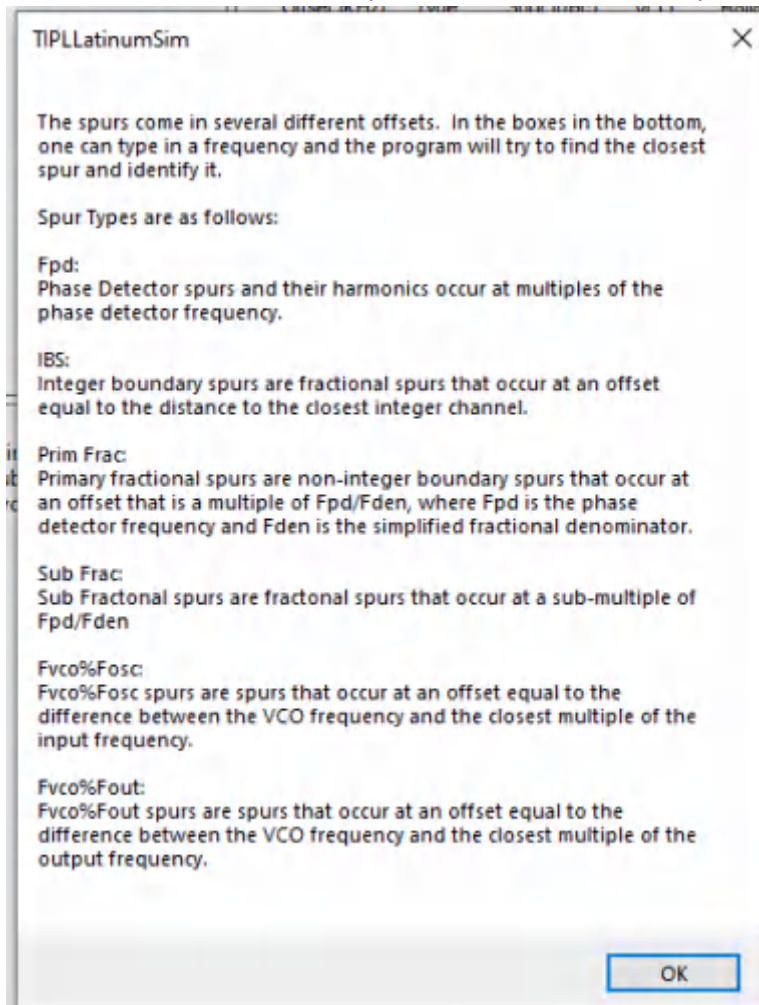


Figure 3. Various Spurs Possible in PLL and Modeled in PLLatinum simTool

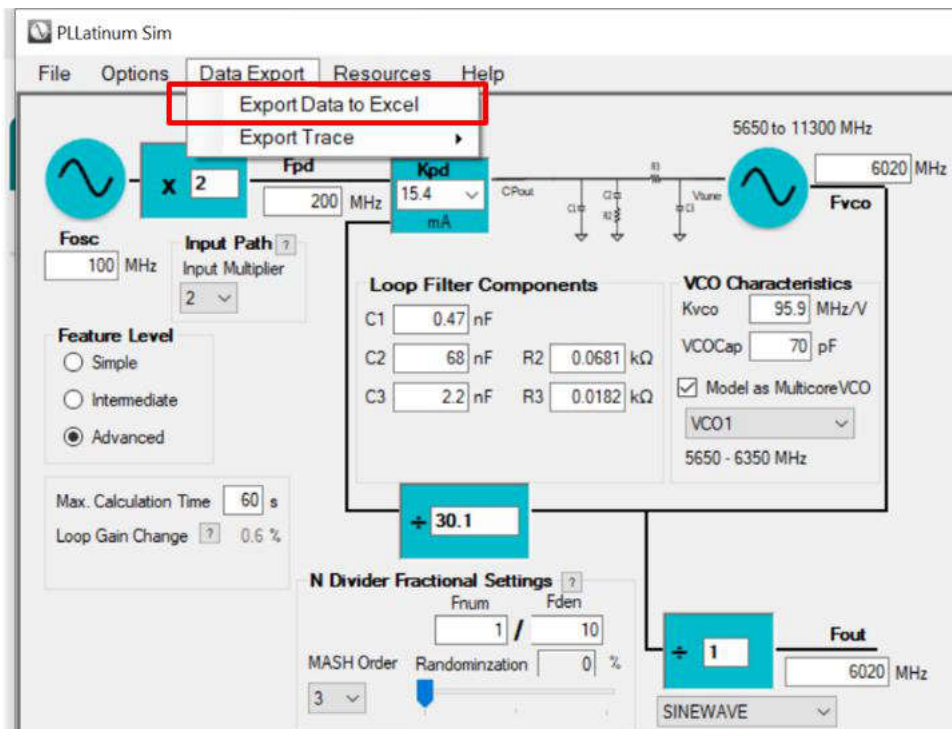


Figure 4. MASH Pattern Export Option in PLLatinum Sim

For a particular Fraction input and MASH_SEED, the PLLatinum sim tool predicts and models the pattern of the MASH output. Export the pattern from the PLLatinum sim tool as shown in Figure 4. Column X in spurs sheet of the downloaded excel provides the sequence.

Fractional Mode

Fractional Mode: NUM/DEN is non-zero. There are multiple orders for MASH operation. This App brief covers the following topics:

- **First Order:** Example of spur placement.
- **Second Order:** Example for the impact of MASH_SEED on spurs and optimization.
- **Second Order versus Third Order and spur optimization:** Two examples.
- **Third Order:** Denominator(PLL_DEN) offset by 1.
- **More Guidelines for MASH_SEED selection**

First Order

As shown in below in Figure 5, first order MASH gives IBS (Integer Boundary Spur) at 20MHz with magnitude of -62.1dBc/Hz. This spur magnitude can be optimized as shown in the rest of the App brief.

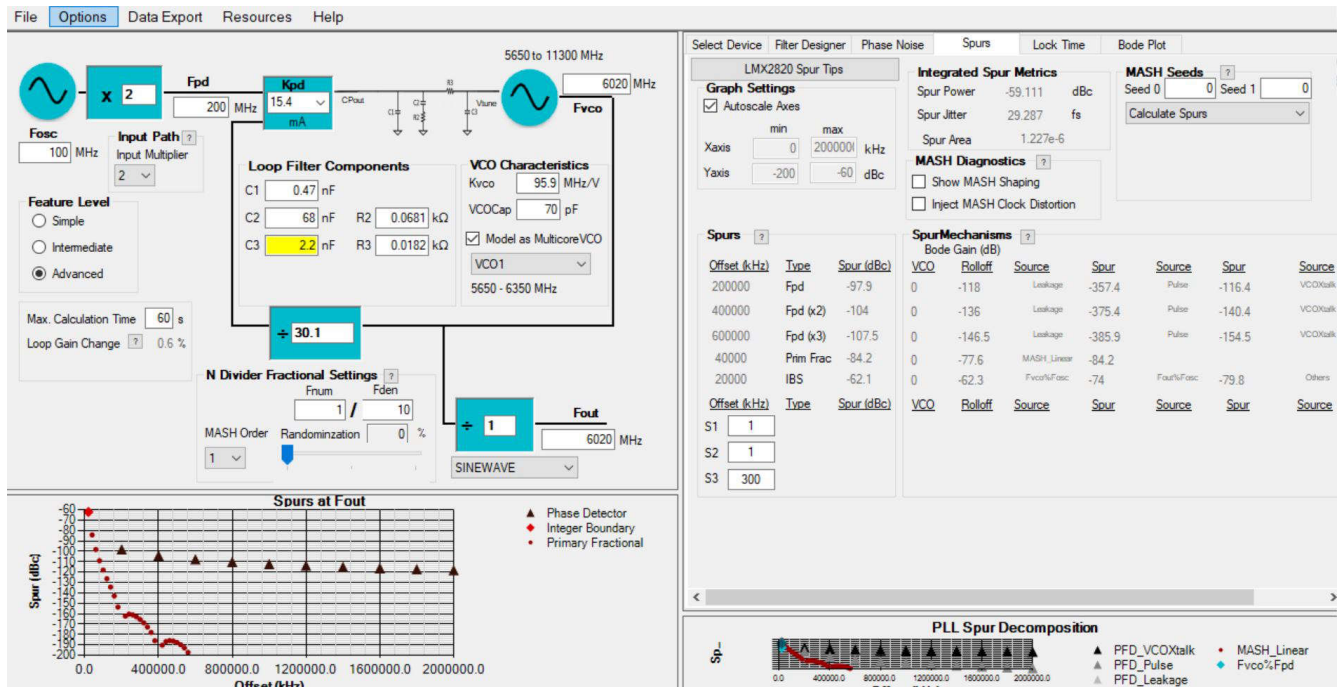


Figure 5. PLLatinum Sim Showing the First Order Spurs Placement

Second Order

Check the PLLatinum sim tool to observe how changing the MASH_SEED changes the spur location. Figure 6 and Figure 7 show PLLatinum sim tool snapshots detailing the impact on the spurs due to MASH_SEED change. How do user knows what MASH_SEED to use for a particular configuration? The red box shown in Figure 7 highlights the option to generate seed based on the optimization needs of the user. Once the optimization is done by PLLatinum, there is a notification at the bottom, as shown in Figure 7.

When MASH_ORDER is changed from first to second, IBS spur at 20MHz are reduced from -62.1dBc/Hz (Figure 5) compared to -73dBc/Hz (Figure 6).

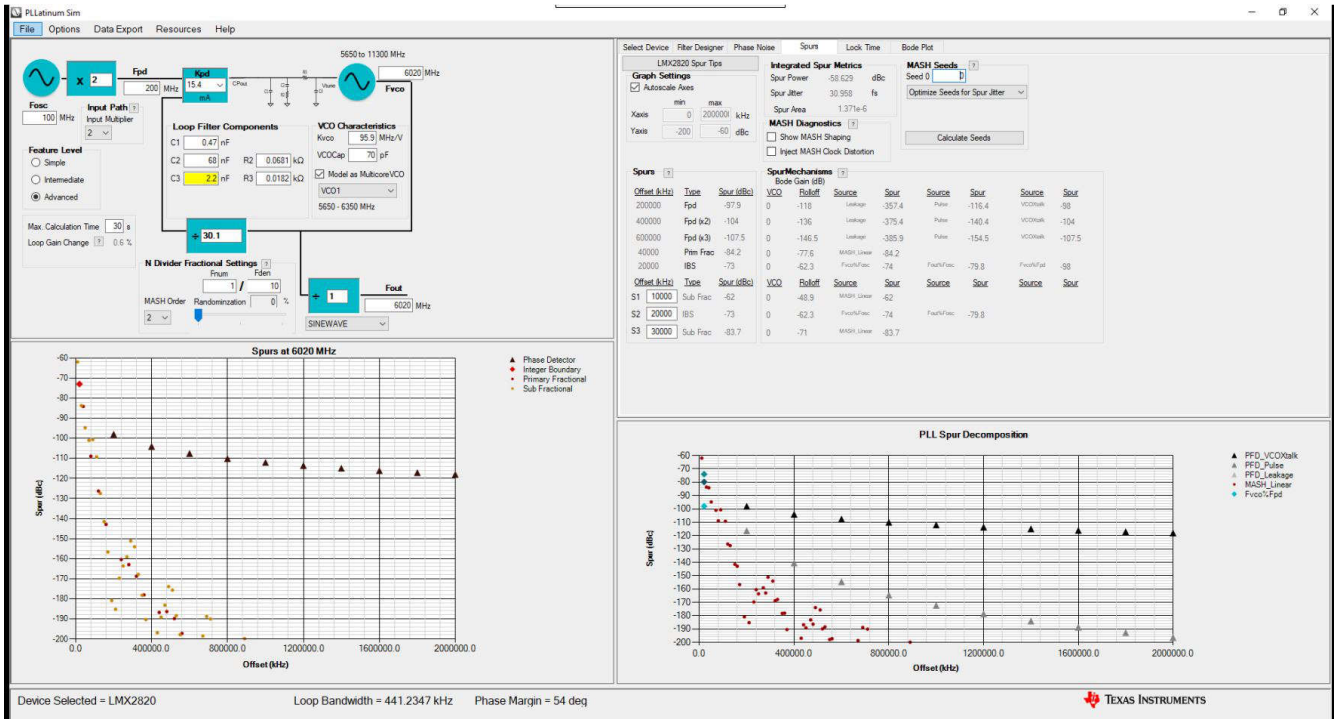


Figure 6. MASH_SEED As 0

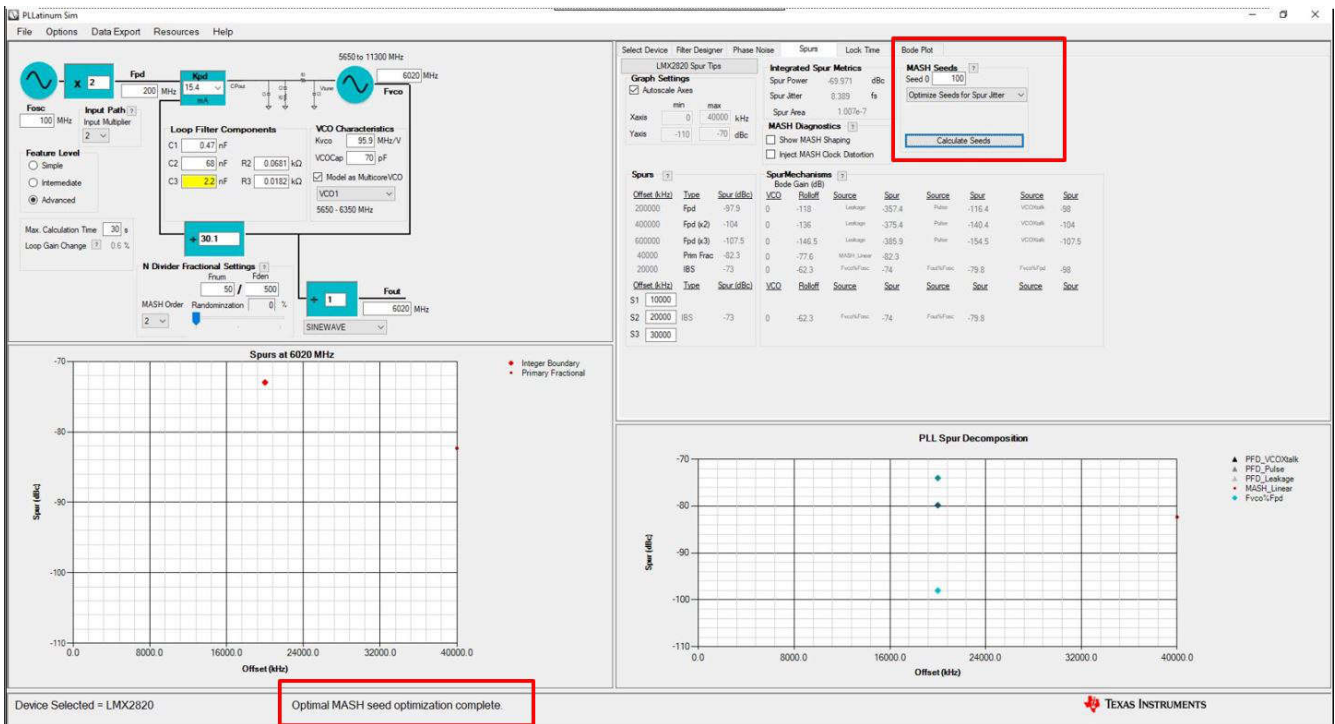


Figure 7. MASH_SEED As 100

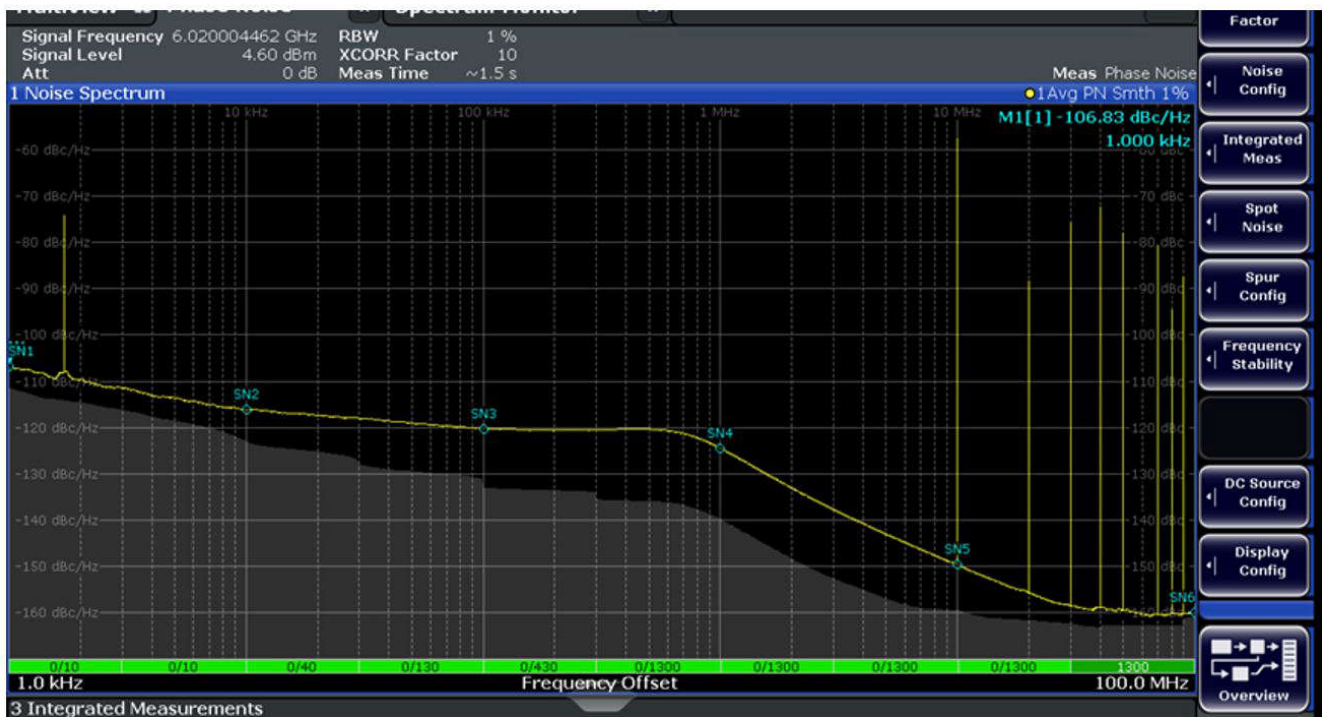


Figure 8. MASH_SEED As 0

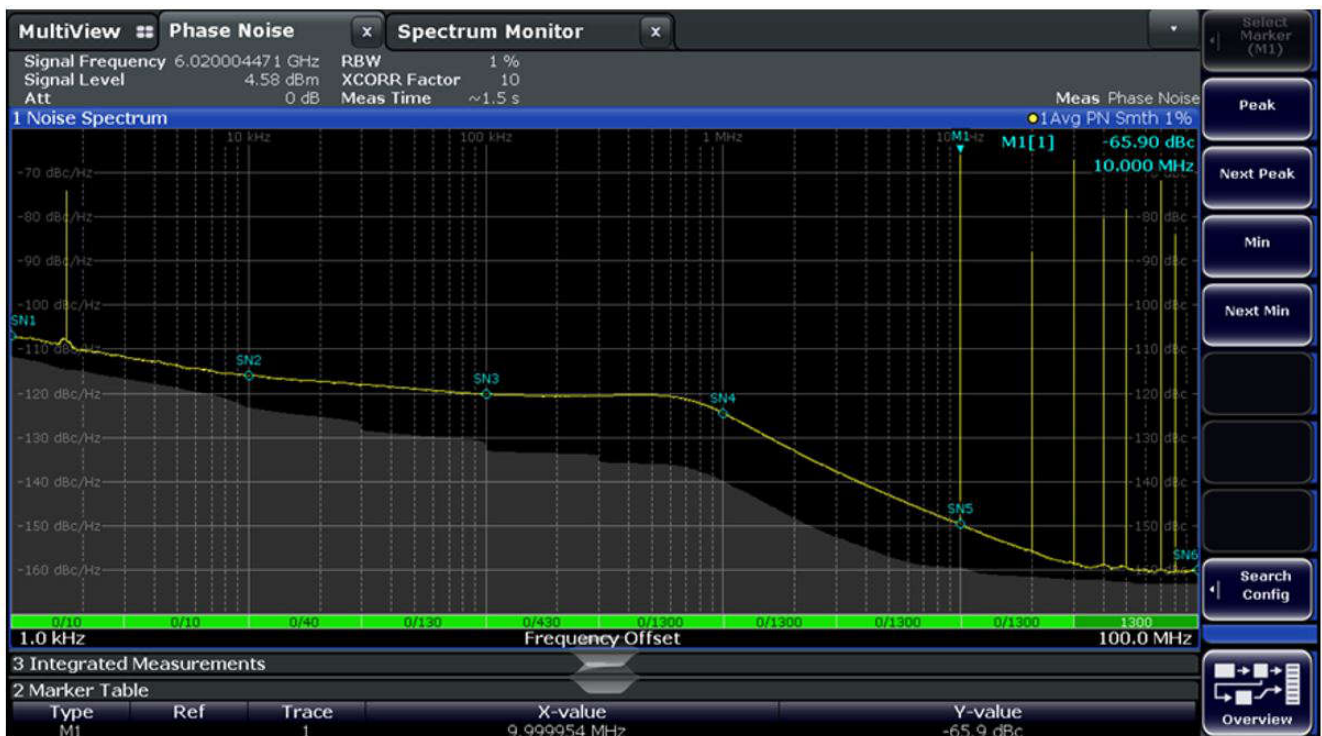


Figure 9. MASH_SEED As 100

IBS (Integer Boundary Spur) at 20MHz offset is not impacted by the MASH_SEED variation.

Sub-Frac Spurs ($0.5 \times \text{Fpfd} / \text{DEN} = 0.5 \times (200\text{M} / 10)$) at 10MHz that are generated from MASH are reduced when MASH_SEED optimization is used. As shown in above Figure 8 and Figure 9, when MASH_SEED is changed from 0 to 100, dominant Sub-Frac Spur at 10MHz are reduced from -57dBc/Hz to -65.9dBc/Hz. The PLLatinum sim tool predicted the vanishing of Sub-Frac spurs with MASH_SEED of 100 but in silicon there is reduction of

9dBc/Hz for the major Sub-Frac spur. So the direction in which PLLatinum sim tool predicts is matching with the silicon.

Two Examples of Second Order versus Third Order and Spur Optimization

Example 1

The following list of figures shows second versus third order and spur optimization at 6.42GHz:

- [Figure 10](#)
- [Figure 11](#)
- [Figure 12](#)
- [Figure 13](#)

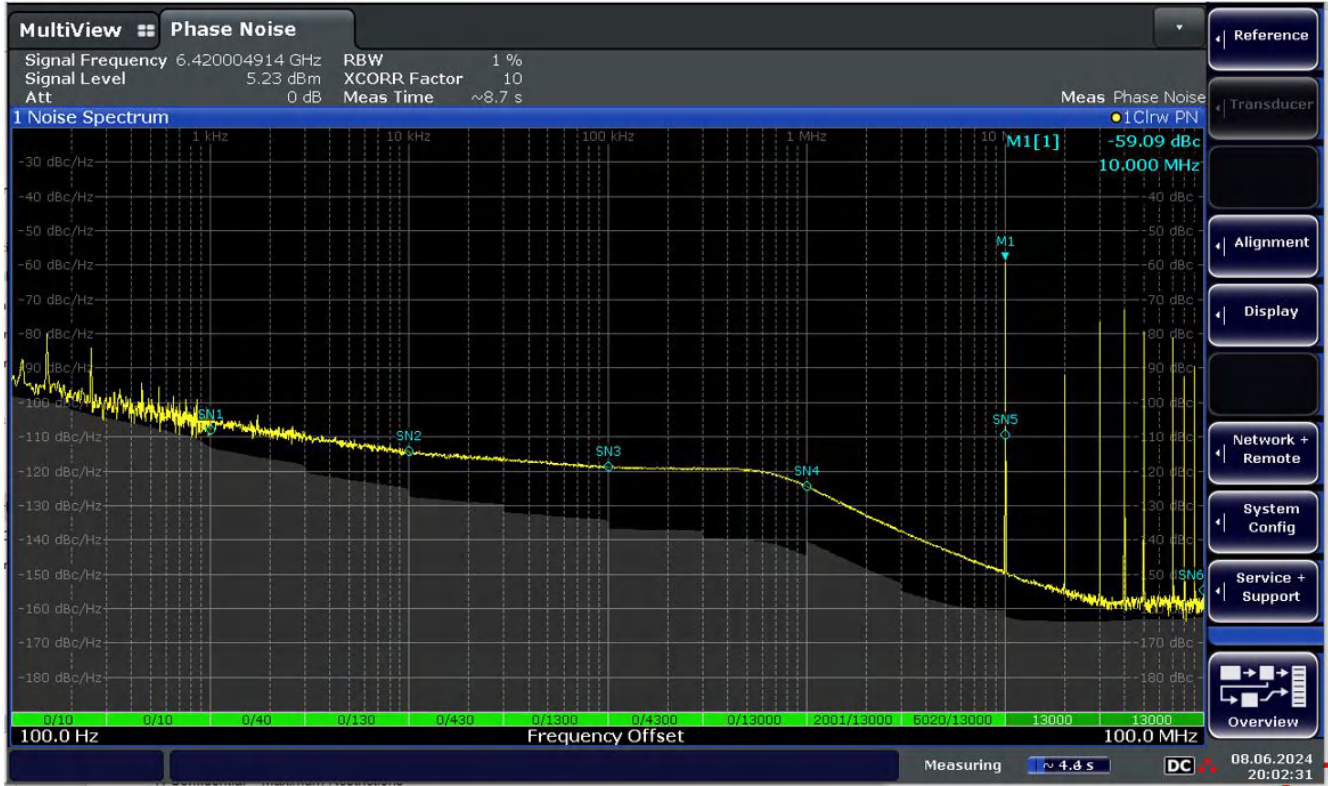


Figure 10. Second Order (Silicon PN Plot)

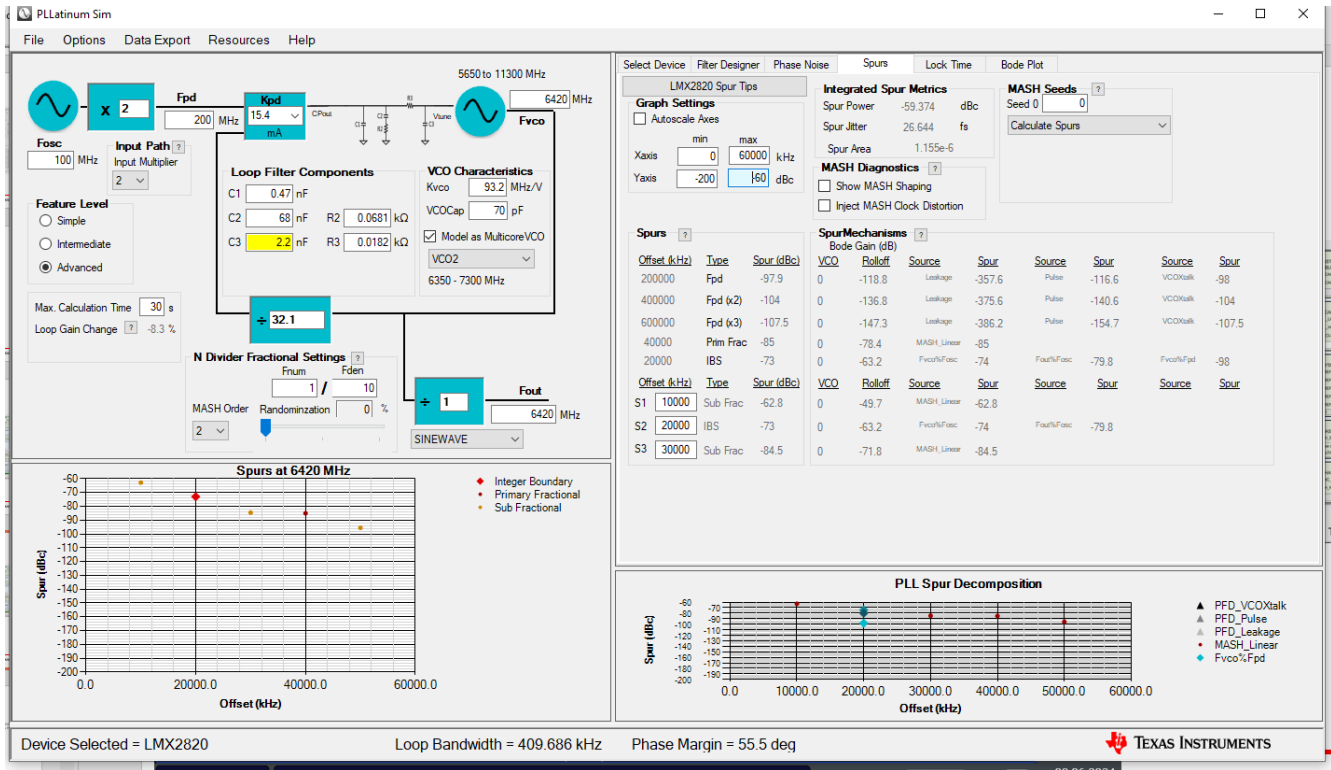


Figure 11. Second Order (PLLatinum sim Setting Snapshot)



Figure 12. Third Order (Silicon PN Plot)

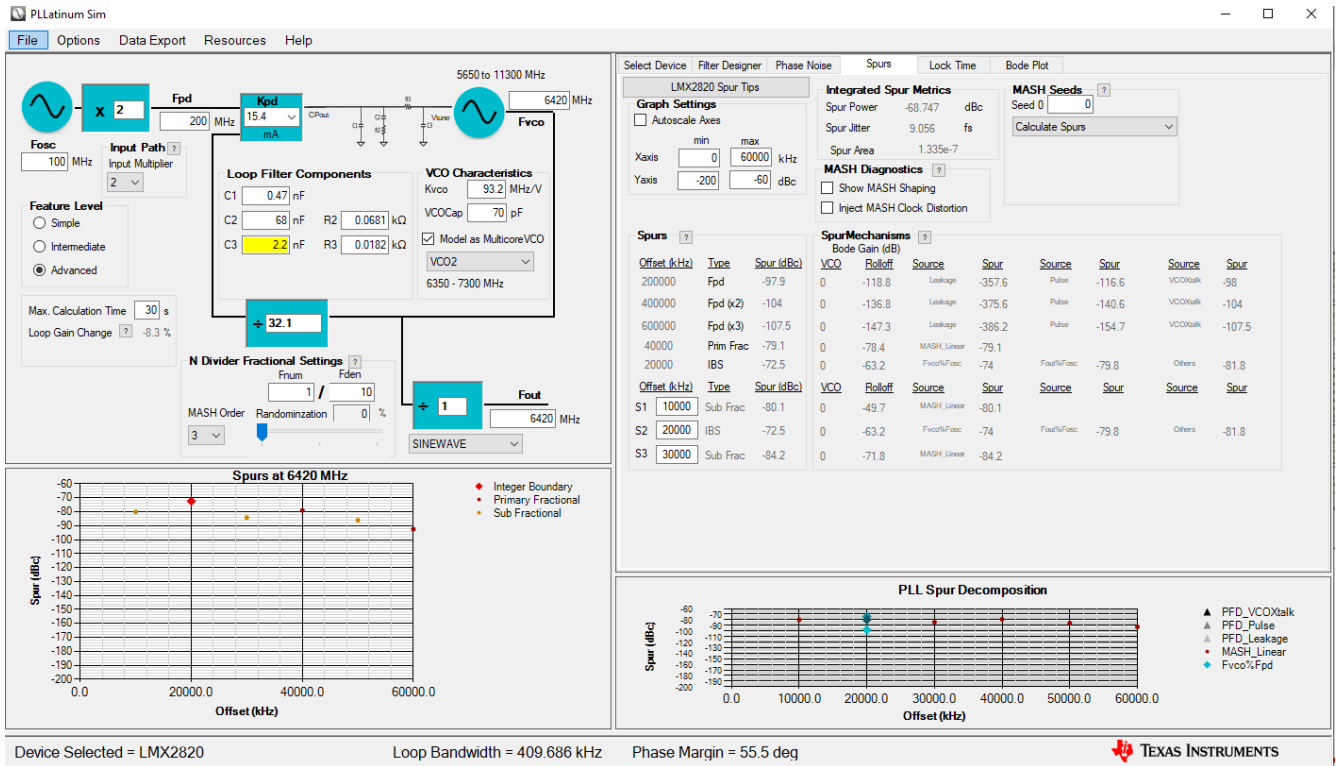


Figure 13. Third Order (PLLatinum sim Setting Snapshot)

Third order MASH can improve spurs over second order MASH as shown in Figure 10 and Figure 12. PLLatinum sim predicted a Sub-Frac spur at 10MHz magnitude reduction from -62.8dBc/Hz to -80dBc/Hz (change of 17.2dBc/Hz) when MASH_ORDER is changed from second to third order. Silicon is showing a change from -59dBc/Hz to -73dBc/Hz(change of 14dBc/Hz).

Another option to reduce the spur is to reduce the gain from the charge pump. Lets see in the PLLatinum sim tool how the roll-off at these offsets look when charge pum gain is changed from 15.4mA to 4.2mA.

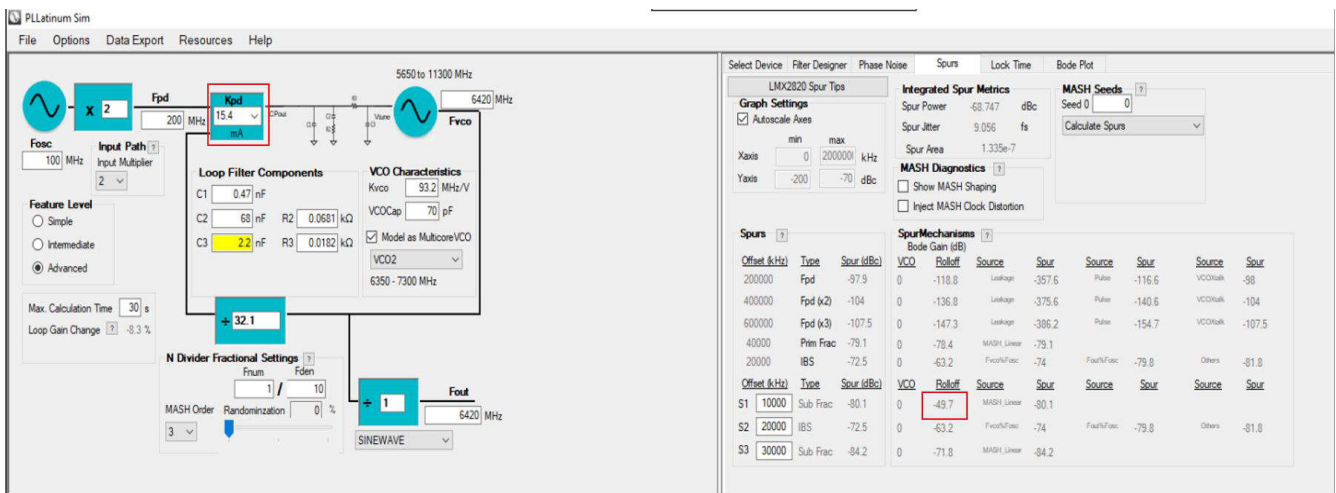


Figure 14. Roll-off value at 10MHz offset with Charge pump gain of 15.4mA

Figure 14 and Figure 15 shows the roll-off variation due to charge pump gain.

There is ≈ 11 dB variation in the roll-off (10MHz offset) from the PLLatinum sim tool. Figure 16 shows the silicon result with charge pump gained reduced to 4.2mA. Comparing Sub-Frac spur (10MHz) between Figure 16

(-74dBc/Hz) and Figure 12(-84dBc/Hz), there is close to 10dBc/Hz variation. This closely matches with the PLLatinum sim tool prediction.

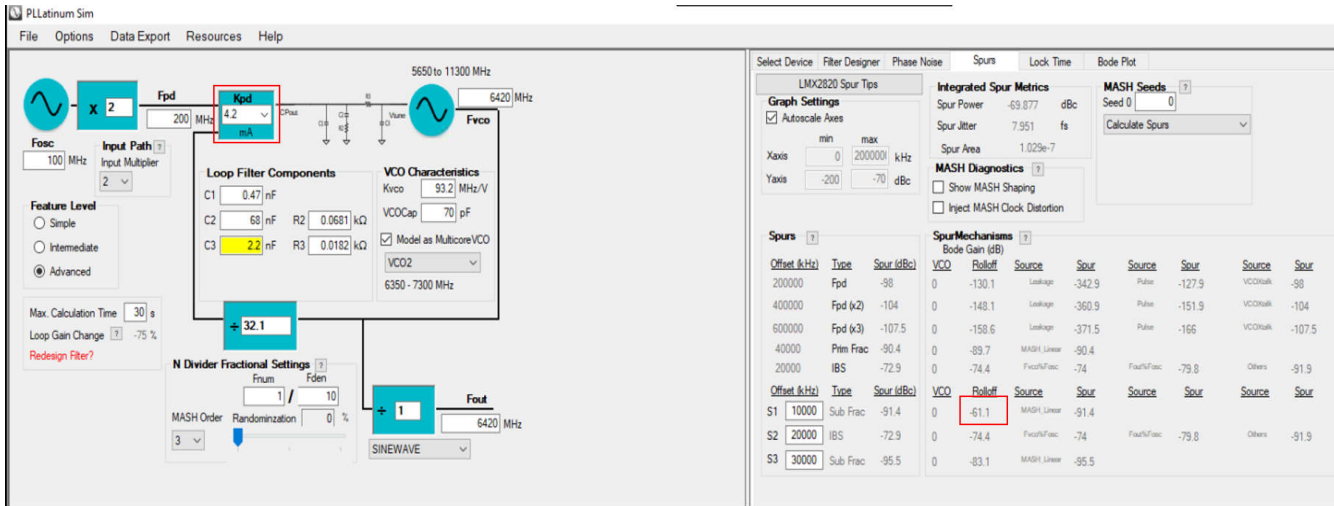


Figure 15. Roll-Off Value at 10MHz Offset With Charge Pump Gain of 4.2mA



Figure 16. Third Order (Silicon PN Plot) With Charge Pump Gain Reduced

Example 2 (6.02GHz)

The following Figure 17 and Figure 19 show the silicon plots comparison for second versus third order and spur optimization at 6.02GHz.

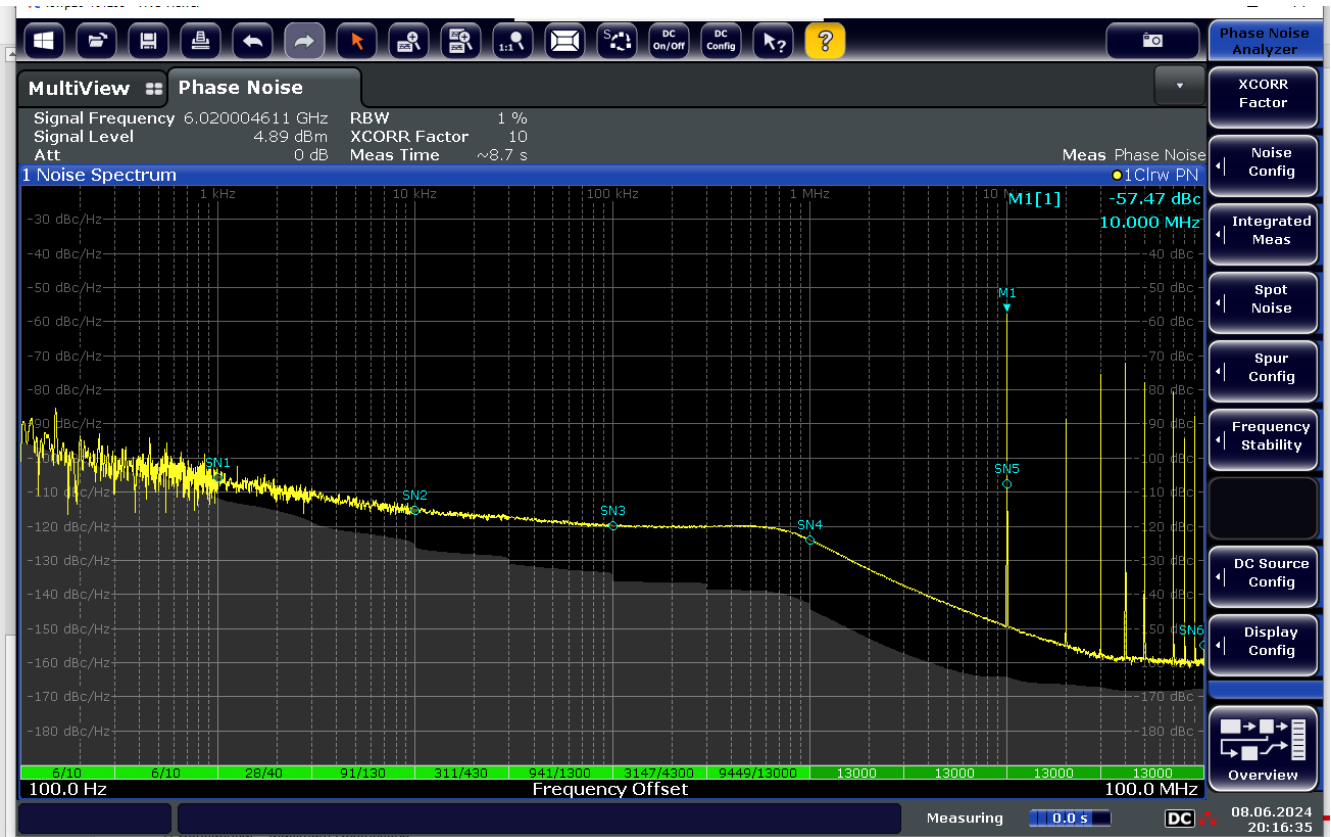


Figure 17. Second Order MASH (Silicon PN Plot)

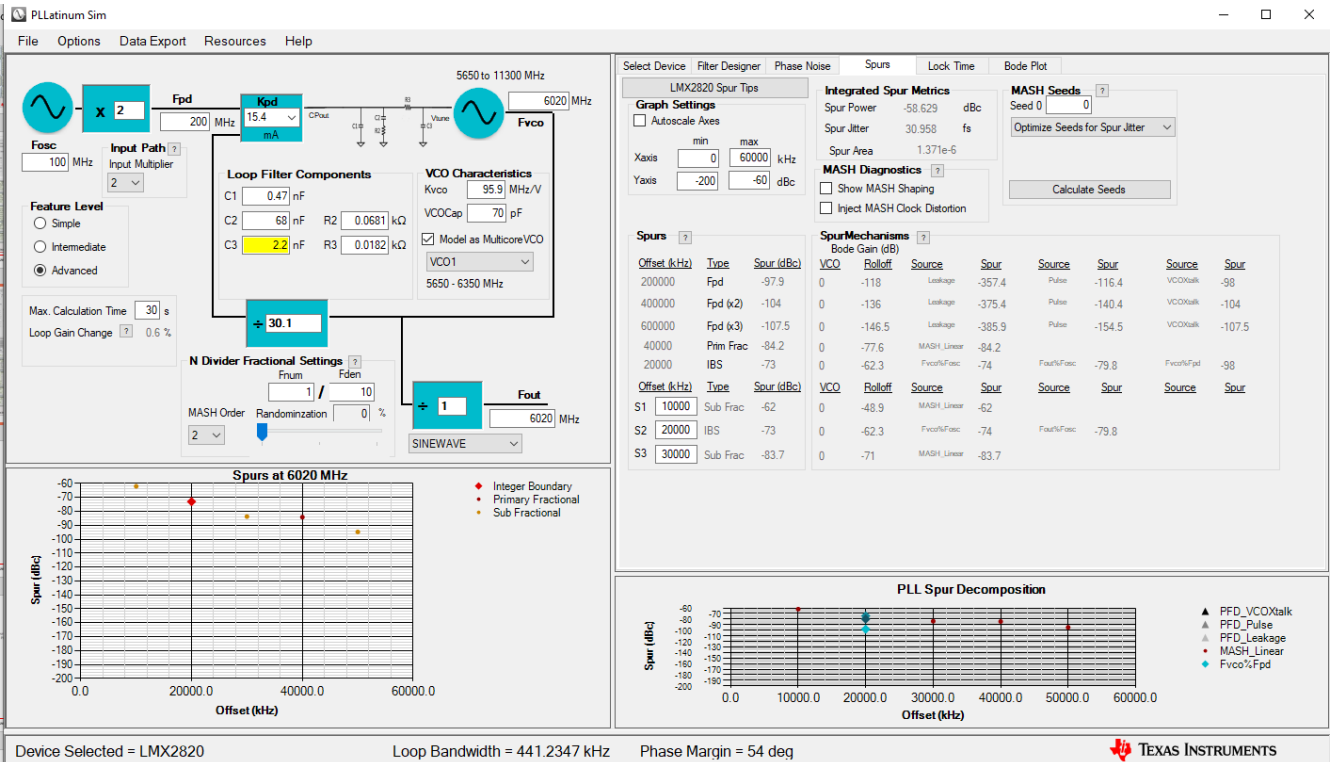


Figure 18. Second Order MASH (PLLatinum sim Setting Snapshot)

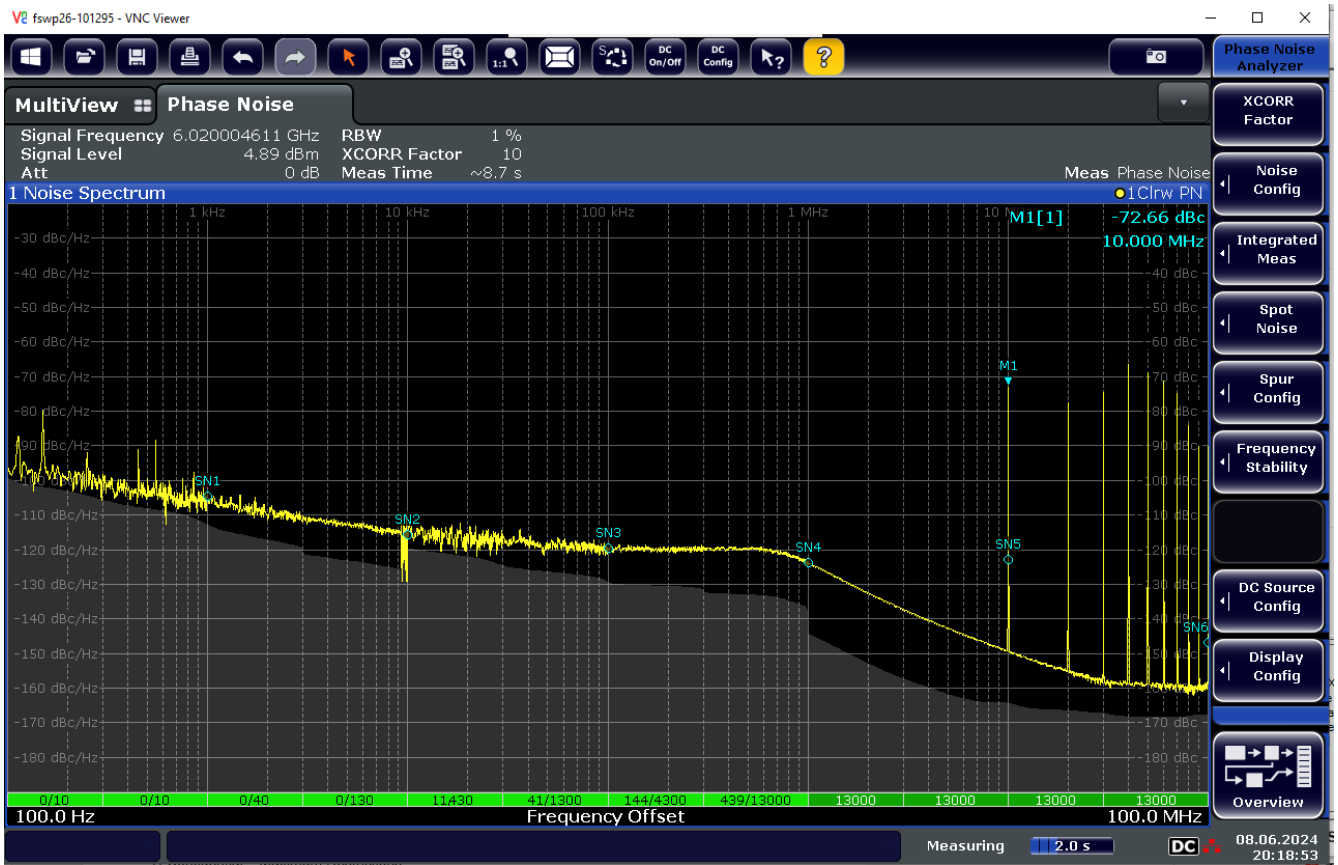


Figure 19. Third Order MASH (Silicon PN Plot)

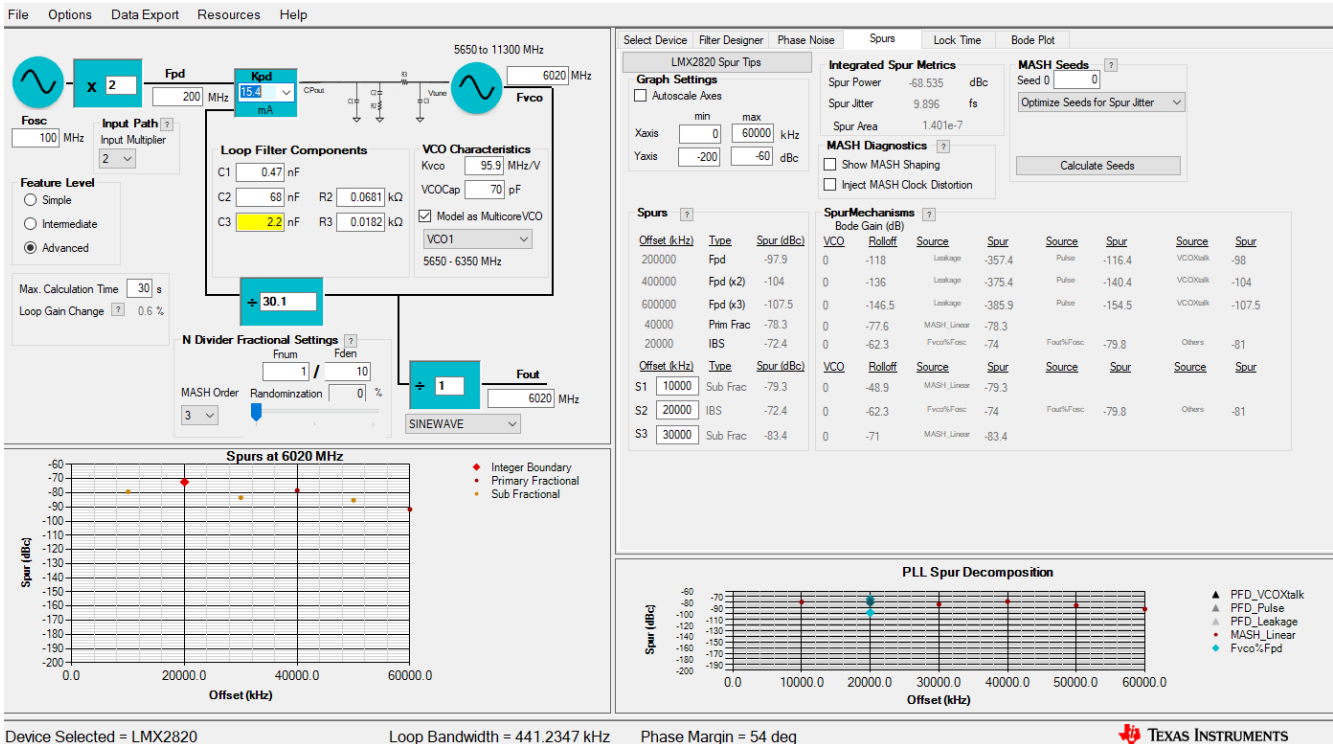


Figure 20. Third Order (PLLatinum sim Setting Snapshot)

For example 2, when MASH_ORDER is moved from second to third order, the PLLatinum sim tool (Figure 18 and Figure 20) predict a spur magnitude change of ≈ 17 dBc/Hz (-62 dBc/Hz to -79.3 dBc/Hz) for the Sub-Frac spur at 10 kHz. Silicon shows a spur magnitude change of -15 dBc/Hz (-57.47 dBc/Hz to -72.66 dBc/Hz).

Gain from the charge pump is reduced to 4.2 mA and impact on the phase noise is shown in Figure 21. When this option is exercised, make sure that the phase margin is greater than 45 degrees.



Figure 21. Third Order MASH (Silicon PN Plot) With Charge Pump Gain Reduced

There is another way to reduce the spurs as shown in Figure 22. Using a larger nonequivalent fraction is an effective way to reduce spurs. Compared to Figure 21, the magnitude of the spur is less in Figure 22.



Figure 22. Third Order MASH (Silicon PN Plot) With Charge Pump Gain Reduced and Slight Change in Fraction

In the third order, the denominator is offset by 1, as shown in Figure 23.

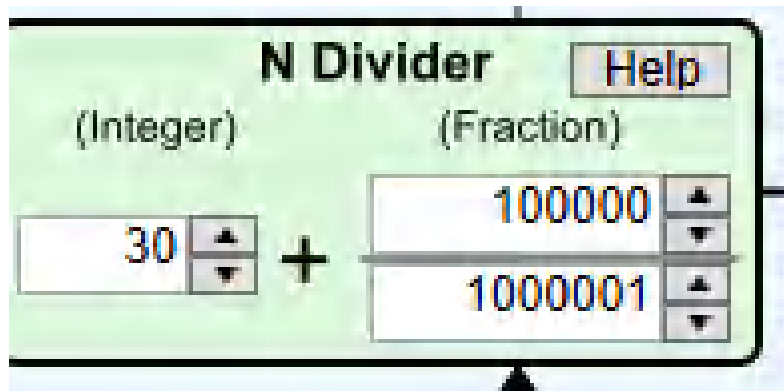


Figure 23. Fraction Change Settings

Another example for the slight change in denominator impact on the spurs:

1. PLL_NUM/PLL_DEN = 1510000/36000000 and then set MASH_SEED = 1
2. PLL_NUM/PLL_DEN = 1510000/36000001 and then set MASH_SEED = 0

Following Figure 24, Figure 25, Figure 26 shows the phase noise plots for the cases shown above. Offsetting the denominator by 1, gives better improvement compared to without offset and MASH_SEED as 1.

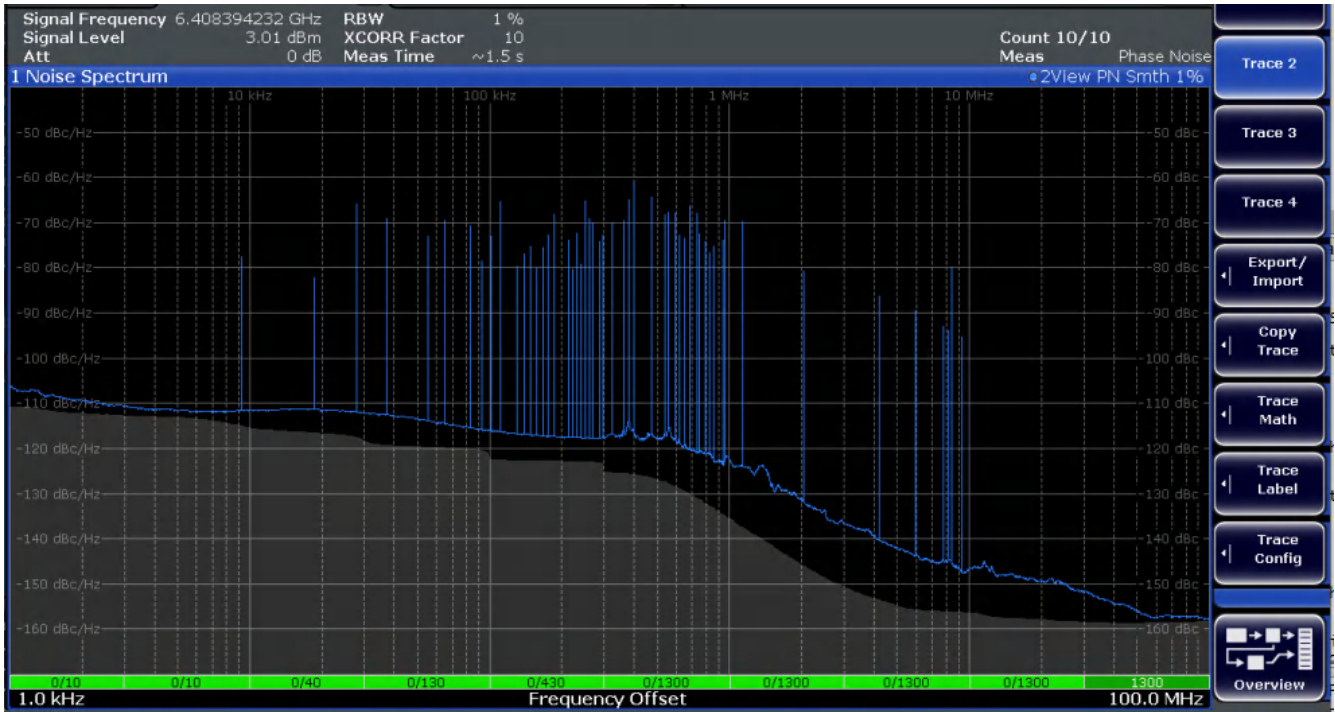


Figure 24. 3rd Order With MASH_SEED As 0 and PLL_NUM/PLL_DEN = 151000/3600000

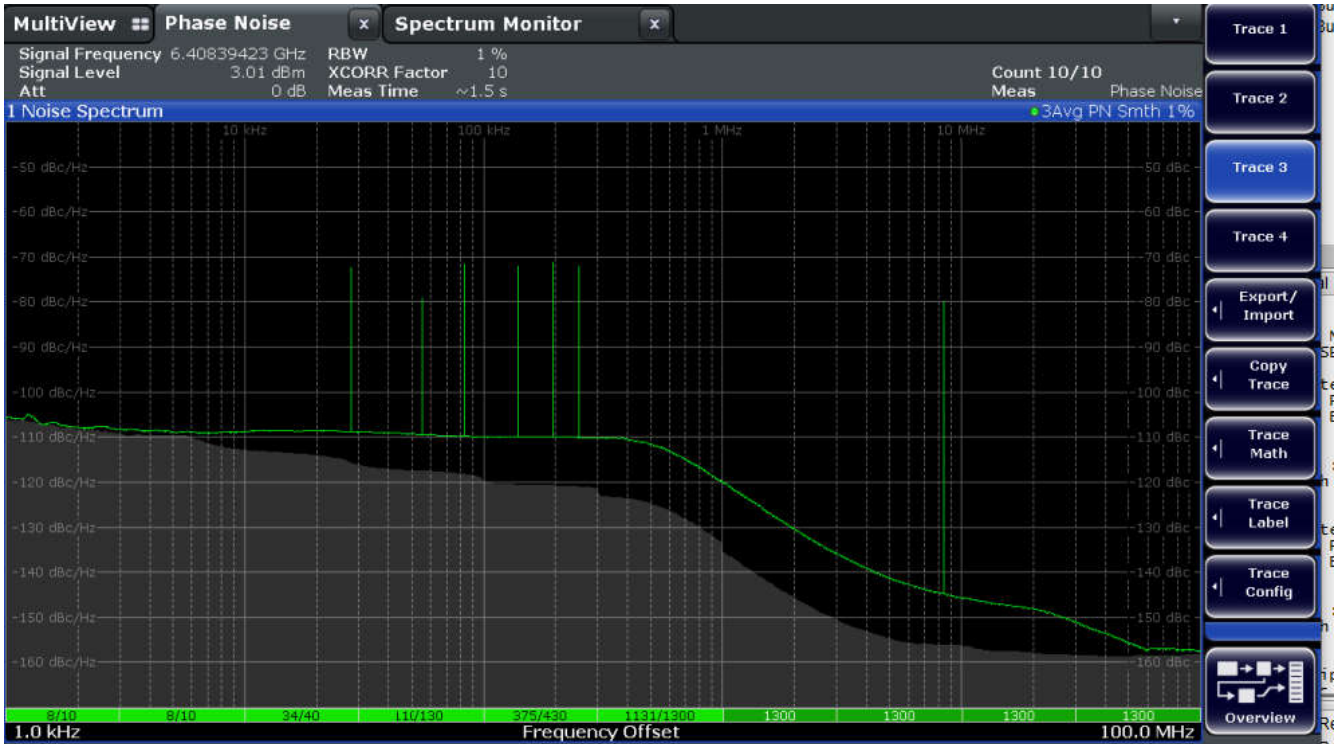


Figure 25. 3rd Order With MASH_SEED As 1 and PLL_NUM/PLL_DEN = 151000/3600000

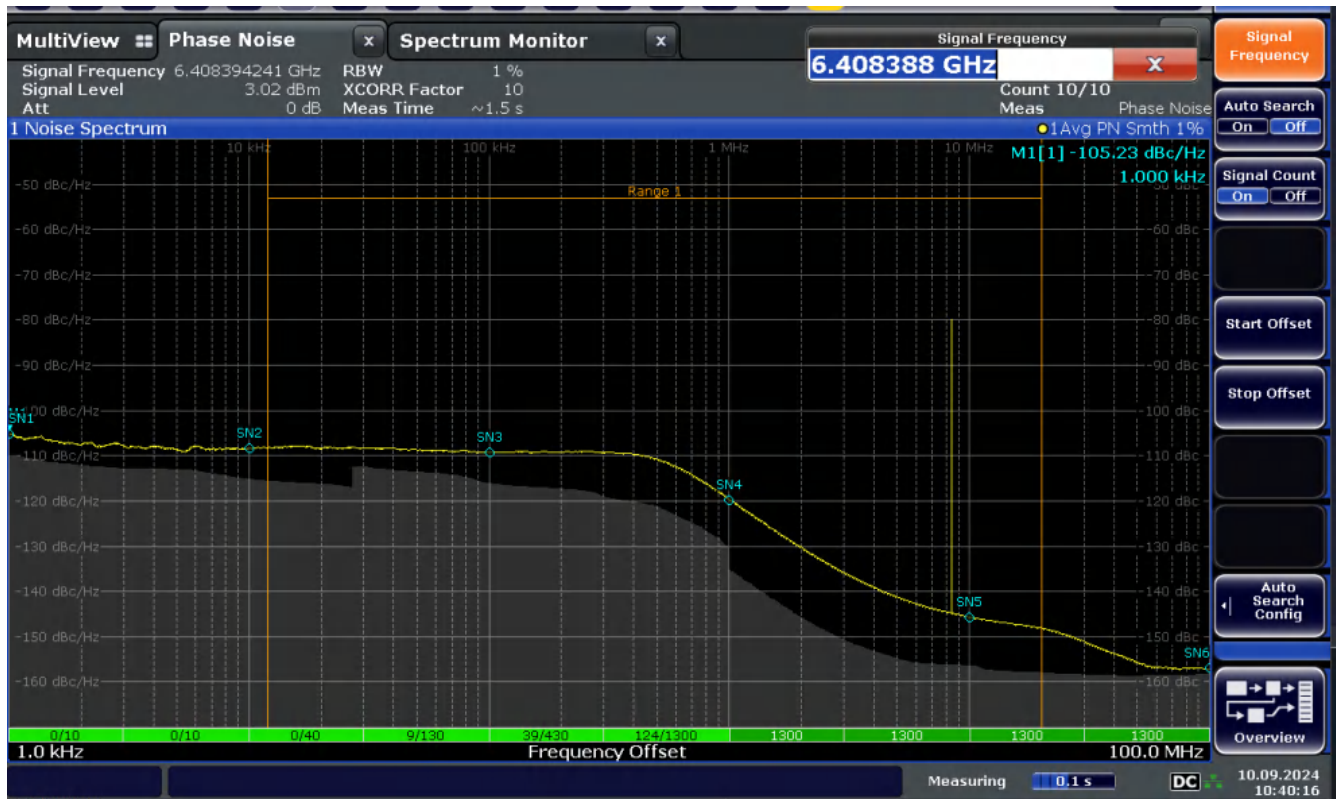


Figure 26. 3rd Order With MASH_SEED As 0 and PLL_NUM/PLL_DEN = 1510000/36000001

Using a large nonequivalent fraction is effective way to reduce spurs. If the user does not want an the inexact output frequency, use MASH_SEED = 1, however MASH_SEED = 1 is not as effective as the larger, nonequivalent fraction.

Points to note when changing MASH_SEED:

1. For purposes of spur reduction, there is no point in making the Seed any larger than (PLL_DEN) - 1
 - a. If MASH_SEED is a multiple of PLL_DEN, the MASH_SEED is the same as MASH_SEED = 0, for example if PLL_DEN = 10 and MASH_SEED = 100, there is no impact
 - b. Impact of MASH_SEED Mod PLL_DEN. For instance, if the fraction is 3/10, then MASH_SEED = 1, 11, 21, 31, ... 10n+1, ... all have the same impact
2. Simplify fractions if MASH_SEED = 0
 - a. Fraction (PLL_NUM/PLL_DEN) of 10/100 has the same spectrum as 1/10 if MASH_SEED = 0, but not if MASH_SEED=1

More Spur Optimization Options

Use predividers and a multiplier in the reference path to change the spur offset location.

Additional Resources

- Texas Instruments, [Timing Is Everything: Improving Integer Boundary Spurs in Fractional PLL Synthesizers](#), technical article
- Dean Banerjee, [PLL Performance, Simulation, and Design, 5th Edition](#), Chapters 20 and 21
- Texas Instruments, [PLLATINUMSIM-SW simulator tool](#), software support

Trademarks

All trademarks are the property of their respective owners.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated