Literature Number: SNAP002

PLL Fundamentals

Part 2: PLL Behavior

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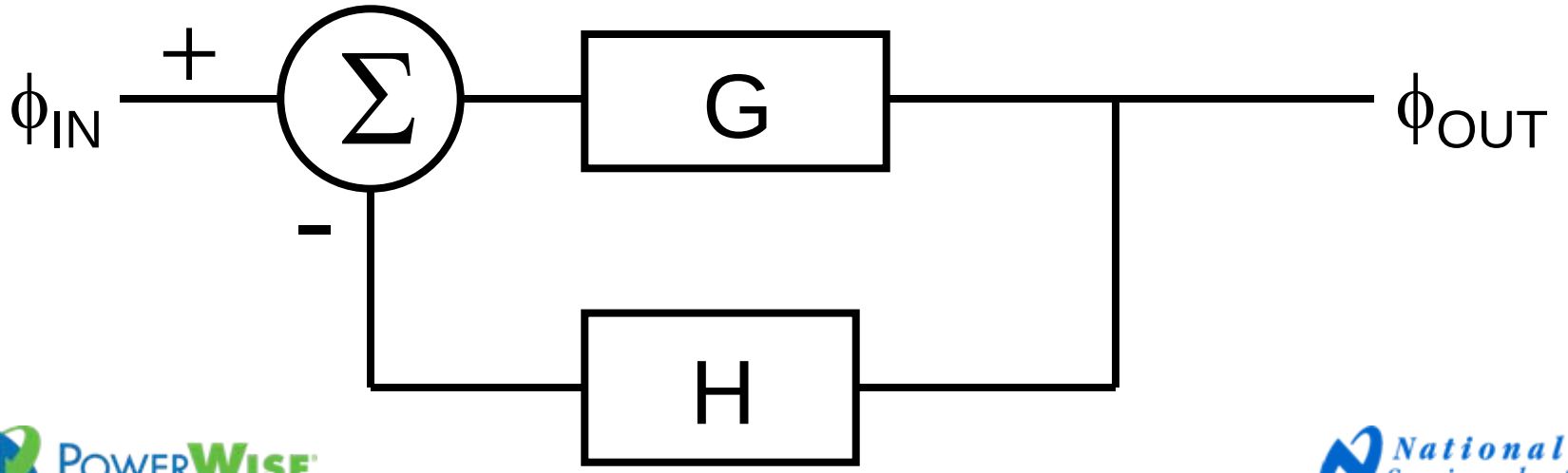
Overview

- General PLL Performance Concepts
  - PLL Loop Theory
  - Lock Time
  - Spurs
  - Phase Noise
- Fractional PLL Performance Concepts
  - Generation of Fractional N Value
  - Fractional N Phase Noise
  - Fractional N Spurs

Notes

Derivation of Noise Transfer Functions

- **G = Kϕ●(Kvco/s)●Z(s)**
  - Kϕ = Charge Pump Gain
  - Kvco = VCO Gain
  - Z(s) = Transfer function of the loop filter
  - Note that G is a DECREASING function in s = j●ω
- **H = 1/N**
  - Note that H is a CONSTANT with respect to s = j●ω
- **Transfer functions apply to both phase and frequency**



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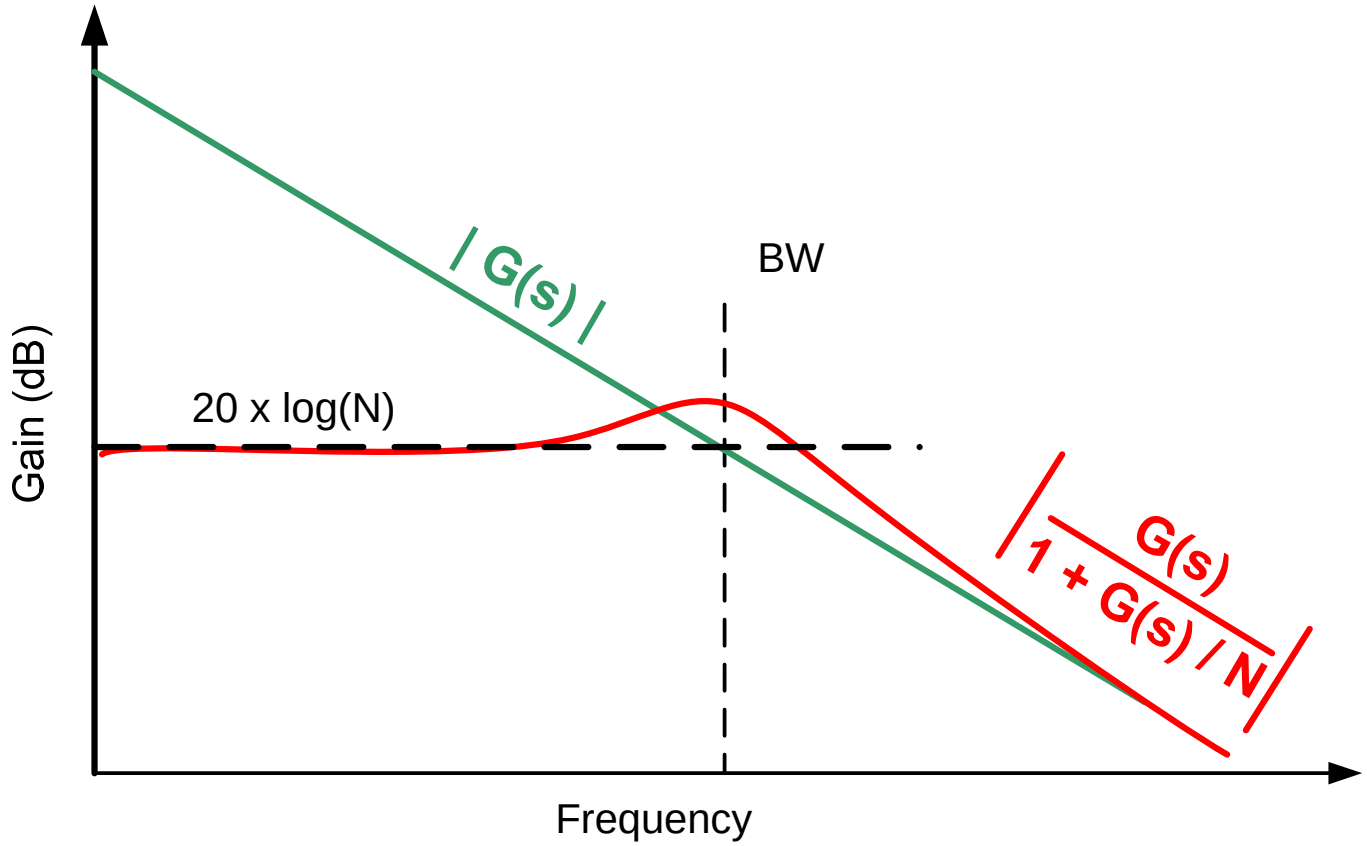
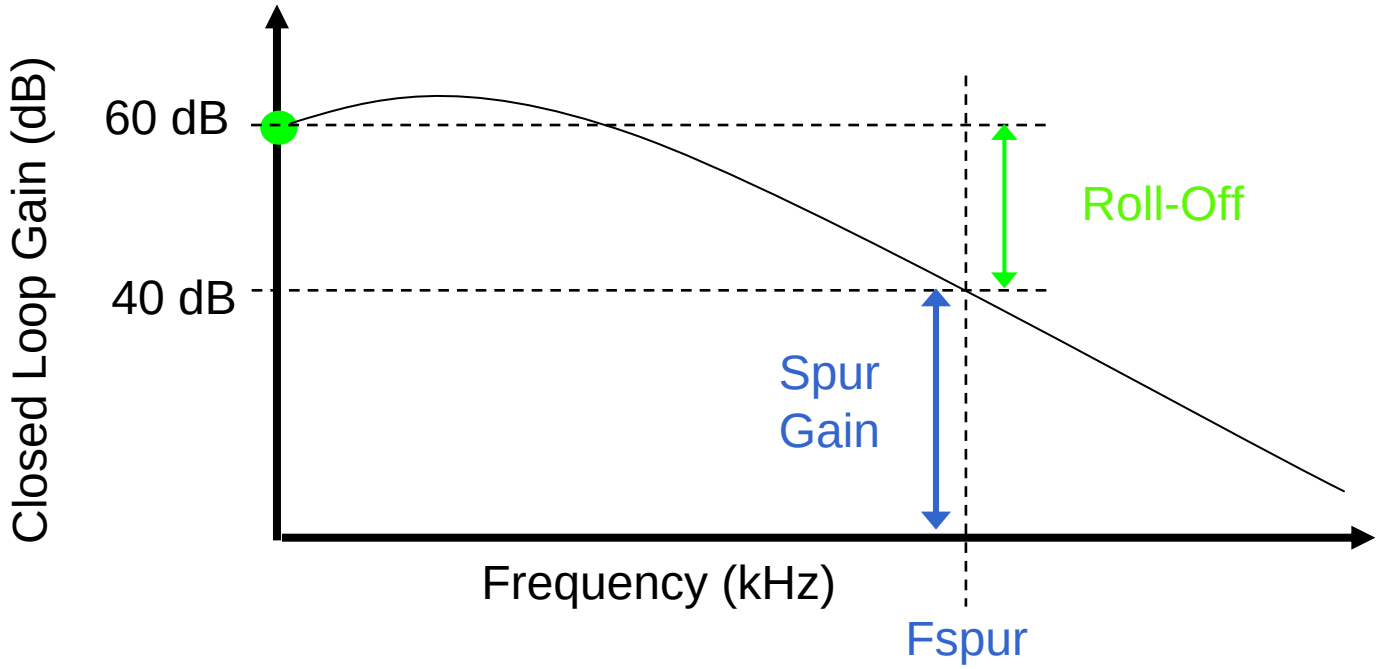
Analysis of Transfer Functions



Closed Loop Gain



- **Spur Gain Applies more to Integer PLL Phase Noise and Spurs**
- **Roll-Off Applies more to fractional PLL Phase Noise and Spurs**

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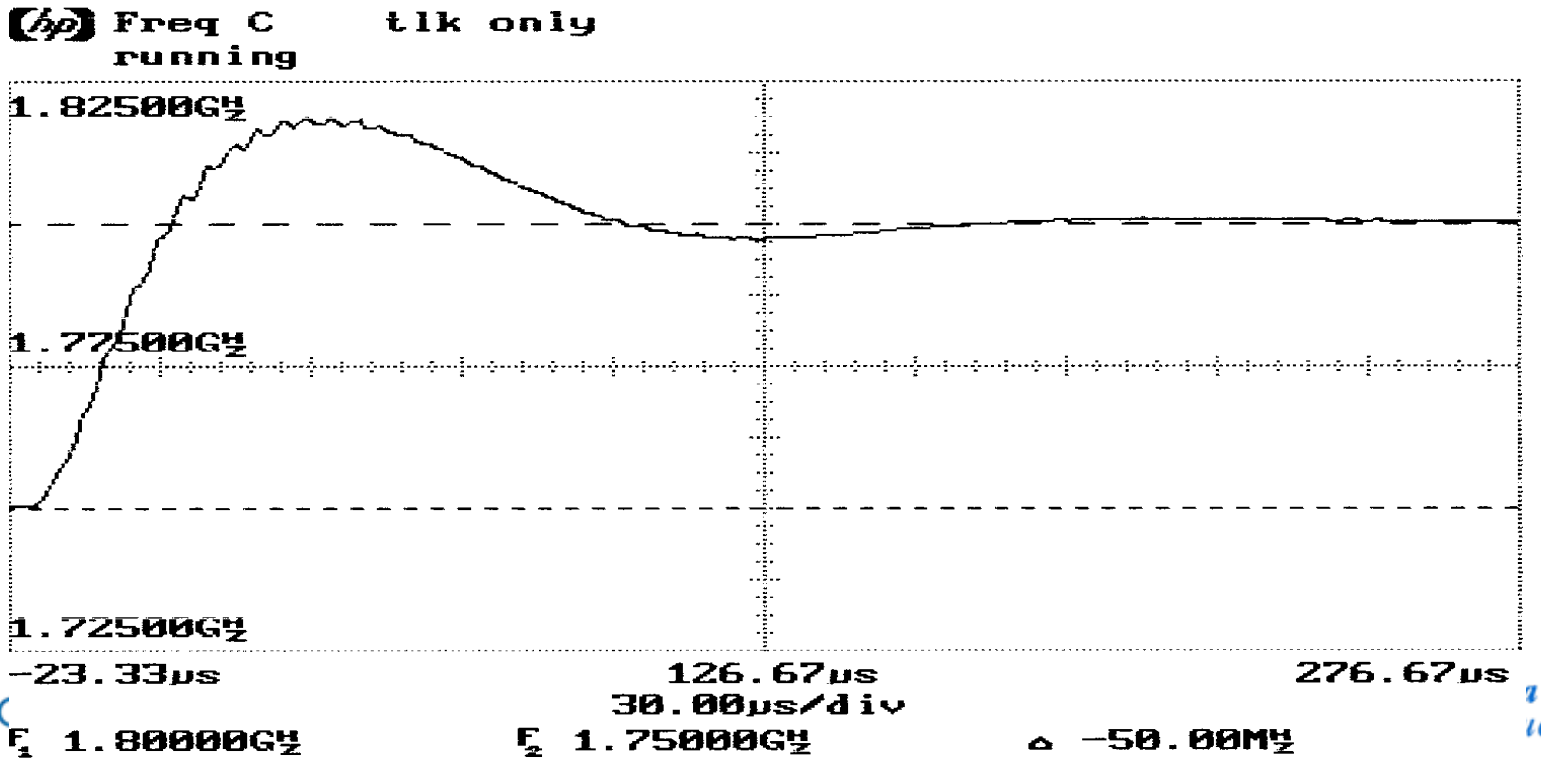
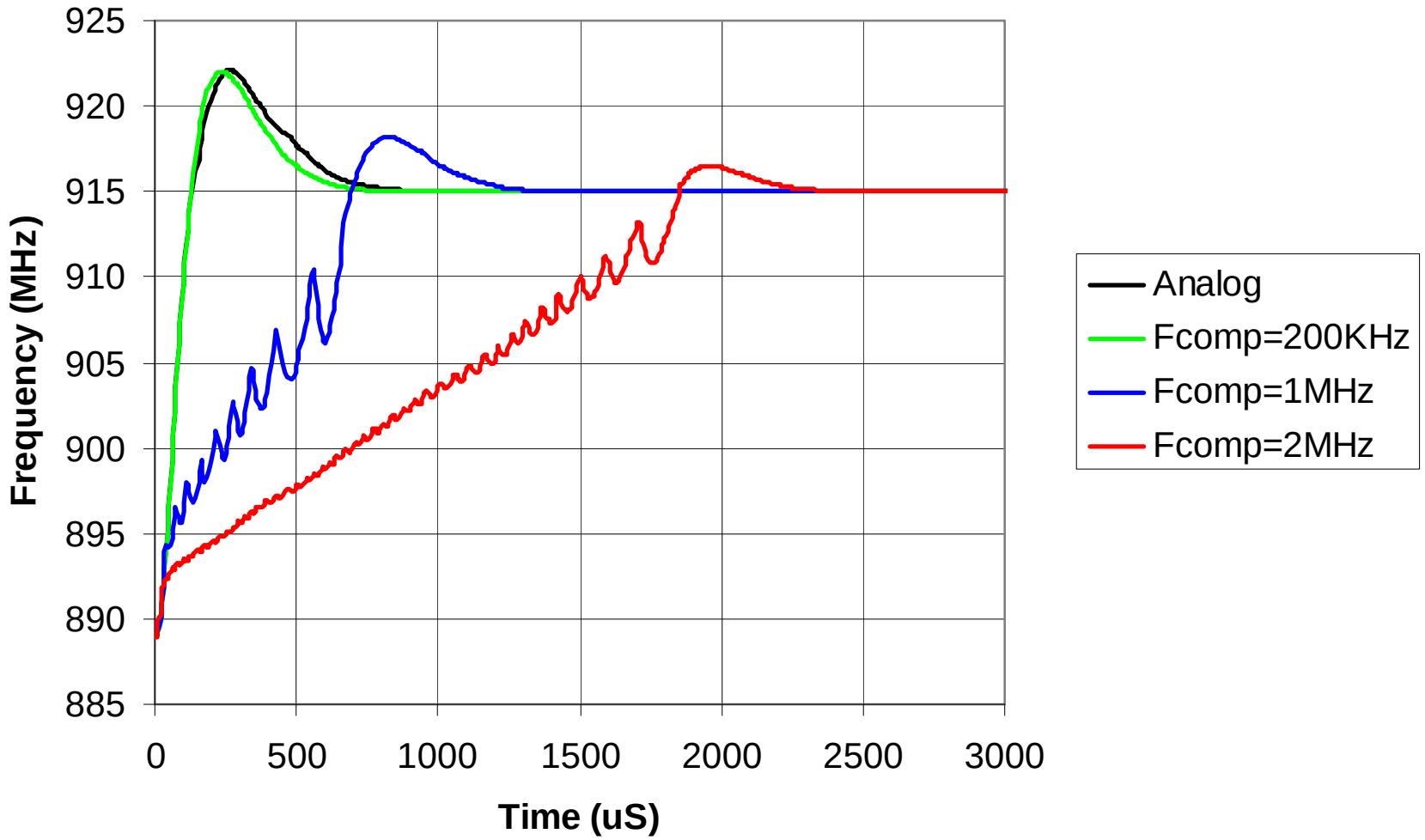
Lock Time

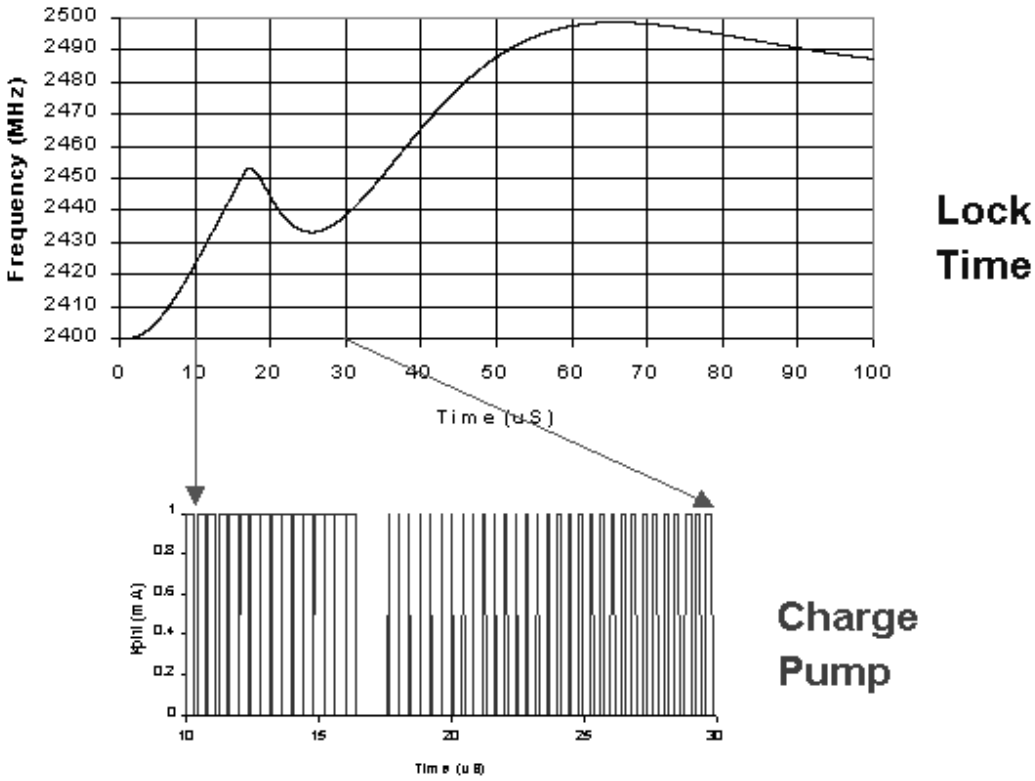
- **Indicates the time it takes from an initial to within a tolerance of a final frequency.**
  - **Depends mainly on Loop Bandwidth**
  - **Depends on size of frequency switch**



The Impact of Cycle Slipping

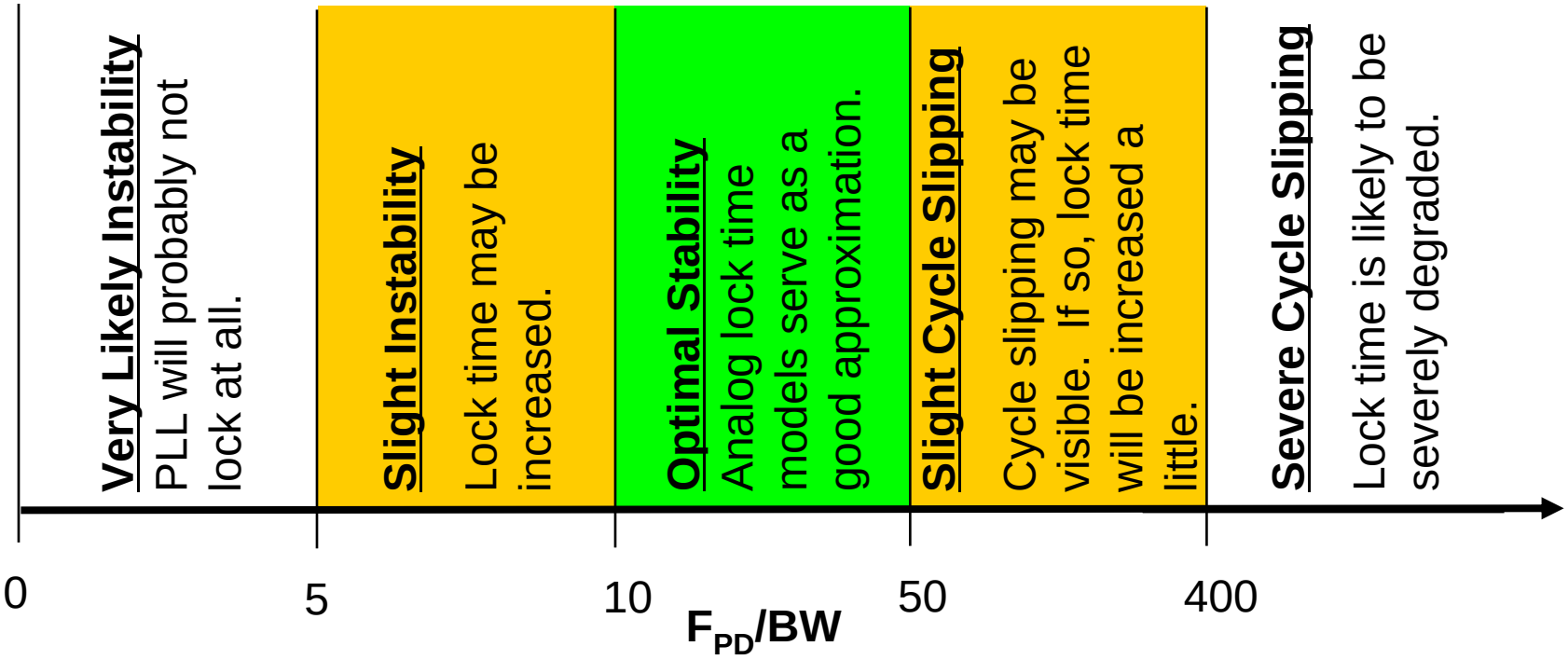


The Anatomy of a Cycle Slip



- **Cycle slip is caused when the phase detector is off by 1 cycle**
- **Voltage is produced across loop filter resistor R2, which causes the glitch**

Impact of f_{PD}/BW Ratio on Cycle Slipping



- **Discrete sampling action of phase detector impacts lock time**
- **f_{PD}/BW**
  - **Ratio of phase detector frequency to loop bandwidth**
  - **As the ratio gets smaller, instability increases**
  - **As the ratio gets larger, cycle slipping increases**

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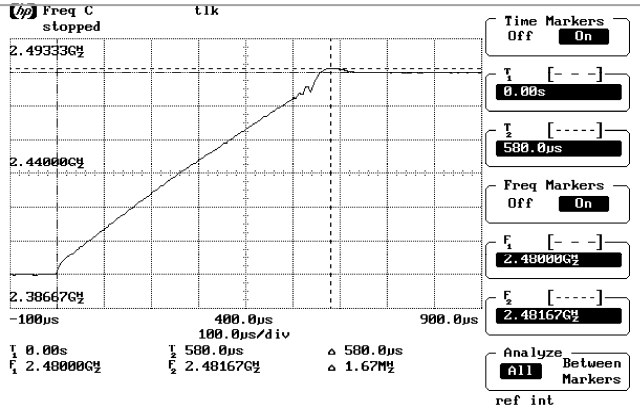
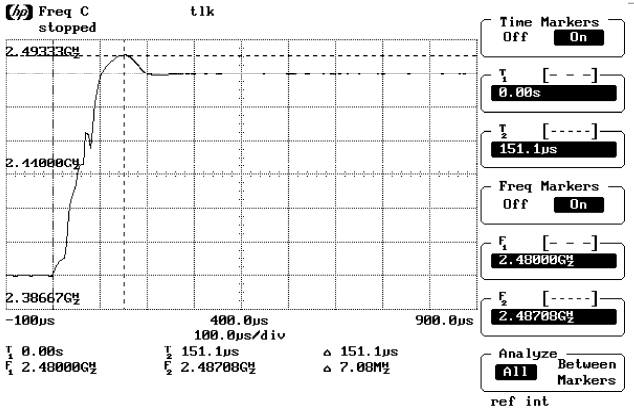
LMX2485 Cycle Slip Reduction Technique



No Cycle Slip Reduction

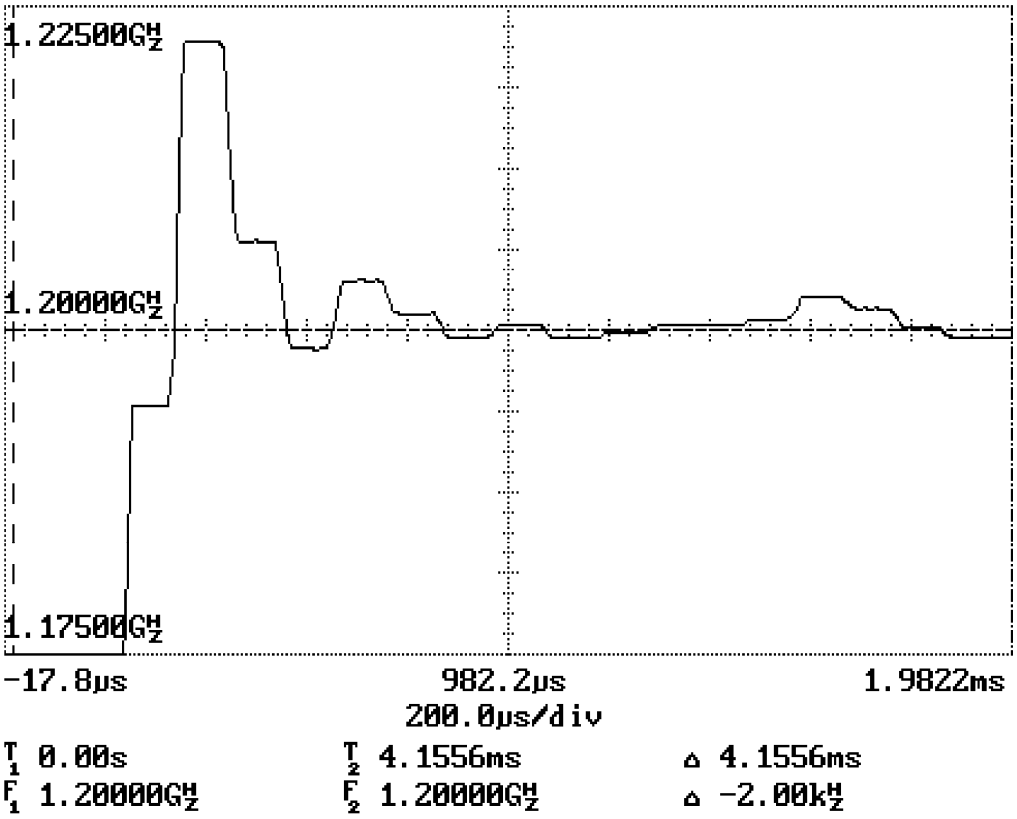
- Peak Time = 561 uS
- Lock Time = 834 uS



With Cycle Slip Reduction

- Peak Time = 151 uS
- Lock Time = 486 uS

LMX2531/LMX2541 VCO Tuning Algorithm Reduces Cycle Slipping



- **Calibration gets VCO Close (5-30 MHz) to final frequency**
- **Cycle Slipping is dependent on the side of the frequency change**

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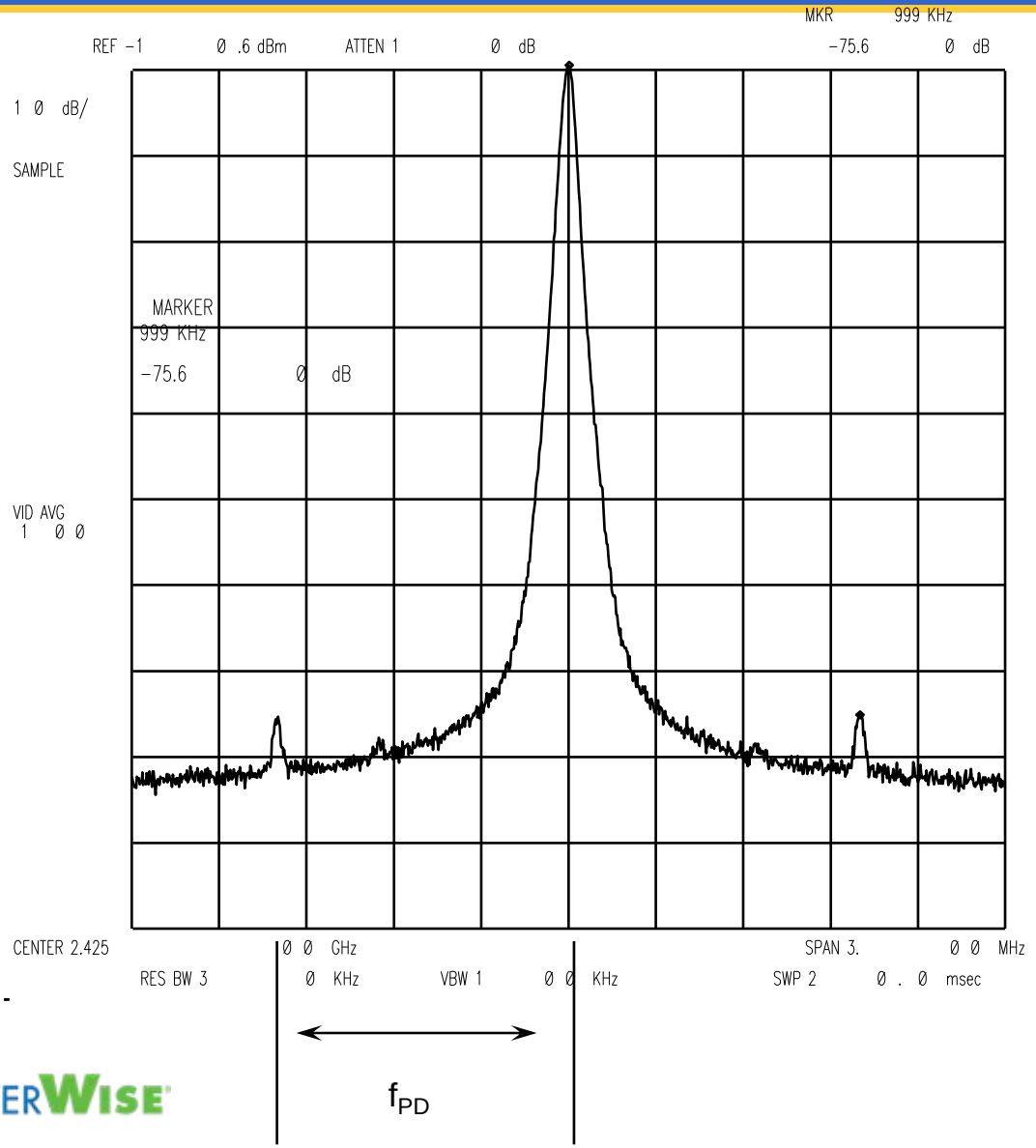
Reference Spurs

- **Undesired Spurious outputs that appear at a spacing of F_{PD} from the carrier**
- **VCO Tuning Voltage has small AC component**
  - Caused by leakage of the charge pump
  - Caused by mismatched currents of the charge pump
  - Smaller for narrower loop bandwidths
  - Smaller for larger comparison frequencies due to more filtering
- **This AC Voltage causes frequency spurs**
- **By making the Comparison Frequency Larger, thus making N smaller, these spurs are filtered out more**

Reference Spur Example



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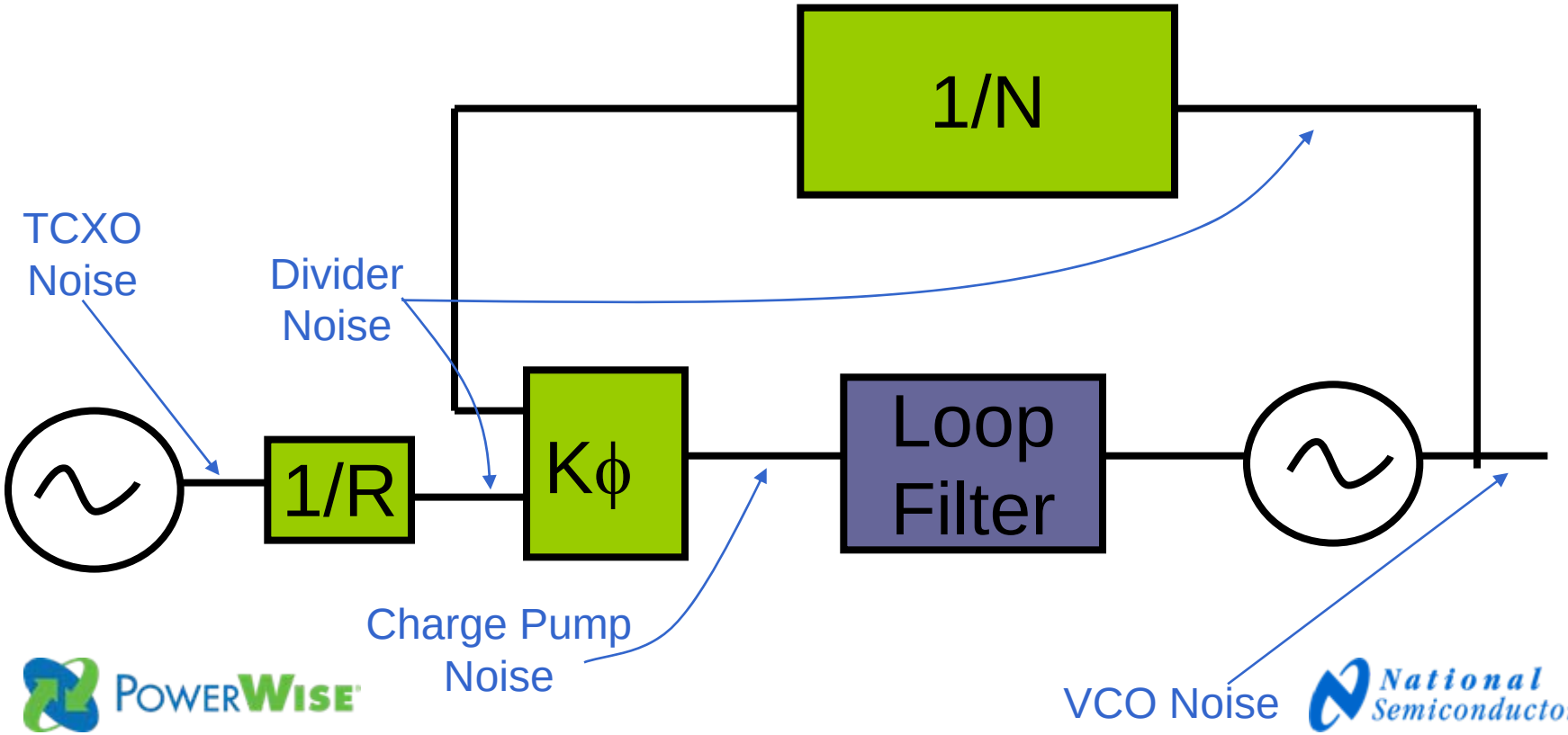
PLL Noise Sources

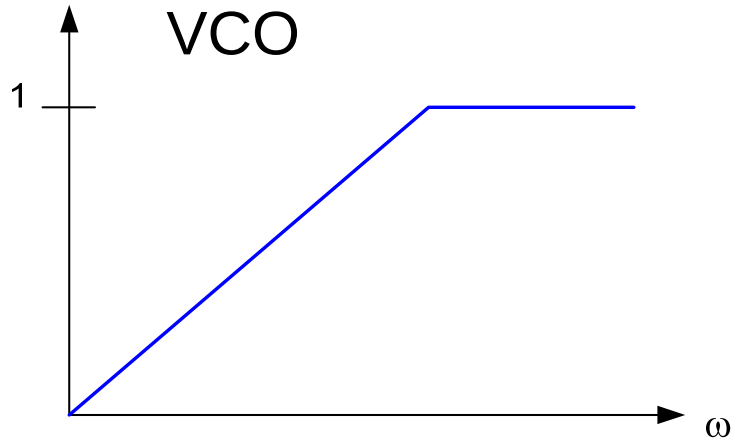
- **VCO Noise is high pass filtered**
- **All other noise sources are multiplied by N and low pass filtered**
- **Charge Pump Noise and VCO Noise tend to dominate**

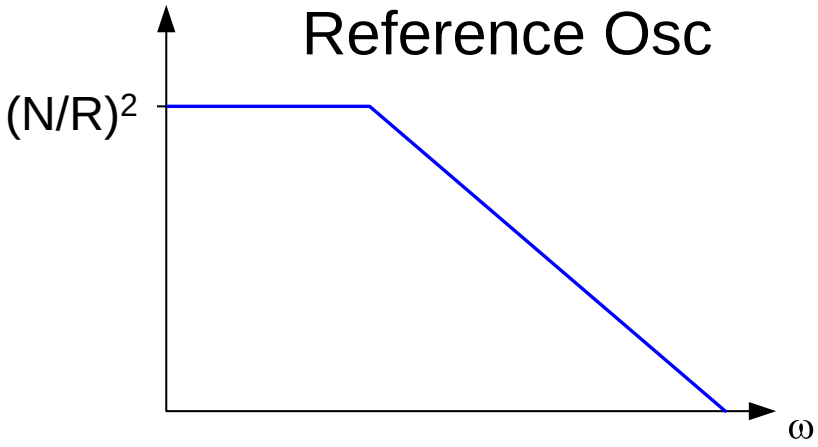


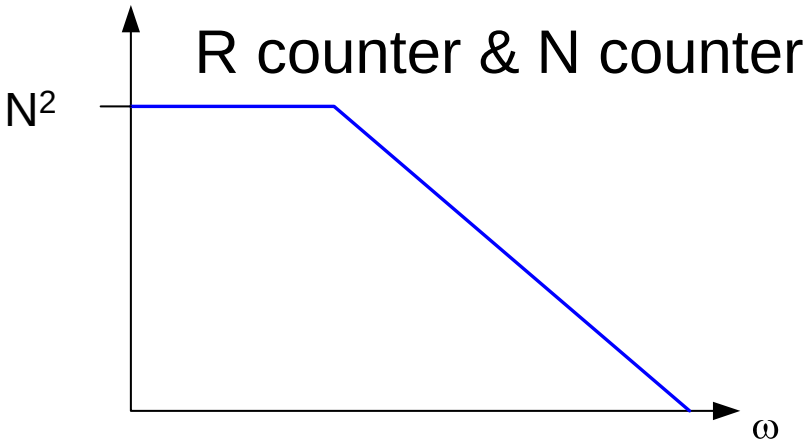
Noise Transfer Functions

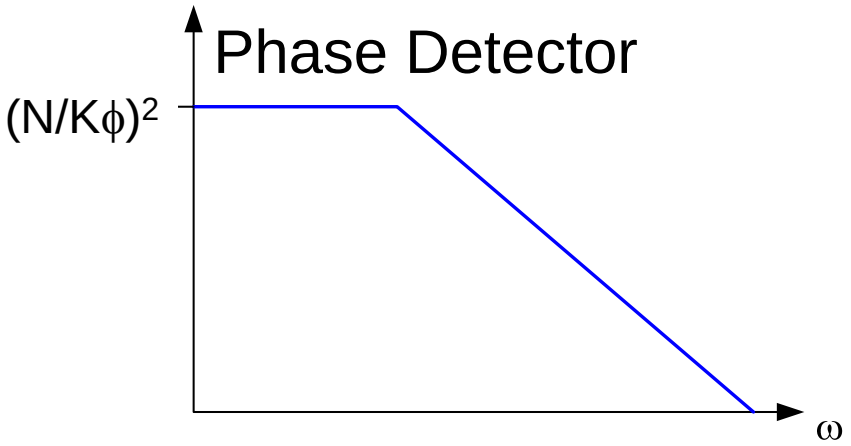
Source	Transfer Function	Low Freq. Approx.	High Freq. Approx.	Response Shape
VCO	$\frac{1}{1+\left[G(s)\cdot\frac{1}{N}\right]}$	1/G(s), $\lvert 1/G(s)\rvert^2$	1	Highpass
Reference Oscillator	$\frac{1}{R}\cdot\frac{G(s)}{1+\left[G(s)\cdot\frac{1}{N}\right]}$	N/R, $(N/R)^2$	G(s), $\lvert G(s)\rvert^2$	Lowpass
R counter	$\frac{G(s)}{1+\left[G(s)\cdot\frac{1}{N}\right]}$	N, N^2	G(s), $\lvert G(s)\rvert^2$	Lowpass
N counter	$\frac{G(s)}{1+\left[G(s)\cdot\frac{1}{N}\right]}$	N, N^2	G(s), $\lvert G(s)\rvert^2$	Lowpass
Phase Detector	$\frac{1}{K_\phi}\cdot\frac{G(s)}{1+\left[G(s)\cdot\frac{1}{N}\right]}$	N/K_ϕ, $(N/K_\phi)^2$	G(s), $\lvert G(s)\rvert^2$	Lowpass

Noise Transfer Functions









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1 Hz Normalized Phase Noise

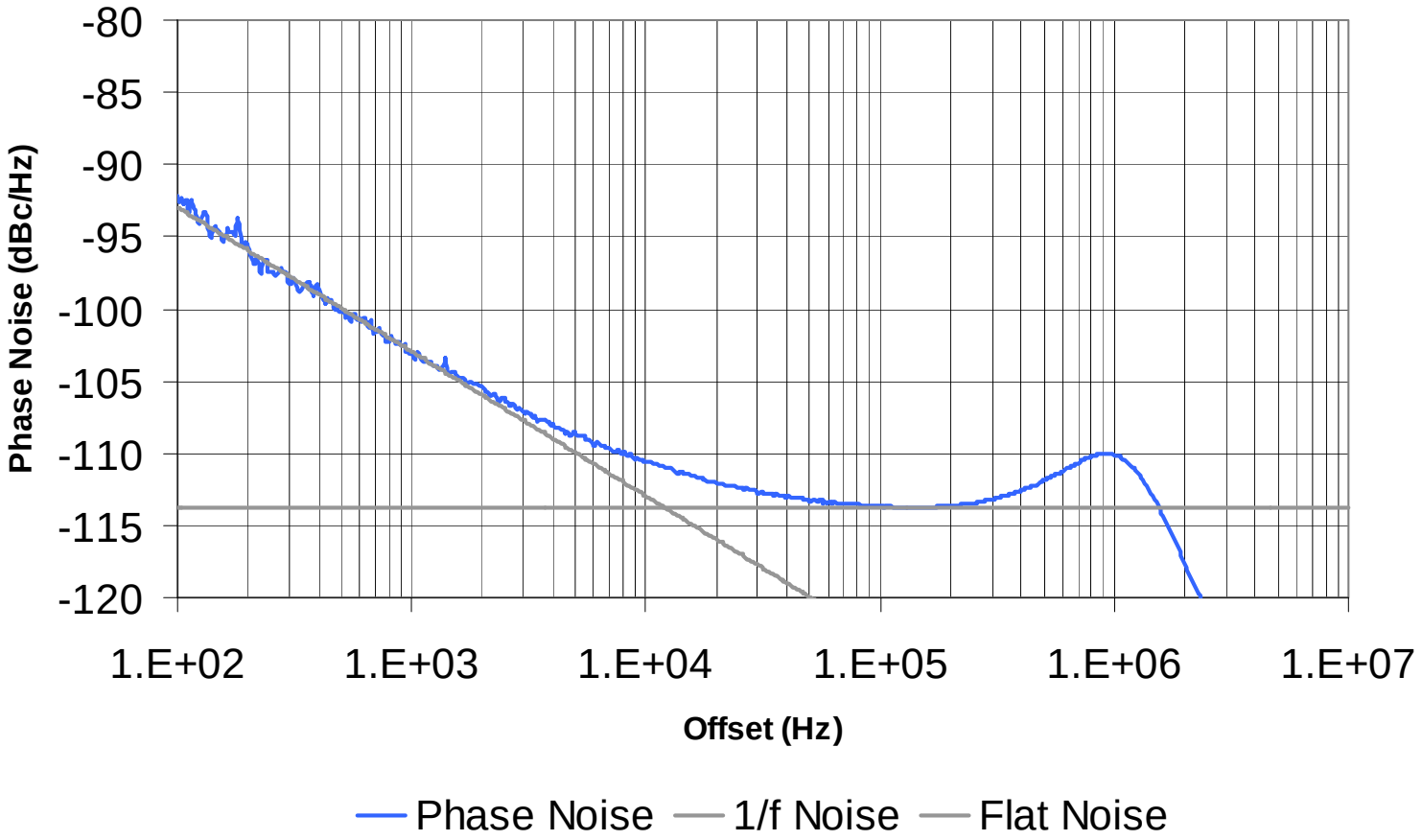
- Good way to characterize the phase noise of a PLL
- Assumes Charge Pump Noise is Dominant
- Number is deceptive for fractional N parts because it does not take into account the phase noise advantage of having a lower N counter.
- PN1Hz = PN – 20•log(N) – 10•log(f_{PD})
  - N = N Counter Value
  - f_{PD} = Phase Detector frequency in Hz
  - PN = Phase Noise
- This number is part specific.
  - LMK03001C = -224 dBc/Hz
  - LMX2485 = -212 dBc/Hz
  - LMX2470/LMX2531= -212 dBc/Hz
  - LMX2541 = -225.4 dBc/Hz

Normalized 1/f Noise

- **This models the close-in phase noise of the PLL**
- **Normalized to a 1 GHz Output Frequency**
- **Normalized to a 10 kHz offse**
- **Important to consider if the comparison frequency is high**
- **Number is deceptive for fractional N parts because it does not take into account the phase noise advantage of having a lower N counter.**
- **PN10kHz = PN(10kHz) – 20●log(Fout/1GHz) – 10●log(10kHz/Offset)**
- **This number is part specific.**
  - **LMK03001C = -122 dBc/Hz**
  - **LMX2485 = -104 dBc/Hz**
  - **LMX2531/LMX2470 = -104 dBc/Hz**
  - **LMX2541 = -124.5 dBc/Hz**

LMX2541 Phase Noise

- **VCO Frequency = 3700 MHz**
- **Phase Detector Frequency = 100 MHz**



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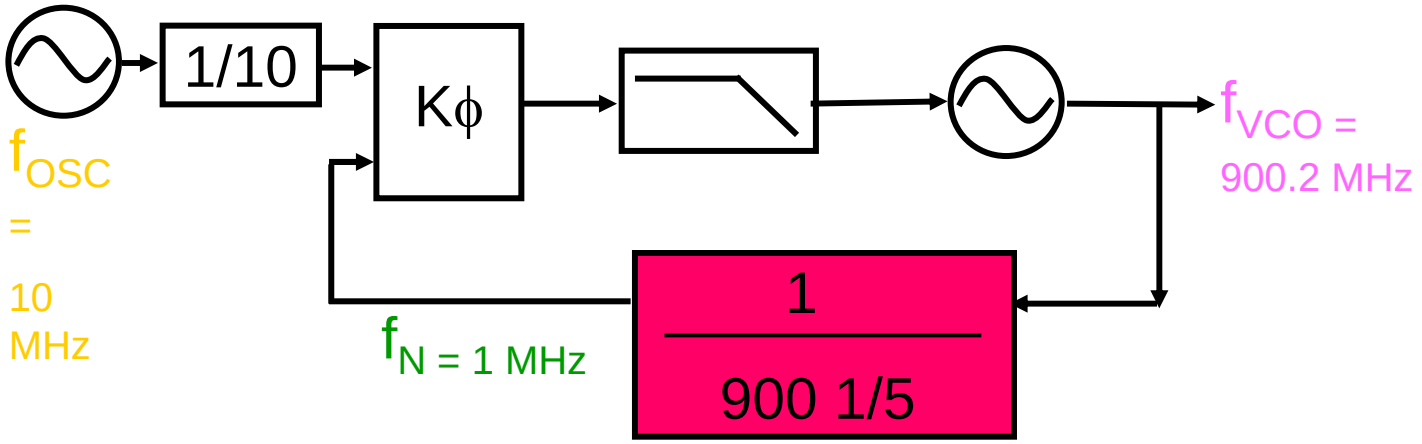
Fractional N Counter



- **Allowing N to be fractional allows it to be lower, which results in finer tuning resolution and better noise performance. For more narrow channel spacing, it also can result in lower spurs and faster switching speed.**
- **The denominator of the fractional part of the N counter is called the fractional modulus (5 in this case)**

Fractional N Implementation

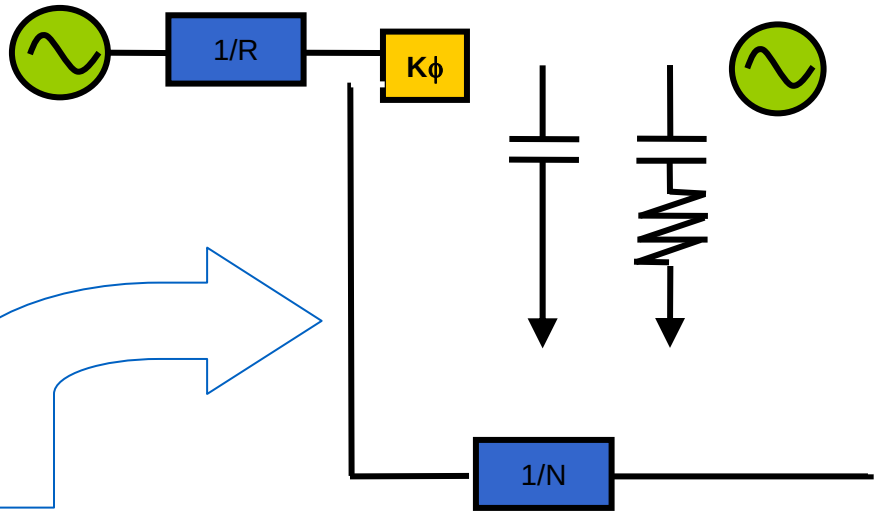
- **Uses Fractional N Averaging**

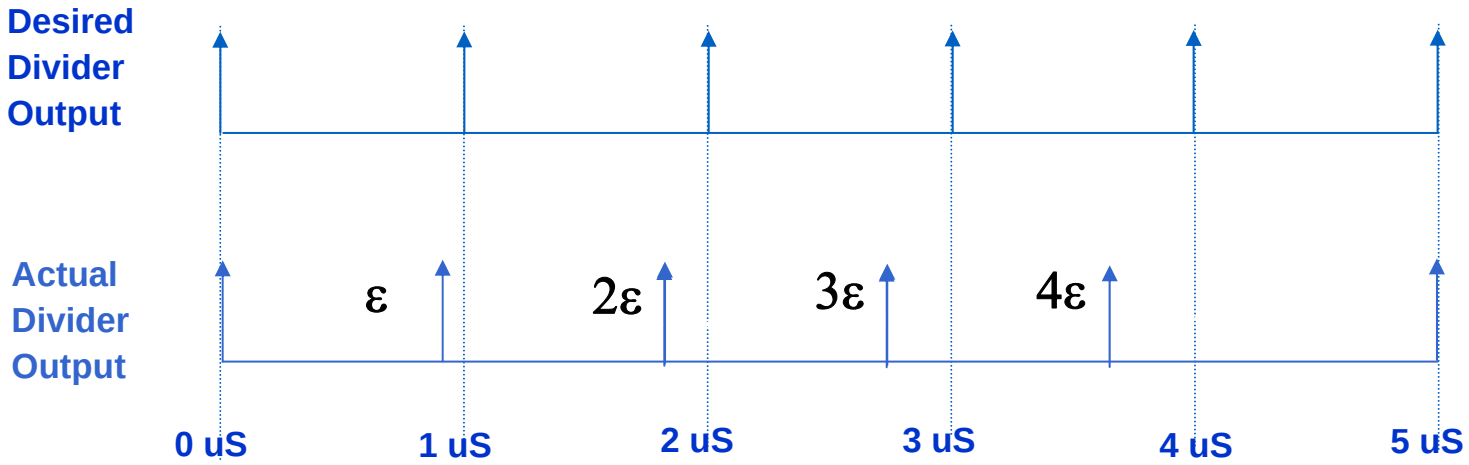
900	First Time
900	Second Time
900	Third Time
900	Fourth Time
901	Fifth time
900.2	Average Value

- **Although the Average Value is correct, compensation is necessary to correct for the instantaneous phase error. This phase error gives rise to fractional spurs. They would be at offsets that are increments of 200 kHz in this example.**

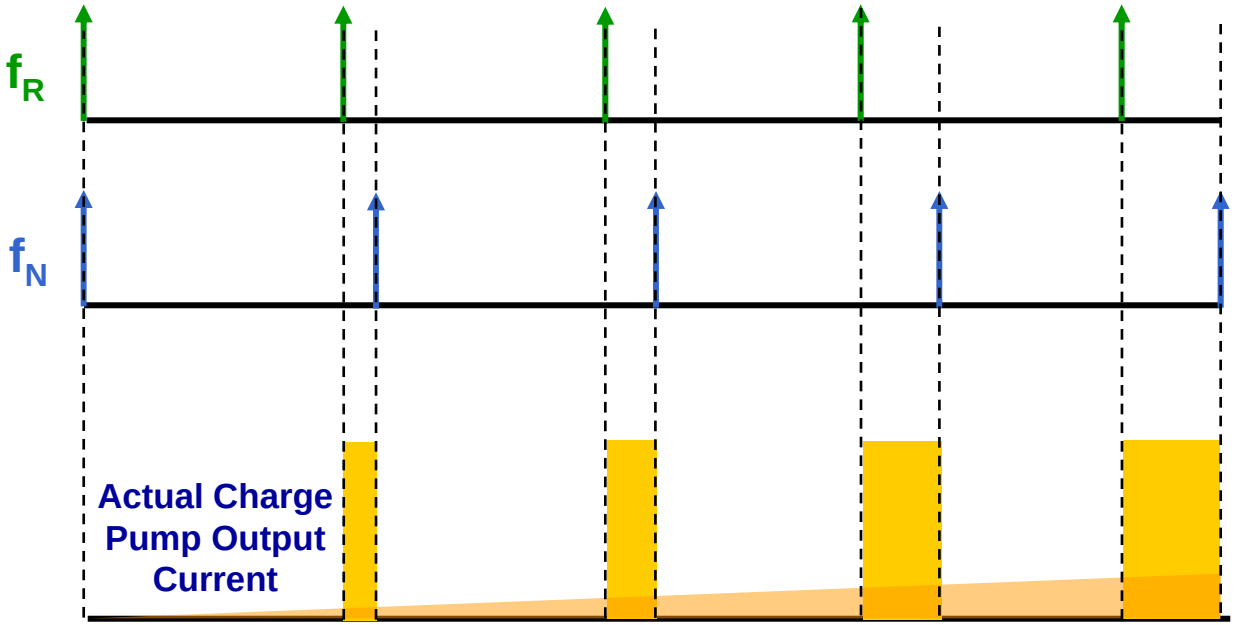
The Need for Compensation

$$\varepsilon = \frac{900.2 - 900}{900.2\ MHz}$$



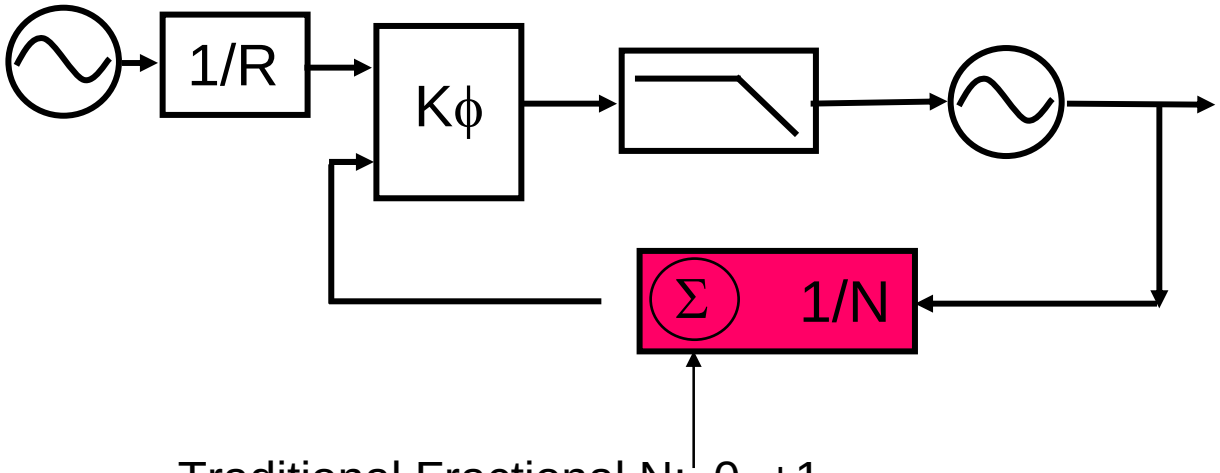


Fractional Compensation Techniques



- Current Correction Technique cancels current with another current, but this can be impredicatable, especially over temperature
- Phase Delay Technique corrects with a phase delay at the phase detector, but can add phase noise

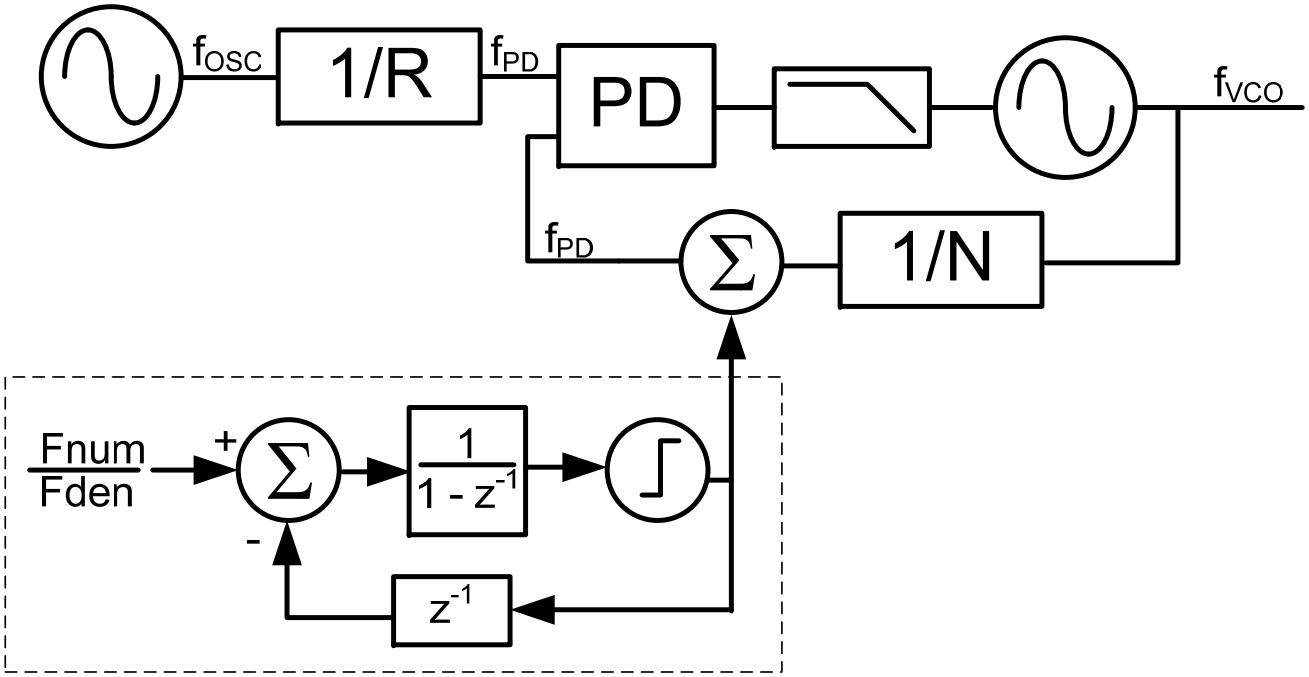
Delta Sigma N Counter



Traditional Fractional N: 0, +1
2nd Order Delta Sigma Fractional N: -1, 0, 1, 2
3rd Order Delta Sigma Fractional N: -7, -6, … + 8
4th Order Delta Sigma Fractional N: -15, -14, … + 16

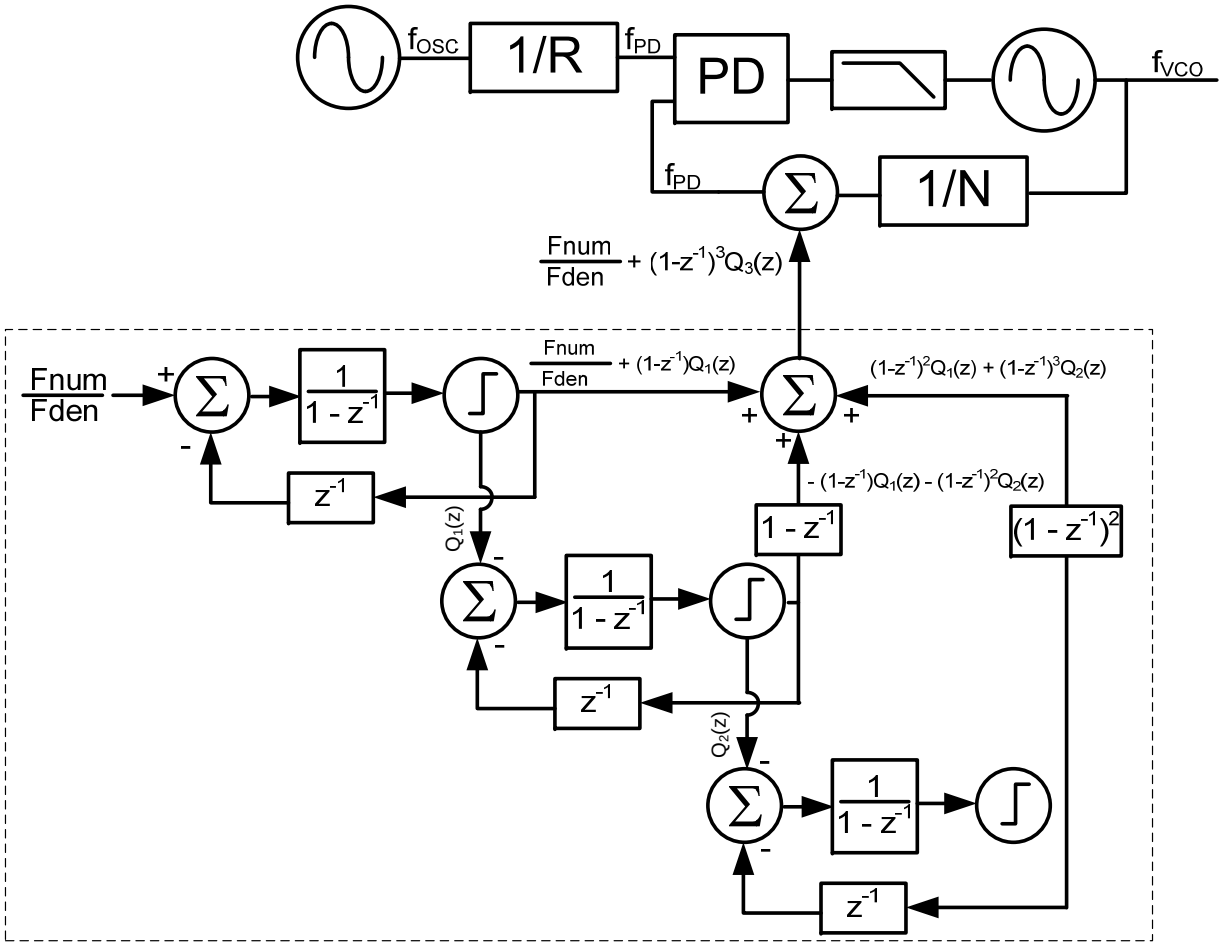
- **N counter value is modulated such that the average value is equal to the desired fraction**

First Order Modulator



- Z^{-1} is a one clock cycle delay
- $1 / (1-z^{-1})$ is a summation

3rd Order Modulator Example



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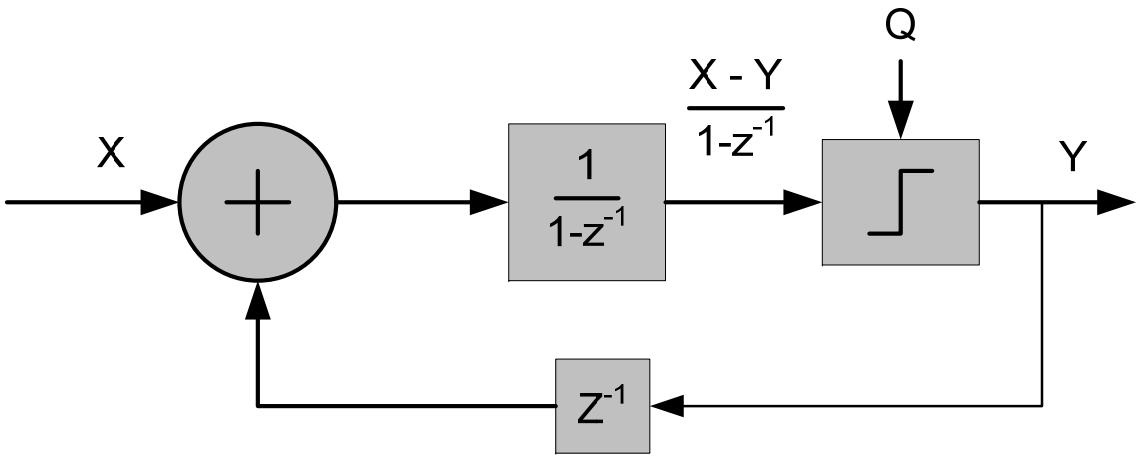
Delta Sigma Noise Shaping



$$Y = X + (1-z^{-1})*Q = Y = X + N(z)*Q$$

- **$N(z) = 1 - z^{-1} = 1 - e^{-j\omega} = 1 - \cos(\omega) + j\sin(\omega)$, $\omega = 2\pi f/f_{PD}$.**
- **$|N(z)|^2 = (1 - \cos(\omega))^2 + \sin^2(\omega) = 4*\sin^2(\pi f/f_{PD})$**
- **$|N(z)|^2 = |Q(z)|^2 = 4*\sin^2(\pi f/f_{PD})$**

Σ-Δ Phase Noise

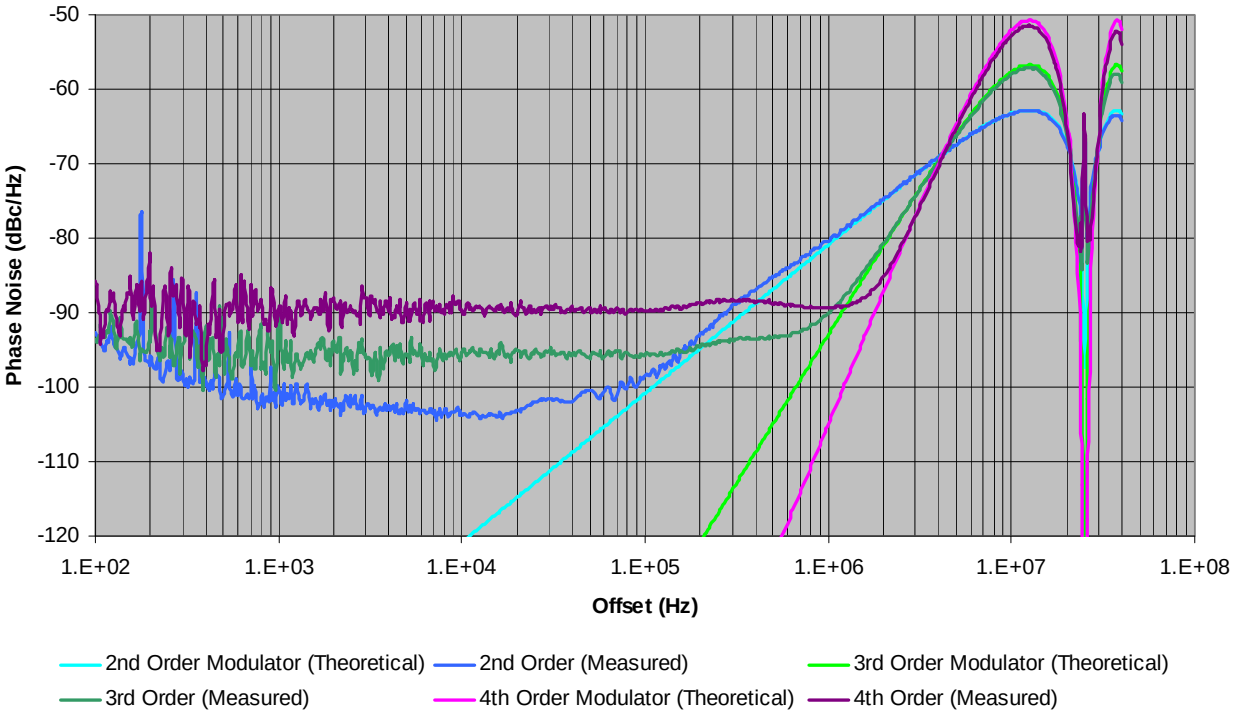
- **The full expression for quantization noise at the synthesizer output:**

$$S_\phi(f) = \frac{1}{12}\frac{1}{T_{PD}} \cdot \left|T_{PD} \cdot G(f)\right|^2 (2\pi)^2 \left(2 \cdot \sin\left(\frac{\pi f}{f_{PD}}\right)\right)^{2(n-1)}$$

- **G(f) is PLL lowpass response, so excluding this gives the shaped PSD of the quantization noise alone**

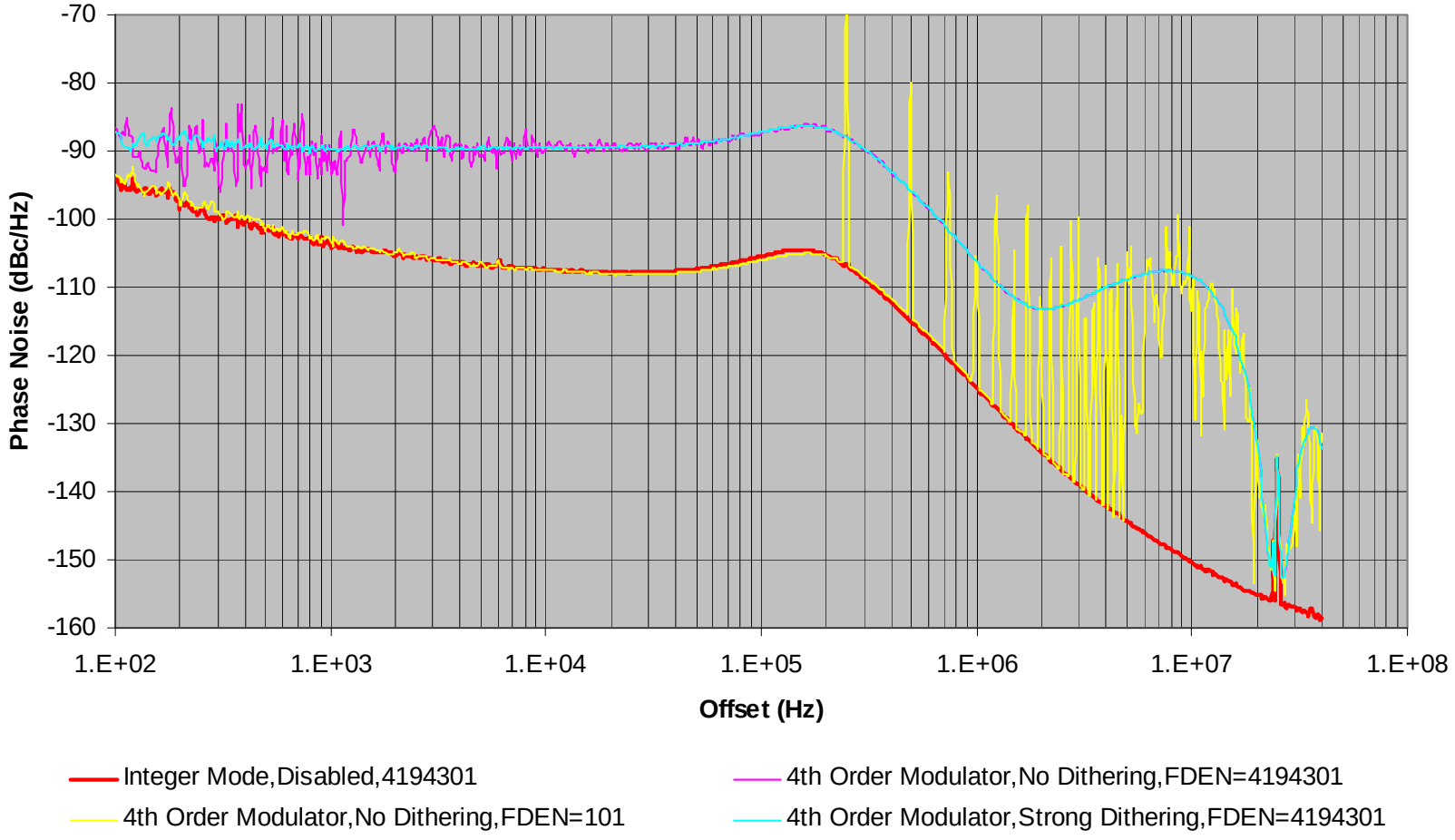
$$S_Q(f) = \frac{1}{12 \cdot f_{PD}} (2\pi)^2 \left(2 \cdot \sin\left(\frac{\pi f}{f_{PD}}\right)\right)^{2(n-1)}$$

Delta Sigma Noise



- **Excellent agreement with theory at far offsets**
- **Charge Pump causes higher frequency noise to mix down to lower offsets**
- **This close-in noise is relatively consistent for the LMX2485, LMX2531, and LMX2541 families**
  - **2nd Order Modulator -105 dBc**
  - **3rd Order Modulator -95 dBc**
  - **4th Order Modulator -90 dBc**

Notion of Well-Randomized



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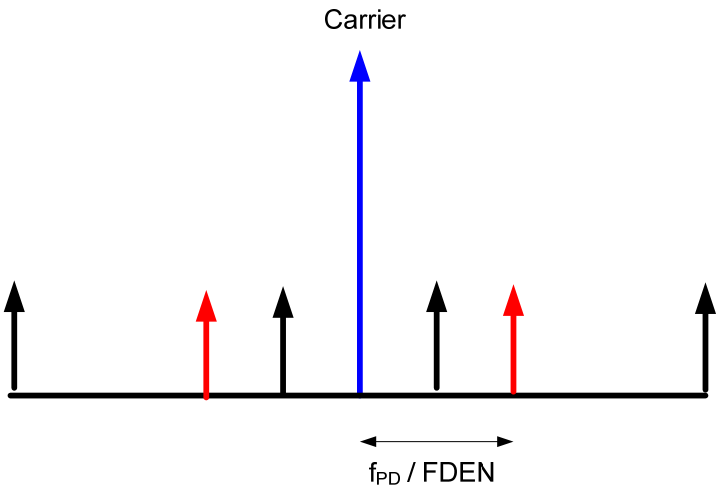
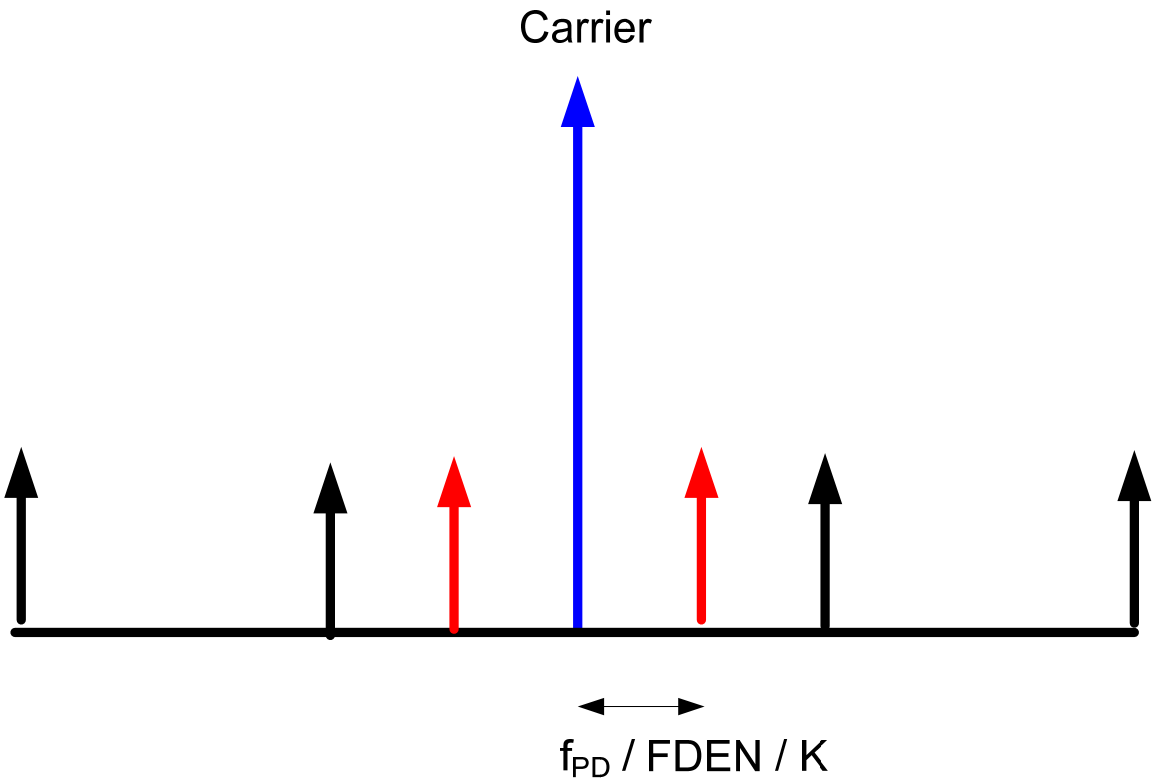
Primary Fractional Spurs



- **Highly Dependent on Fraction**
- **Theory and Measured Data Agree Well for Analog Compensation**
  - **Theory involves calculating Fourier series**
  - **Subtract out a Constant Factor**
  - **Tracks Roll-off**
  - **Sort of works the same for Delta-Sigma PLLs**

Sub-Fractional Spurs



- **Occur at a fraction of the channel spacing**

Sub-Fractional Spurs

- **Occur at a sub-multiple of where the fractional spur would be**
- **Typically less than primary fractional spur**
- **Impacted a lot by dithering and also the way the fraction is expressed (i.e. 1000/1000000 vs. 1/10)**
- **Occurrence based on chart below**

ORDER	Fractional Denominator Factors			
	No Factor of 2 or 3	Factor of 2 but not 3	Factor of 3 but not 2	Factor of 2 and 3
Integer Mode	None	None	None	None
1st Order Modulator	None	None	None	None
2nd Order Modulator	None	Fch/2	None	Fch/2
3rd Order Modulator	None	Fch/2	Fch/3	Fch/6
4th Order Modulator	None	Fch/4	Fch/3	Fch/12

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