EVM User's Guide: LMH1239EVM

LMH1239 Evaluation Module

Description

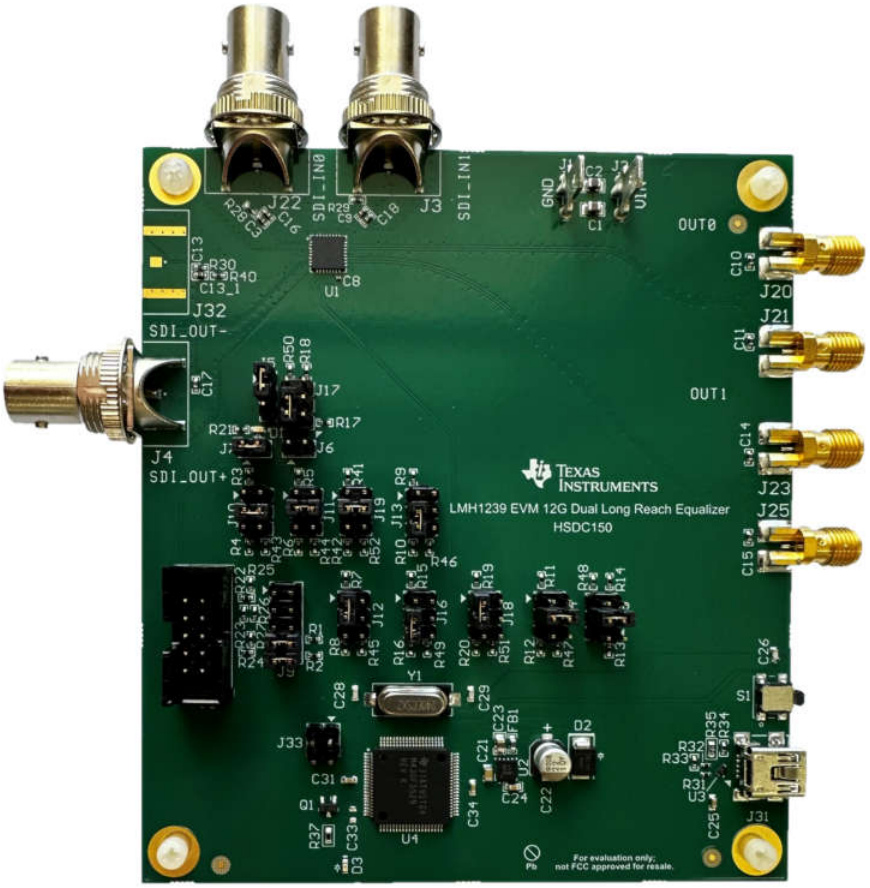
The LMH1239 is a long reach adaptive cable equalizer with integrated reclocker, dual outputs, and 75Ω loop-through output. The device is designed to equalize data transmitted over 75Ω coaxial cable and operates across SMPTE data rates ranging from 125Mbps to 11.88Gbps.

Features

- User configurable adaptive cable equalizer or cable driver with integrated reclocker
- Supports ST-2082-1(12G), ST-2081-1(6G), ST-424(3G), ST-292(HD), and ST-259(SD)
- Integrated reclocker locks to SMPTE video rates of 11.88 Gbps, 5.94 Gbps, 2.97 Gbps, 1.485 Gbps or divide-by-1.001 sub-rates and 270Mbps
- Dual adaptive cable equalizer at 75Ω single-ended input ports SDI_IN0± and SDI_IN1±
- Dual 100Ω output driver with de-emphasis output port OUT0± and OUT1±
- Line-side reclocked 75Ω loop-through output on port SDI_OUT±
- Programmable by pin, SPI, or SMBus interface
- Single supply operation: VDD = 2.5V ± 5%
- -40°C to +85°C operation
- High speed signal flow–thru pin-out package: 5mm x 5mm 32-pin WQFN package

Applications

- SMPTE compatible serial digital interface
- UHDTV, 4K, 8K, HDTV, SDTV video
- Broadcast video routers, switches, distribution amplifiers, and monitors
- Digital video processing and editing



1 Evaluation Module Overview

1.1 Introduction

The LMH1239EVM is an evaluation module designed for high speed performance and functional evaluation of the Texas Instruments LMH1239 12G UHD long reach cable equalizer with integrated reclocker and input mux.

With this kit, users can quickly evaluate the cable reach and output signal integrity supported by the LMH1239. High performance edge mount BNC connectors are used at the 75Ω port for the SDI_IN and SDI_OUT signals, while 100Ω differential output ports are routed to edge mount SMA connectors. These connectors facilitate connection to lab equipment or user systems for performance evaluation.

An onboard MSP430 MCU is included to support an optional SMBus or SPI serial control interface when configuring the LMH1239 operating modes.

- LMH1239 features:
  - Dual adaptive cable equalizer at 75Ω single-ended input ports SDI_IN0± and SDI_IN1±
  - Dual 100Ω output driver with de-emphasis output port OUT0± and OUT1±
  - Line-side reclocked 75Ω loop-through output on port SDI_OUT±

1.2 Kit Contents

- (1) LMH1239EVM

1.3 Device Information

Table 1-1. LMH1239 Ordering Information

EVM ID	DEVICE ID	DEVICE PACKAGE
LMH1239EVM	LMH1239RTV	WQFN (32)

2 Hardware

2.1 Setup

The LMH1239EVM can be used in one of three modes:

1. **Pin Mode (Default)** – Provides general access to the LMH1239 signal integrity and I/O control settings with IC pin-level logic.
2. **SPI Mode** – Provides full access to the LMH1239 signal integrity and control settings with POCI, PICO, SCK, and CS pins.
3. **SMBus Mode** – Provides full access to the LMH1239 signal integrity and control settings via SDA, SCL, and GND pins. ADDR0 and ADDR1 pins are used for SMBus address strap.

Using either SPI or SMBus mode, users have full access to all register controls in the LMH1239. For convenience, the LMH1239EVM features an on-chip MSP430 that is configured as a USB2ANY interface between LMH1239 and PC through the mini-USB port header on J31.

The default configuration for the LMH1239EVM has SDI_IN0 enabled while SDI_OUT and OUT1 are disabled. See Figure 2-1 for the labeled outputs and default pin shunt configuration.

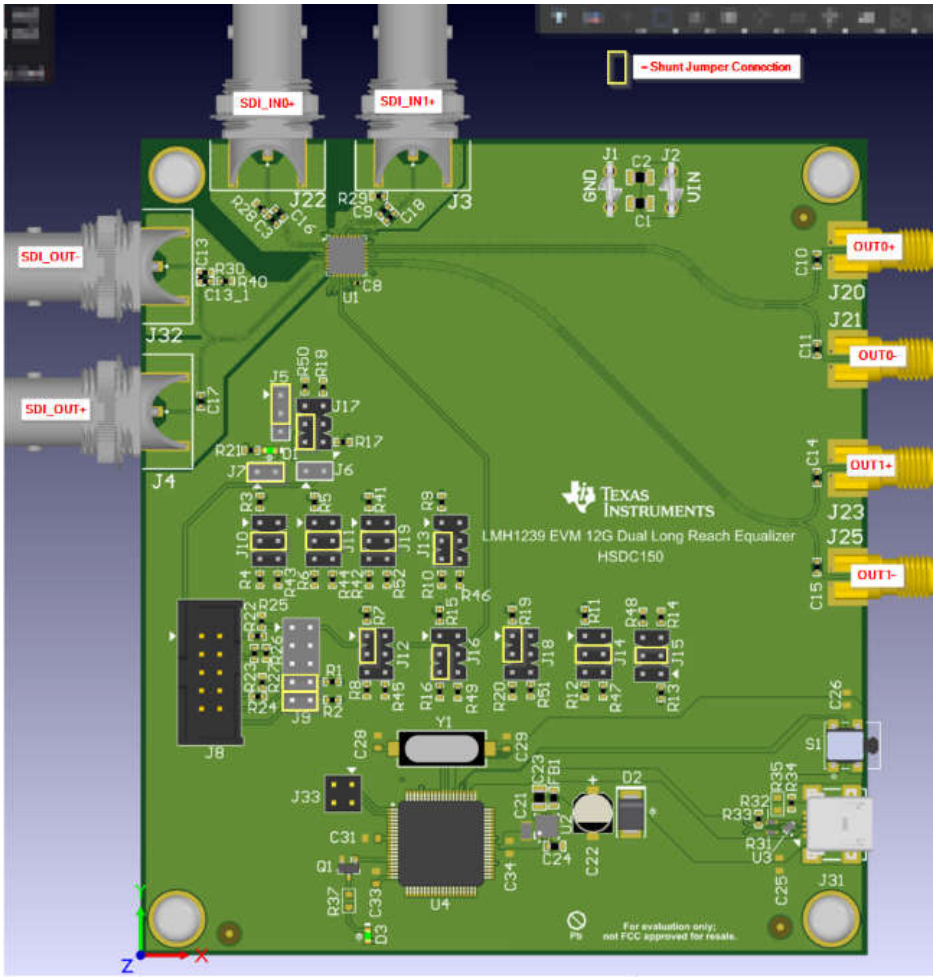


Figure 2-1. LMH1239 EVM inputs, Outputs and Pin Shunt Configurations

Note

Currently, the interface from PC to on-board MSP430 can only support SMBus communication.

The external control pins on the LMH1239EVM are used to configure the default device settings. A 4-level input scheme across the control pin interface increases the amount of control levels available to the device with fewer physical pins. The channel settings and controls are configurable in pin mode for the LMH1239 4-logic levels (L, R, F, H). The four logic levels correspond to the following voltages in Table 2-1.

Table 2-1. Description of 4-Level Voltage Inputs and Jumper Ties

LEVEL	SETTING	NOMINAL PIN VOLTAGE
H	Tie 1kΩ to VIN	VIN
F	Float (leave pin open)	2/3 × VIN
R	Tie 20kΩ to GND	1/3 × VIN
L	Tie 1kΩ to GND	0

Typical 4-level input thresholds:

- Internal threshold between L and R = 0.2 × VIN
- Internal threshold between R and F = 0.5 × VIN
- Internal threshold between F and H = 0.8 × VIN

To set these 4-level voltage inputs, each input is controlled by a group of 6 jumper pins set in Figure 2-2.

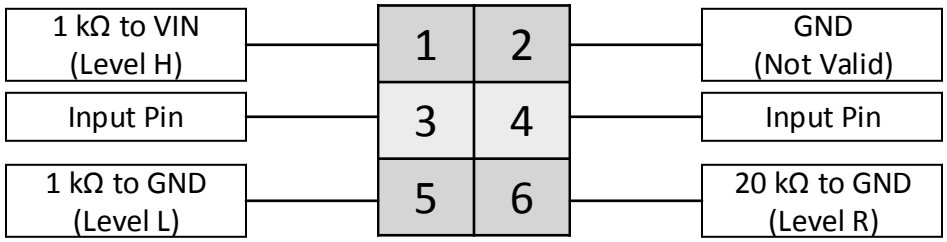


Figure 2-2. Jumper Orientation for User Configuration

Therefore, the following jumper positions allow access to each of the four logic levels:

LEVEL	JUMPER TIES
H	Pin 1-3
F	Pin 3-4 (or no connect)
R	Pin 4-6
L	Pin 3-5

The following jumpers have 4-level input control: J10, J11, J12, J13, J14, J15, J16, J17, J18, and J19.

In Pin Mode, OUT0_OUT1_SEL, LOOP_BW_SEL, VOD_DEM_SEL, MODE_SEL, OUT_CTRL, SDI_VOD, SDI_OUT_ENA and SDI_IN_SEL pins control different LMH1239 settings. Using SPI or SMBus, these initial pin control values can be overridden by setting the appropriate override bits through register control. Both SPI and SMBus interfaces allow full control over a wide range of device settings. See Table 2-2 and Table 2-3 for jumper descriptions and differences.

Table 2-2. Description of Connections in SPI Mode (MODE_SEL = Level F)

COMPONENT	NAME	COMMENTS
J1	GND	GND power supply
J2	VIN	2.5V VIN power supply
J5	ENABLE	Enable pin for the LMH1239. Shunt Pin 1 and 2 for proper operation. Refer to LMH1239 data sheet for detailed information.
J6	POCI	Shunt Pin 1 and 2 to connect POCI signal to J8 for proper SPI mode operation.
J7	LOCK_N	Reclocker lock indicator for the selected input. Shunt Pin 1 and 2 for proper operation. Refer to LMH1239 data sheet for detailed controls.
J8	SPI Access	SPI access pins. See data sheet and EVM schematic for detailed pin-out information.
J9	SPI Access	For SPI mode, install pin 1-2, 3-4, and 5-6 for SPI 3.3V to 2.5V level shift. Leave pin 7-10 open. See data sheet for additional information on SPI operation.
J10	OUT0_OUT1_SEL	OUT0_OUT1_SEL pin selects the SMA outputs. H: OUT0 and OUT1 muted. F and L: OUT0 enabled and OUT1 muted. R: OUT0 and OUT1 enabled.
J11	LOOP_BW_SEL	LOOP_BW_SEL- H: 13MHz/7MHz/5MHz/3MHz/1MHz. F: 13MHz/7MHz/5MHz/3MHz/1MHz. R: 800KHz/437KHz/312KHz/187KHz/62KHz. L: 400KHz/219KHz/156KHz/94KHz/31KHz. **Note** These are for 12G/6G/3G/HD/SD data rates. External caps are needed for H, R and L cases.
J12	VOD_DEM_SEL	VOD_DEM_SEL- H:410 mVpp, 0dB DEM F:560 mVpp, -0.9dB R: 635 mVpp, -2.4dB L: 810 mVpp, -4.0dB See data sheet and EVM schematic for additional operation information.
J13	MODE_SEL	Level F: SPI Mode
J14	OUT_CTRL	OUT_CTRL selects the signal flow from the selected IN port to the enabled outputs. OUT_CTRL selects reclocked data, reclocked data and clock, bypass reclocker (equalized data route to output driver), or both equalizer and reclocker bypassed.
J15	SDI_VOD	SDI VOD - H: About +5% (nominal) F:800mVpp (nominal) R: About 10% of nominal L:About -5% of nominal
J16	CS_N_ADDR0	Chip select. When CS_N is at logic low, CS_N enables SPI access to the LMH1239 peripheral device.
J17	POCI_ADDR1	POCI is the SPI serial control data output from the LMH1239 peripheral device. POCI is a 2.5V LVCMOS output.
J18	SDI_OUT_ENA	SDI_OUT_ENA pin enables or disables the SDI_OUT 75Ω output. H: SDI_OUT Disabled F and R: Do not use L: SDI_OUT Enabled See data sheet and EVM schematic for additional operation information.
J19	SDI_IN_SEL	SDI_IN_SEL pin determines the SDI-IN 75Ω input that is enabled. Level F: SDI-IN0. See data sheet and EVM schematic for additional operation information.

Table 2-3. Description of Connections in SMBus Mode (MODE_SEL = Level L)

COMPONENT	NAME	COMMENTS
J6	POCI	Leave Pin 1 and 2 open for proper SMBus operation.
J7	LOCK_N	Reclocker lock indicator for the selected input. Shunt Pin 1 and 2 for proper operation. Refer to LMH1239 data sheet for detailed controls.
J8	SMBus Access	SMBus access pins. See the data sheet and EVM schematic for detailed pinout information.
J9	SMBus Access	External 2kΩ pullup resistor to 3.3V supply. Install shunt jumpers on pin 7-8 and 9-10 for proper operation. Leave pins 1-6 open. See the data sheet for additional information on SMBus operation.
J13	MODE_SEL	Level L: SMBus mode.
J16	ADDR0	4-Level strap pins to determine up to 16 unique SMBus address with J17 to create AD[1:0]. See the data sheet for different SMBus address combinations.
J17	ADDR1	4-Level strap pins to determine up to 16 unique SMBus address with J16 to create AD[1:0]. See the data sheet for different SMBus address combinations.

Table 2-4. Input and Output Channel Connections

SIGNAL INPUTS AND OUTPUTS	
JUNCTION NUMBERS	FUNCTION
J4, J32	SDI_OUT+, SDI_OUT- (BNC single-ended)
J22, J3	SDI_IN0+, SDI_IN1+ (BNC single-ended)
J22, J23	OUT0+, OUT0– (SMA)
J24, J25	OUT1+, OUT1– (SMA)

Note

Jumpers not listed in Table 2-3 are identical to the functions mentioned in Table 2-2.

2.1.1 Hardware and Software: Description and Setup

By factory default, the LMH1239EVM is configured to accept a valid SDI signal on SDI_IN0 and output the retimed data on OUT0.

The general procedure for setting up and testing with the LMH1239EVM is as follows. For pin configurations, reference the illustrations in Figure 2-3 and Figure 2-4.

1. Connect 2.5V power (0.5A max) to the EVM and install the appropriate shunt jumpers to operate in SMBus Mode:
   a. Connect J2: VIN = 2.5V and J1: GND.
      i. Install shunt jumper on J7 Pins 1-2(H).
   b. Set the following control switches for appropriate operation:
      i. Install shunt jumper on J5 pins 1-2(H).
      ii. Install shunt jumper on J17 pins 3-5(L).
      iii. Install shunt jumper on J7 pins 1-2(H).
      iv. Install shunt jumpers on J9 pins 7-8 and Pins 9-10.
      v. Install shunt jumper on J10 pins 3-4(F).
      vi. Install shunt jumper on J11 pins 3-4(F).
      vii. Install shunt jumper on J19 pins 3-5(L).
      viii. Install shunt jumper on J13 pins 3-5(L).
      ix. Install shunt jumper on J12 pins 1-3(H).
      x. Install shunt jumper on J16 pins 3-5(L).
      xi. Install shunt jumper on J18 pins 1-3(H).
      xii. Install shunt jumpers on J14 and J15 pins 3-4(F).
2. Connect PC to LMH1239EVM with a USB-to-mini-USB cable through the mini-USB port located on J31. The LMH1239's control and signal integrity settings are programmable with SigCon Architect, a GUI which supports full register access through SMBus communication. For more information about SigCon Architect, reference the *SigCon Architect: Installation and Starter's Guide*.

3. If SigCon Architect is used, then connect PC to LMH1239EVM with a USB-to-mini-USB cable via mini-USB port located on J31. If operating without software, then leave the mini-USB port on J31 unconnected, and refer to LMH1239 data sheet and LMH1239EVM schematic for detailed information on how to properly set up J11, J12, J14, J15, and J18 to the test needs.

Note

When using Sigcon Architect with address headers J16 and J17 set to L, the peripheral address assigned to the LMH1239 is 7A.

1. SDI_OUT enabled: Connect the LMH1239EVM to the system under test.
   a. The input signal on J22 can be connected to a video signal generator over a 75Ω coax cable. Alternatively, the LMH1218EVM can be used as a 100Ω differential-to-75Ω single-ended converter. Then, the 75Ω OUT0+ of the LMH1218 can be used as an input to the SDI_IN0+ of the LMH1239.
   b. The output signal on J20, J21, J23 and J25 can be connected with matched 100Ω differential cables to a high-speed scope to view the output eye diagram.
   c. The output signal on J32 can be connected with a 75Ω coax cable to a video pattern analyzer as a loop-through output becausem the signal is enabled in the shunt jumper settings shown in Figure 2-3.

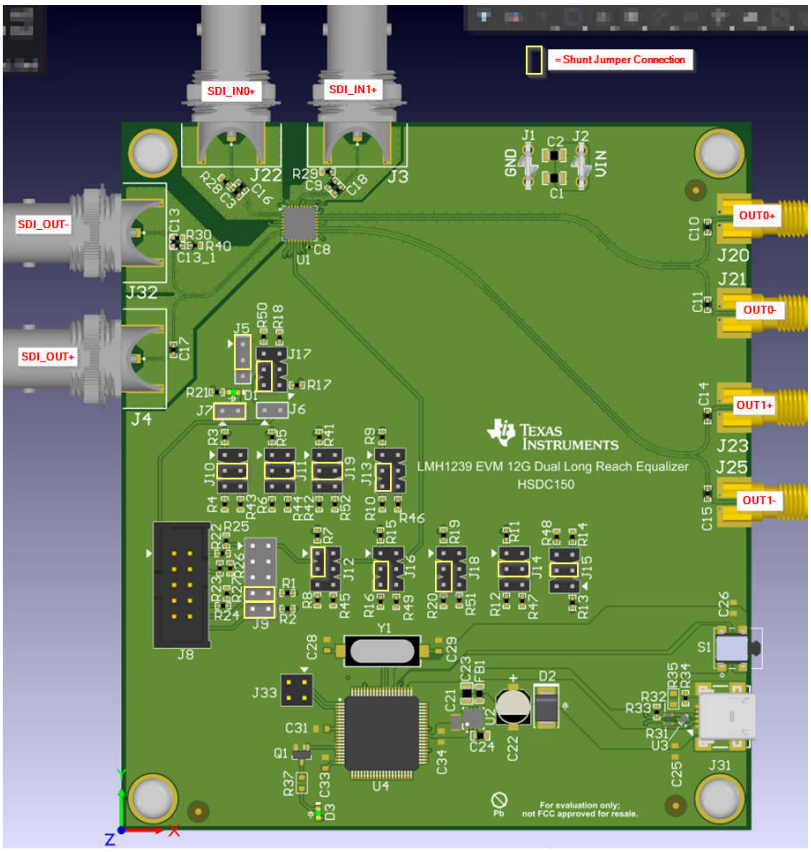


Figure 2-3. LMH1239EVM SDI_OUT Enabled for SMBus Operation

2.1.1.1 SDI_IN1 Selected

1. Connect the LMH1239EVM to the system under test.
   a. The input signal on J3 can be connected to a video signal generator over a 75Ω coax cable.
   b. The output signals on J20, J21, J23 and J25 can be connected with matched 100Ω differential cables to a high-speed scope to view the output eye diagram. Alternatively, this 100Ω output can be used as the source for another SDI cable driver.
   c. The output signal on J32 can be connected with 75Ω coax cable to a video pattern analyzer.

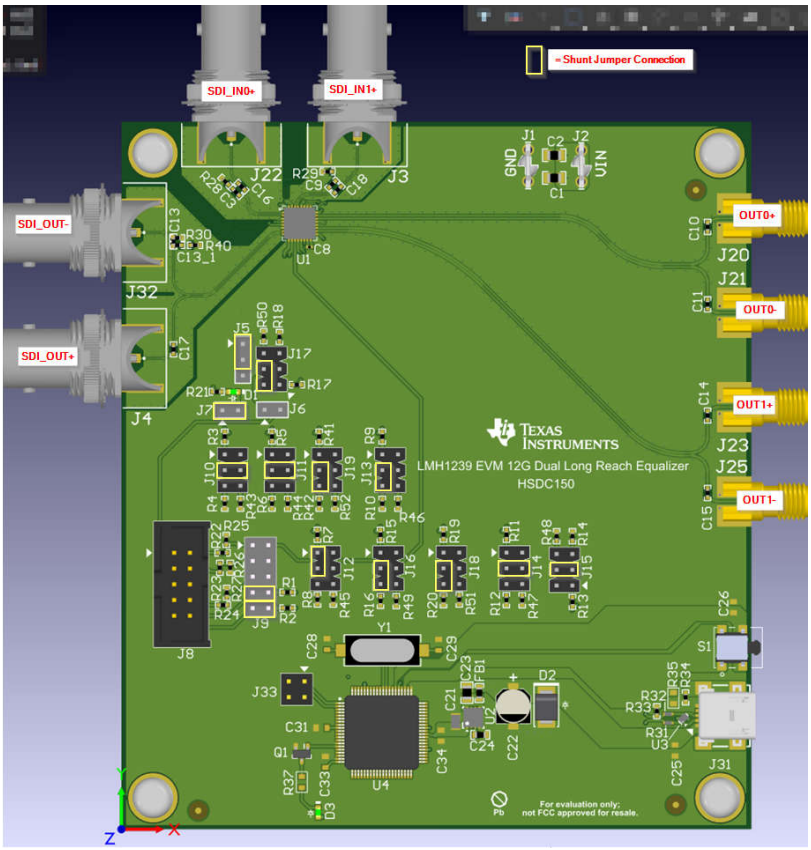


Figure 2-4. LMH1239EVM SDI_OUT and SDI_IN1 Enabled for SMBus Operation

3 Hardware Design Files

3.1 Schematics

Figure 3-1 shows the schematic for LMH1239EVM.

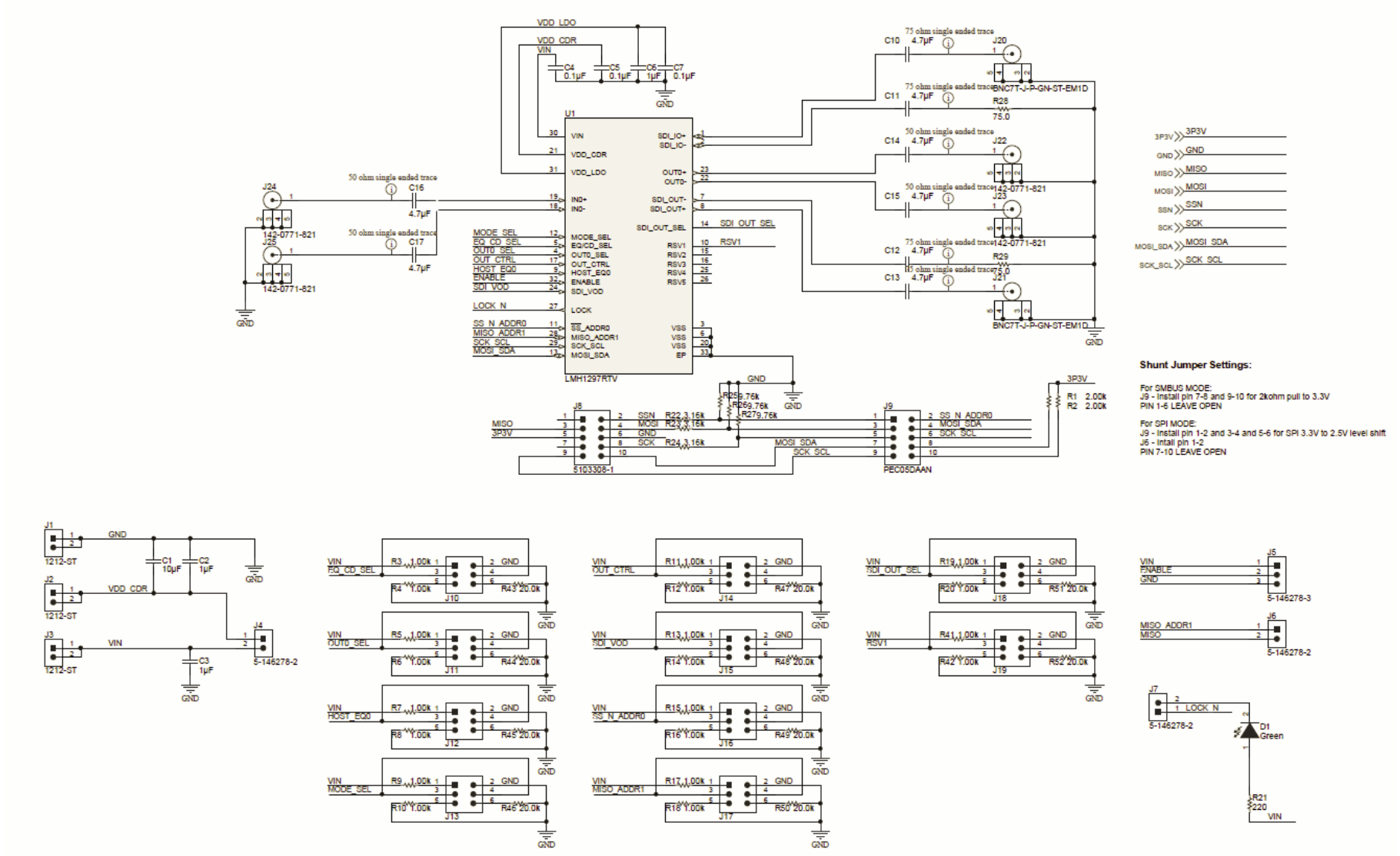


Figure 3-1. LMH1239EVM Schematic Page

3.2 PCB Layout

The following figures show the LMH1239EVM layout. The evaluation board controls signal integrity control settings via jumper pins.

The LMH1239EVM allows access to all input channels (SDI_IN0 and SDI_IN1) and output channels (OUT0, OUT1, and SDI_OUT). The EVM is very compact and low power. The WQFN package offers an exposed thermal pad to enhance electrical and thermal performance. This must be soldered to the copper landing on the PCB.

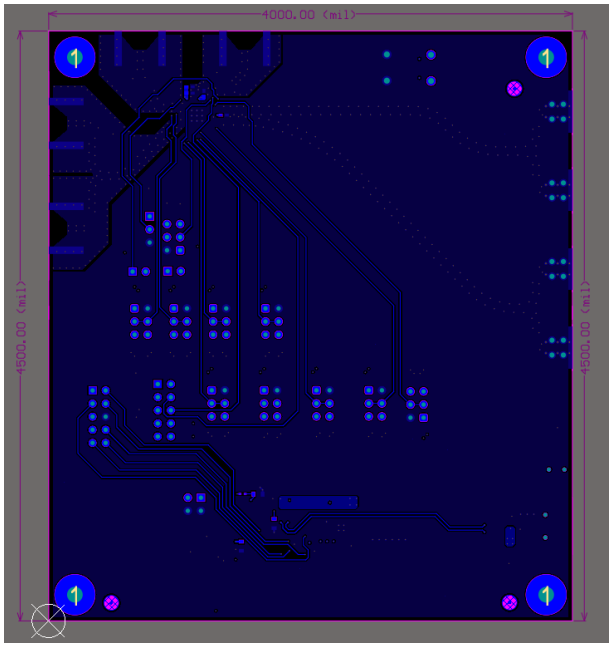


Figure 3-2. LMH1239EVM Bottom Layer

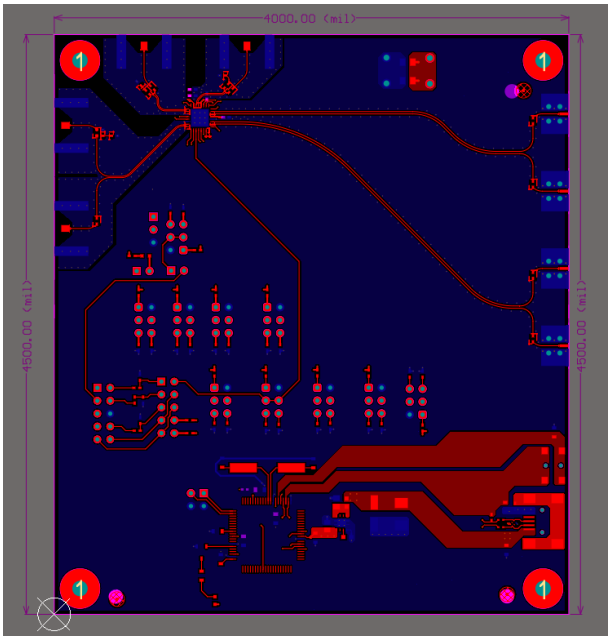


Figure 3-3. LMH1239EVM Top Layer

4 Additional Information

4.1 Trademarks

All trademarks are the property of their respective owners.

5 Related Documentation

- LMH12x9 data sheet, SNOSDC1

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265