DP83815,DP83816

AN-1323 Updating DP83815 MacPHYTER Hardware Designs to DP83816 MacPHYTER-II

Literature Number: SNLA063

Updating DP83815 Mac-PHYTER™ Hardware Designs to DP83816 MacPHYTER-II

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1.0 Scope

This application note is provided to allow a DP83815 based design to be updated to DP83816 efficiently. It details the differences in pin connections and functionality between DP83816 MacPHYTER-II and DP83815 MacPHYTER.

2.0 General Information

1. The **DP83816** is only available in 144-LQFP package as used on the **DP83815**.
2. The **DP83816** uses 0.18μm CMOS technology compared to the **DP83815** which uses 0.35μm CMOS technology.
3. NSC provided drivers are compatible on both the **DP83816** and the **DP83815**.
4. To allow differentiation between the **DP83816** and the **DP83815**, the Silicon Revision Register (SRR - offset 58h) has been updated to 0505h for the **DP83816**.

3.0 Pin Change Information

Pin changes on the **DP83816** are divided into three categories. Required connection changes, must be observed for proper operation (see Table 1). Optional connection changes, pin can be left connected as it was on the **DP83815** with no adverse effects, although it has a different function on the **DP83816** (see Table 2). Informational changes, pins that have kept the same connections but changed names (see Table 3).

Table 4 shows all pins of both devices for easy comparison.

3.1 REQUIRED PIN CONNECTION CHANGES

Required pin connection changes must be done for proper operation of the device. Note that although pin 48 has nothing connected to it on both devices, its functionality on the **DP83816** has changed. The reason for not connecting it has changed and is explained below.

- For **DP83816,** pin 19 should be connected to GND through 10μF and 0.1μF parallel caps, as shown in Figure 1.
  For **DP83815**, pin 19 is connected to the 3.3V AUX supply and to a 0.01μF cap, as shown in Figure 2.
- For **DP83816**, pin 40 is connected to GND via a 10KΩ resistor, as shown in Figure 1.
  For **DP83815**, pin 40 is connected to GND via a 9.31KΩ resistor, as shown in Figure 2.
- For **DP83816**, pin 48 is Reserved and cannot be connected to any external logic or net, as shown in Figure 1.
  For **DP83815**, pin 48 is a No Connect, as shown in Figure 2.

Table 1 compares these pins on both devices.

Figure 1. DP83816 pin connections Block Diagram

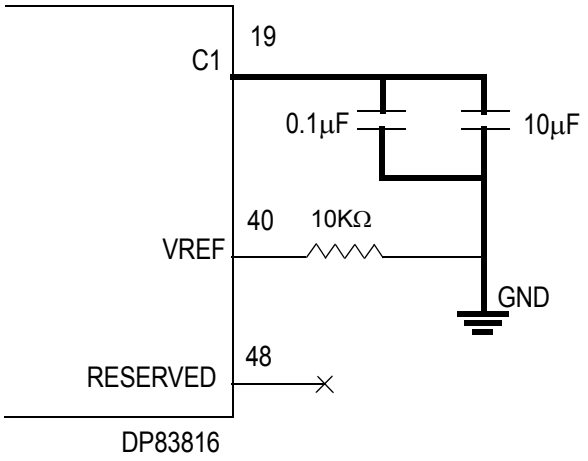
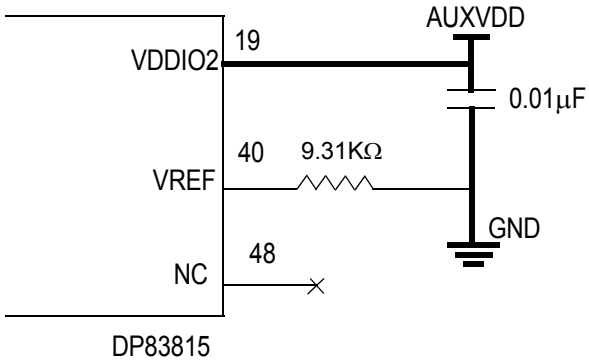


Figure 2. DP83815 pin connections Block Diagram



3.2 OPTIONAL PIN CONNECTION CHANGES

These pins have functionally changed, however previous connections would have no adverse effects.

Table 2 compares these pins on both devices.

3.3 INFORMATIONAL PIN CHANGES

These are pin name changes only, functionality remains the same.

Table 3 compares these pins on both devices.

Table 1. DP83816 required pin connection changes

DP83815	DP83816	LQFP Pin No(s)	Description
VDDIO2	C1	19	**On DP83815:** Connect to Aux 3.3V supply VDD **On DP83816:** Connect to GND through 10uF and 0.1uF external parallel capacitors
VREF	VREF	40	**Bandgap Reference:** External current reference resistor for internal Phy bandgap circuitry. **For the DP83815:** The value of this resistor is 9.31 KΩ 1% metal film (100 ppm/^{o}C) which must be connected from the VREF pin to ground. **For the DP83816:** The value of this resistor is 10 KΩ 1% metal film (100 ppm/^{o}C) which must be connected from the VREF pin to ground
NC	RESERVED	48	**On DP83815:** No Connect **On DP83816:** Reserved and cannot be connected to any external logic or net.

Table 2. DP83816 optional pin connection changes

DP83815	DP83816	LQFP Pin No(s)	Description
FXVDD, SUBGND1, VSSIO4, VDDIO4, MACVSS2, MACVDD2, SUBGND3	NC	36, 37, 84, 85, 124, 125, 126	**On DP83815:** Connect pins 36, 37, 84, 85, 124, 125 and 126 to isolated Aux 3.3V supply VDD, GND, GND, Aux 3.3V supply VDD, GND, Aux 3.3V supply VDD, and GND respectively. **On DP83816:** These pins, that were previously supply pins on the DP83815, are now No Connects, and thus having them connected as they were previously on the DP83815 has no adverse effects.

Table 3. DP83816 pin name changes

DP83815	DP83816	LQFP Pin No(s)	Description
VDDIO1, PHYVDD1, VDDIO3, PHYVDD2, TXDVDD, MACVDD1, VDDIO5	AUXVDD	9, 21, 27, 33, 56, 58, 137	Connect to Aux 3.3V supply VDD
PCIVDD1, PCIVDD2, PCIVDD3, PCIVDD4, PCIVDD5	PCIVDD	69, 80, 94, 107, 117	PCI VDD - connect to PCI bus 3.3V VDD
VSSIO1, VSSIO2, VSSIO3, PHYVSS1, PHYVSS2, FXVSS, RXAVSS1, RXAVSS2, SUBGND2, TXDVSS, TXIOVSS1, TXIOVSS2, MACVSS1, PCIVSS1, PCIVSS2, PCIVSS3, PCIVSS4, PCIVSS5, VSSIO5	VSS	8, 16, 20, 26, 32, 35, 38, 44, 49, 51, 52, 55, 57, 65, 77, 90, 103, 114, 136	VSS

Table 4. DP83815 pins vs. DP83816 pins

DP83815	DP83816	LQFP Pin No(s)	Description
PCI Bus Interface			
AD[31-0]	AD[31-0]	66, 67, 68, 70, 71, 72, 73, 74, 78, 79, 81, 82, 83, 86, 87, 88, 101, 102, 104, 105, 106, 108, 109, 110, 112, 113, 115, 116, 118, 119, 120, 121	**Address and Data:** Multiplexed address and data bus. As a bus master, the DP83815/16 will drive address during the first bus phase. During subsequent phases, the DP83815/16 will either read or write data expecting the target to increment its address pointer. As a bus target, the DP83815/16 will decode each address on the bus and respond if it is the target being addressed.
CBEN[3-0]	CBEN[3-0]	75, 89, 100, 111	**Bus Command/Byte Enable:** During the address phase these signals define the “bus command” or the type of bus transaction that will take place. During the data phase these pins indicate which byte lanes contain valid data. CBEN[0] applies to byte 0 (bits 7-0) and CBEN[3] applies to byte 3 (bits 31-24) in the Little Endian Mode. In Big Endian Mode, CBEN[3] applies to byte 0 (bits 31-24) and CBEN[0] applies to byte 3 (bits 7-0). Big Endian mode only applies to PCI master operations; the byte ordering does not change for target register accesses.
PCICLK	PCICLK	60	**Clock:** This PCI Bus clock provides timing for all bus phases. The rising edge defines the start of each phase. The clock frequency ranges from 0 to 33 MHz.
DEVSELN	DEVSELN	95	**Device Select:** As a bus master, the DP83815/16 samples this signal to insure that the destination address for the data transfer is recognized by a PCI target. As a target, the DP83815/16 asserts this signal low when it recognizes its address after FRAMEN is asserted.
FRAMEN	FRAMEN	91	**Frame:** As a bus master, this signal is asserted low to indicate the beginning and duration of a bus transaction. Data transfer takes place when this signal is asserted. It is de-asserted before the transaction is in its final phase. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.
GNTN	GNTN	63	**Grant:** This signal is asserted low to indicate to the DP83815/16 that it has been granted ownership of the bus by the central arbiter. This input is used when the DP83815/16 is acting as a bus master.
IDSEL	IDSEL	76	**Initialization Device Select:** This pin is sampled by the DP83815/16 to identify when configuration read and write accesses are intended for it.
INTAN	INTAN	61	**Interrupt A:** This signal is asserted low when an interrupt condition occurs as defined in the Interrupt Status Register, Interrupt Mask, and Interrupt Enable registers.
IRDYN	IRDYN	92	**Initiator Ready:** As a bus master, this signal will be asserted low when the DP83815/16 is ready to complete the current data phase transaction. This signal is used in conjunction with the TRYDN signal. Data transaction takes place at the rising edge of PCICLK when both IRDYN and TRDYN are asserted low. As a target, this signal indicates that the master has put the data on the bus.
PAR	PAR	99	**Parity:** This signal indicates even parity across AD[31-0] and CBEN[3-0] including the PAR pin. As a master, PAR is asserted during address and write data phases. As a target, PAR is asserted during read data phases.

DP83815	DP83816	LQFP Pin No(s)	Description
PERRN	PERRN	97	**Parity Error:** The DP83815/16 as a master or target will assert this signal low to indicate a parity error on any incoming data (except for special cycles). As a bus master, it will monitor this signal on all write operations (except for special cycles).
REQN	REQN	64	**Request:** The DP83815/16 will assert this signal low to request ownership of the bus from the central arbiter.
RSTN	RSTN	62	**Reset:** When this signal is asserted all outputs of DP83815/16 will be tri-stated and the device will be put into a known state.
SERRN	SERRN	98	**System Error:** This signal is asserted low by DP83815/16 during address parity errors and system errors if enabled.
STOPN	STOPN	96	**Stop:** This signal is asserted low by the target device to request the master device to stop the current transaction.
TRDYN	TRDYN	93	**Target Ready:** As a master, this signal indicates that the target is ready for the data during write operation and with the data during read operation. As a target, this signal will be asserted low when the (target) device is ready to complete the current data phase transaction. This signal is used in conjunction with the IRDYN signal. Data transaction takes place at the rising edge of PCICLK when both IRDYN and TRDYN are asserted low.
PMEN/ CLKRUNN	PMEN/ CLKRUNN	59	**Power Management Event/Clock Run Function:** This pin is a dual function pin. The function of this pin is determined by the CLKRUN_EN bit 0 of the CLKRUN Control and Status register (CCSR). Default operation of this pin is PMEN. **Power Management Event:** This signal is asserted low by DP83815/16 to indicate that a power management event has occurred. For pin connection please refer to Section 6.7. **Clock Run Function:** In this mode, this pin is used to indicate when the PCICLK will be stopped.
3VAUX	3VAUX	122	**PCI Auxiliary Voltage Sense:** This pin is used to sense the presence of a 3.3V auxiliary supply in order to define the PME Support available. For pin connection please refer to Section 6.7. This pin has an internal weak pull down.
PWRGOOD	PWRGOOD	123	**PCI bus power good:** Connected to PCI bus 3.3V power, this pin is used to sense the presence of PCI bus power during the D3 power management state. This pin has an internal weak pull down.
Media Independent Interface (MII)			
COL	COL	28	**Collision Detect:** The COL signal is asserted high asynchronously by the external PMD upon detection of a collision on the medium. It will remain asserted as long as the collision condition persists.
CRS	CRS	29	**Carrier Sense:** This signal is asserted high asynchronously by the external PMD upon detection of a non-idle medium.
MDC	MDC	5	**Management Data Clock:** Clock signal with a maximum rate of 2.5 MHz used to transfer management data for the external PMD on the MDIO pin.
MDIO	MDIO	4	**Management Data I/O:** Bidirectional signal used to transfer management information for the external PMD. (See Section 3.12.4 for details on connections when MII is used.)
RXCLK	RXCLK	6	**Receive Clock:** A continuous clock, sourced by an external PMD device, that is recovered from the incoming data. During 100 Mb/s operation RXCLK is 25 MHz and during 10 Mb/s this is 2.5 MHz.

DP83815	DP83816	LQFP Pin No(s)	Description
RXD3/MA9, RXD2/MA8, RXD1/MA7, RXD0/MA6	RXD3/MA9, RXD2/MA8, RXD1/MA7, RXD0/MA6	12, 11, 10, 7	**Receive Data**: Sourced from an external PMD, that contains data aligned on nibble boundaries and are driven synchronous to RXCLK. RXD[3] is the most significant bit and RXD[0] is the least significant bit. **BIOS ROM Address:** During external BIOS ROM access, these signals become part of the ROM address.
RXDV/MA11	RXDV/MA11	15	**Receive Data Valid:** Indicates that the external PMD is presenting recovered and decoded nibbles on the RXD signals, and that RXCLK is synchronous to the recovered data in 100 Mb/s operation. This signal will encompass the frame, starting with the Start-of-Frame delimiter (JK) and excluding any End-of-Frame delimiter (TR). **BIOS ROM Address:** During external BIOS ROM access, this signal becomes part of the ROM address.
RXER/MA10	RXER/MA10	14	**Receive Error:** Asserted high synchronously by the external PMD whenever it detects a media error and RXDV is asserted in 100 Mb/s operation. **BIOS ROM Address:** During external BIOS ROM access, this signal becomes part of the ROM address.
RXOE	RXOE	13	**Receive Output Enable:** Used to disable an external PMD while the BIOS ROM is being accessed.
TXCLK	TXCLK	31	**Transmit Clock:** A continuous clock that is sourced by the external PMD. During 100 Mb/s operation this is 25 MHz +/- 100 ppm. During 10 Mb/s operation this clock is 2.5 MHz +/- 100 ppm.
TXD3/MA15, TXD2/MA14, TXD1/MA13, TXD0/MA12	TXD3/MA15, TXD2/MA14, TXD1/MA13, TXD0/MA12	25, 24, 23, 22	**Transmit Data:** Signals which are driven synchronous to the TXCLK for transmission to the external PMD. TXD[3] is the most significant bit and TXD[0] is the least significant bit. **BIOS ROM Address:** During external BIOS ROM access, these signals become part of the ROM address.
TXEN	TXEN	30	**Transmit Enable:** This signal is synchronous to TXCLK and provides precise framing for data carried on TXD[3-0] for the external PMD. It is asserted when TXD[3-0] contains valid data to be transmitted.
100BASE-TX/10BASE-T Interface			
TPTDP, TPTDM	TPTDP, TPTDM	54, 53	**Transmit Data:** Differential common output driver. This differential common output is configurable to either 10BASE-T or 100BASE-TX signaling: 10BASE-T: Transmission of Manchester encoded 10BASE-T packet data as well as Link Pulses (including Fast Link Pulses for Auto-Negotiation purposes). 100BASE-TX: Transmission of ANSI X3T12 compliant MLT-3 data. The DP83815/16 will automatically configure this common output driver for the proper signal type as a result of either forced configuration or Auto-Negotiation.
TPRDP, TPRDM	TPRDP, TPRDM	46, 45	**Receive Data:** Differential common input buffer. This differential common input can be configured to accept either 100BASE-TX or 10BASE-T signaling: 10BASE-T: Reception of Manchester encoded 10BASE-T packet data as well as normal Link Pulses and Fast Link Pulses for Auto-Negotiation purposes. 100BASE-TX: Reception of ANSI X3T12 compliant scrambled MLT-3 data. The DP83815/16 will automatically configure this common input buffer to accept the proper signal type as a result of either forced configuration or Auto-Negotiation.

DP83815	DP83816	LQFP Pin No(s)	Description
BIOS ROM/Flash Interface			
MCSN	MCSN	129	**BIOS ROM/Flash Chip Select:** During a BIOS ROM/Flash access, this signal is used to select the ROM device.
MD7, MD6, MD5, MD4/EEDO, MD3, MD2, MD1/CFGDISN, MD0	MD7, MD6, MD5, MD4/EEDO, MD3, MD2, MD1/CFGDISN, MD0	141, 140, 139, 138, 135, 134, 133, 132	**BIOS ROM/Flash Data Bus:** During a BIOS ROM/Flash access these signals are used to transfer data to or from the ROM/Flash device. MD[5:0] pins have internal weak pull ups. MD6 and MD7 pins have internal weak pull downs.
MA5, MA4/ EECLK, MA3/ EEDI, MA2/ LED100K, MA1/ LED10N, MA0/ LEDACTN	MA5, MA4/ EECLK, MA3/ EEDI, MA2/ LED100K, MA1/ LED10N, MA0/ LEDACTN	3, 2, 1, 144, 143, 142	**BIOS ROM/Flash Address:** During a BIOS ROM/Flash access, these signals are used to drive the ROM/Flash address.
MWRN	MWRN	131	**BIOS ROM/Flash Write:** During a BIOS ROM/Flash access, this signal is used to enable data to be written to the Flash device.
MRDN	MRDN	130	**BIOS ROM/Flash Read:** During a BIOS ROM/Flash access, this signal is used to enable data to be read from the Flash device.
Clock Interface			
X1	X1	17	**Crystal/Oscillator Input:** This pin is the primary clock reference input for the DP83815/16 and must be connected to a 25 MHz 0.005% (50ppm) clock source. The DP83815/16 device supports either an external crystal resonator connected across pins X1 and X2, or an external CMOS-level oscillator source connected to pin X1 only.
X2	X2	18	**Crystal Output:** This pin is used in conjunction with the X1 pin to connect to an external 25 MHz crystal resonator device. This pin must be left unconnected if an external CMOS oscillator clock source is utilized. For more information see the definition for pin X1.
LED Interface			
LEDACTN/MA0	LEDACTN/MA0	142	**TX/RX Activity:** This pin is an output indicating transmit/receive activity. This pin is driven low to indicate active transmission or reception, and can be used to drive a low current LED (<6 mA). The activity event is stretched to a min duration of approximately 50 ms.
LED100N/MA2	LED100N/MA2	144	**100 Mb/s Link:** This pin is an output indicating the 100 Mb/s Link status. This pin is driven low to indicate Good Link status for 100 Mb/s operation, and can be used to drive a low current LED (<6 mA).
LED10N/MA1	LED10N/MA1	143	**10 Mb/s Link:** This pin is an output indicating the 10 Mb/s Link status. This pin is driven low to indicate Good Link status for 10 Mb/s operation, and can be used to drive a low current LED (<6 mA).
Serial EEPROM Interface			
EESEL	EESEL	128	**EEPROM Chip Select:** This signal is used to enable an external EEPROM device.
EECLK/MA4	EECLK/MA4	2	**EEPROM Clock:** During an EEPROM access (EESEL asserted), this pin is an output used to drive the serial clock to an external EEPROM device.
EEDI/MA3	EEDI/MA3	1	**EEPROM Data In:** During an EEPROM access (EESEL asserted), this pin is an output used to drive opcode, address, and data to an external serial EEPROM device.

DP83815	DP83816	LQFP Pin No(s)	Description
EEDO/MD4	EEDO/MD4	138	**EEPROM Data Out:** During an EEPROM access (EESEL asserted), this pin is an input used to retrieve EEPROM serial read data. This pin has an internal weak pull up.
MD1/CFGDISN	MD1/CFGDISN	133	**Configuration Disable:** When pulled low at power-on time, disables load of configuration data from the EEPROM. Use 1 KΩ to ground to disable configuration load.
External Reference Interface			
VREF	VREF	40	**Bandgap Reference:** External current reference resistor for internal Phy bandgap circuitry. **For the DP83815:** The value of this resistor is 9.31 KΩ 1% metal film (100 ppm/^{o}C) which must be connected from the VREF pin to ground. **For the DP83816:** The value of this resistor is 10 KΩ 1% metal film (100 ppm/^{o}C) which must be connected from the VREF pin to ground
No Connects and Reserved			
NC	NC	34, 42, 43	No Connect
FXVDD, SUBGND1, VSSIO4, VDDIO4, MACVSS2, MACVDD2, SUBGND3	NC	36, 37, 84, 85, 124, 125, 126	**On DP83815:** Connect pins 36, 37, 84, 85, 124, 125 and 126 to isolated Aux 3.3V supply VDD, GND, GND, Aux 3.3V supply VDD, GND, Aux 3.3V supply VDD, and GND respectively. **On DP83816:** These pins, that were previously supply pins on the DP83815, are now No Connects, and thus having them connected as they were previously on the DP83815 has no adverse effects.
NC	RESERVED	48	**On DP83815:** No Connect **On DP83816:** Reserved and cannot be connected to any external logic or net.
RESERVED	RESERVED	41, 50, 127	Reserved and cannot be connected to any external logic or net.
Supply Pins			
VDDIO2	C1	19	**On DP83815:** Connect to Aux 3.3V supply VDD **On DP83816:** Connect to GND through 10uF and 0.1uF external parallel capacitors
RXAVDD1, RXAVDD2	IAUXVDD	39, 47	Connect to isolated Aux 3.3V supply VDD
VDDIO1, PHYVDD1, VDDIO3, PHYVDD2, TXDVDD, MACVDD1, VDDIO5	AUXVDD	9, 21, 27, 33, 56, 58, 137	Connect to Aux 3.3V supply VDD
PCIVDD1, PCIVDD2, PCIVDD3, PCIVDD4, PCIVDD5	PCIVDD	69, 80, 94, 107, 117	PCI VDD - connect to PCI bus 3.3V VDD

DP83815	DP83816	LQFP Pin No(s)	Description
VSSIO1, VSSIO2, VSSIO3, PHYVSS1, PHYVSS2, FXVSS, RXAVSS1, RXAVSS2, SUBGND2, TXDVSS, TXIOVSS1, TXIOVSS2, MACVSS1, PCIVSS1, PCIVSS2, PCIVSS3, PCIVSS4, PCIVSS5, VSSIO5	VSS	8, 16, 20, 26, 32, 35, 38, 44, 49, 51, 52, 55, 57, 65, 77, 90, 103, 114, 136	VSS

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