Application Report
SNLA126A–February 2010–Revised April 2013

AN-2007 Improving the Robustness of Channel Link Designs with Channel Link II Ser/Des

ABSTRACT

This application note discusses how system designers are able to use Channel Link II ser/Des to improve old and new channel link designs.

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1 Introduction

The first generation Channel Link Ser/Des devices allowed system designers to transmit a wide data bus while reducing their interconnect density. These devices used a parallel clock architecture which eliminated the need for local reference oscillators and training/synchronization patterns to obtain lock in the receive system. These unique features allowed devices such as the DS90CR217/218A, DS90CR285/286A and the DS90CR287/288A to become very popular in the industrial imaging, printing and digital video transport markets.

As technology advanced in display and sensor resolution, interconnect distance requirements also increased. Since, the first generation Channel Link devices used a parallel clock architecture to transmit serial data, system designers had to closely monitor the inter-pair (channel-to-channel) skew specifications of their interconnects and in turn, the overall receiver skew margin (RSKM).

The new Channel Link II Ser/Des family of products tackles these limiting older system specifications with new and innovative architectural changes. All Channel Link II Ser/Des use an embedded clock architecture with encoded data. This allows Channel Link II receivers to lock on to random data transmitted through an AC-coupled interfaces with minimal interconnect density and no reference clocks or oscillators. In addition, the thermal tolerance of all Channel Link II Ser/Des was improved to operate within the industrial temperature range of -40°C to +85°C.

2 Channel Link II Ser/Des

DS92LV3241/DS92LV3242 20 MHz – 85 MHz, 32 Bit LVCMOS Ser/Des with Automatic Deskew and Transmit Pre-Emphasis

The DS92LV3241/DS92LV3242 Ser/Des chipset can transport up to 32 bits of parallel data at rates of 20 MHz to 85 MHz across 2 (dual mode) or 4 (quad mode) serial data lanes. An integrated deskew circuit, compensates for the inter-pair skew up to 0.4 x transmit clock period (t_{CIP}). The deskew process is transparent to the system and is performed automatically during the locking sequence of the deserializer. The serializer has a selectable output differential voltage swing (V_{OD}) and configurable transmit pre-emphasis block to help compensate for high frequency attenuation across the serial interconnects. These three key specifications allow the DS92LV3241/DS92LV3242 to transmit more data, through less expensive interconnects and across longer distances that the first generation of Channel Link Ser/Des.

For systems that do not require the full 20 MHz – 85 MHz bandwidth, there is also a pin compatible chipset, the DS92LV3221/DS92LV3222. This chipset operates only in the 2 lane (dual mode) configuration with an operating frequency range of 20 MHz – 50 MHz. The DS92LV3221 and DS92LV3222 contain all of the key specifications of their quad lane capable counterparts such as: automatic deskew, selectable V_{OD}, configurable transmit pre-emphasis and integrated AT-SPEED BIST. The block diagram is shown in Figure 1 and a side-by-side comparison of several Channel Link devices and Channel Link II devices is shown in Table 1.

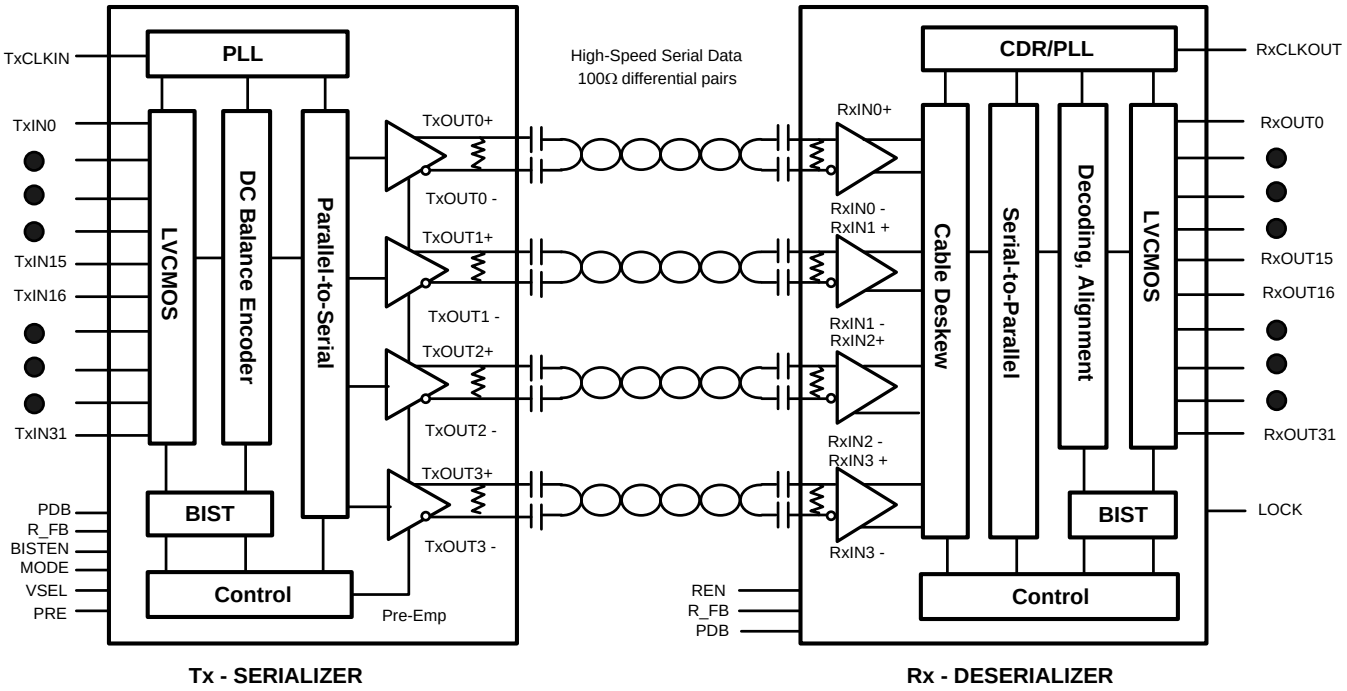

Figure 1. DS92LV3241/DS92LV3242 Block Diagram

Table 1. Channel Link vs. Channel Link II Feature Set Comparison

	Channel Link			Channel Link II	
Chipset (Ser/Des)	DS90CR217/218A	DS90CR285/286A	DS90CR287/288A	DS92LV3221/3222	DS92LV3241/3242
Serialization Ratio	21 : 4 (3 Data + 1 Parallel Clock)	28 : 5 (4 Data + 1 Parallel Clock)	28 : 5 (4 Data + 1 Parallel Clock)	32 : 2 (2 Lanes with Embedded Clock)	32 : 2/4 (2 or 4 Lanes with Embedded Clock)
Frequency Range (MHz)	20 – 85	20 – 66	20 – 85	20 – 50	20 – 85
Parallel Data Bus Width	21 Bit	28 Bit	28 Bit	32 Bit	32 Bit
Max Total Throughput (Gbps)	1.785	1.848	2.38	1.6	2.72
Operating Temperature Range	-10°C to +70°C	-40°C to +85°C	-10°C to +70°C	-40°C to +85°C	-40°C to +85°C
Maximum Skew Tolerance (min RSKM) at f_{MAX}	490 ps (f = 85 MHz)	400 ps (f = 66 MHz)	290 ps (f = 85 MHz)	8.0 ns (f = 50 MHz)	4.7 ns (f = 85 MHz)
Automatic Deskew	No	No	No	Yes	Yes
DC Balanced and Encoded Data	No	No	No	Yes	Yes
AT-SPEED BIST	No	No	No	Yes	Yes
Configurable Transmit Pre-Emphasis	No	No	No	Yes	Yes
Selectable V_{OD}	No	No	No	Yes	Yes

3 New Features in Channel Link II Ser/Des

3.1 Selectable v_{OD}

The output differential voltage swing of the DS92LV3241 and DS92LV3221 can be altered by setting the VSEL pin to LOW for ±220 mV (440 mV_{P-P}), or HIGH for ±425 mV (850 mV_{P-P}). The low swing option consumes less power. However, the large swing option allows for further cable reach. Pre-Emphasis can be used with both V_{OD} settings to help achieve better cable performance, while consuming little additional power.

3.2 Pre-emphasis

Pre-Emphasis can help to compensate for long or lossy transmission lines by proving added current to the higher frequency portions of the transmitted data. The amount of current added is related to the resistor which is attached to the PRE pin to ground (V_{SS}) by the following equations 1 below. Equation 2, shows how the added current corresponds to a boost in the V_{OD}

$$I_{PRE} = 48 / R_{PRE} \quad (1)$$

$$V_{ODPRE} = I_{PRE} \times 50\ \Omega \quad (2)$$

The minimum recommended value for RPRE is 12 kΩ. If no pre-emphasis is required the PRE pin should be left floating.

If pre-emphasis is not expected to be used for a design, it is still recommended to place the pads for a resistor to connect the PRE pin to V_{SS} on the PCB. A simple note to designate “Do Not Populate” the resistor at board assembly allows the serializer to meet existing system requirements, while also allowing the same PCB to be used in future systems which require longer cable lengths.

3.3 AT-SPEED BIST

The AT-SPEED BIST allows users to observe the quality of their link in terms of measured bit errors. In order to use the AT-SPEED BIST the transmitter, DS92LV3241/DS92LV3221, must have both a valid TxCLKIN and the BISTEN pin must be pulled HIGH. The receiving device must obtain lock before it can report out the status of the BIST.

During BIST mode, the serializer will ignore data on the TxIN pins and instead transmit out a balanced and encoded pseudo random bit sequence. The deserializer will automatically detect the incoming BIST pattern and enter BIST mode. While the deserializer is in BIST mode, the RXOUT pins will be reassigned to report out BIST status , pass or fail, and an error count for each high speed serial channel.

The AT-SPEED BIST can be used to speed up the design and validation process, by allowing designers to validate the signal integrity of the serial links. For detailed information on how to use the AT-SPEED BIST, please consult Functional Description section of the applicable datasheets.

3.4 Deskew

Deskew is performed automatically on the serial links during the deserializer lock process. The deserializer does not require a special deskew procedure, nor any special deskew patterns. During lock acquisition, a clock is recovered from each serial channel. These clocks are then used to align the decoded and deserialized data relative to clock recovered on channel 0. As shown in Table 1, the deskew circuit allows the maximum tolerable skew length to increase from the hundreds of picoseconds for Channel Link devices to nanoseconds for Channel Link II devices.

3.5 DC-Balanced and Encoded Data

The parallel data is processed is 3 ways before being serialized and transmitted out onto the serial channel. First the data is scrambled and then DC Balanced. The DC-Balanced data then goes through a bit shuffle circuit which manages the emissions of the serial stream by controlling the number of transitions per serial word. By the time the parallel data is ready to be transmitted out on the serial channel, 4 additional bits have been appended on. The first and last bits of each word are commonly referred to as clock bits. These bits are set at a static value, one HIGH and one LOW. This guarantees that there will always be at a minimum one transition for every serial word.

4 Using Channel Link II Devices to Improve Old and New Designs

First Generation Channel Link devices allowed users to transmit 24-bit color with H-sync(HS), V-sync(VS) and Data Enable (DE), while leaving only one spare bit for other control signals. The 32 bit wide parallel bus of the DS92LV3241/DS92LV3242 allows for a total of 5 additional control signals to be transmitted along with the 24 color and 2-sync and enable bits. These 5 added bits can be used to transmit triggers or other control data on the same wire pairs as the video data, unlike previous generation system which required additional components and wires to transmit this information. Also, the wide data bus now allows for 10-bit color application with 2 bits left for sync signals or data enable.

The integrated transmit signal conditioning allows designers to transmit data over longer distances or use less expensive lossy cables. The automatic deskew circuit also allows the use of more commercially available cables with less stringent skew requirements, such as CAT-5/6.

The automatic deskew circuit allows for a simple start sequence, while enabling cable lengths that were not possible in earlier generation systems. For example, many industrial imaging or machine vision applications use of mini-delta-ribbon (MDR) cable to transport the serial imaging data, because of their relatively tight inter-pair skew specifications which varied from 50 – 100+ ps/m depending on the cable vendor. In first generation Channel Link systems, one of the most critical parameters, RSKM, was dominated by interconnect skew. The minimum RSKM at 85 MHz, was specified to be 290 ps [(1)]. If it is assumed that cable skew dominates RSKM, then at 85 MHz with a high quality MDR cable, the expected cable length performance would max out at 290 ps / (50 ps/m) = 5.8m, neglecting any degradation in performance due to the insertion loss of the cable. With the DS92LV3241/DS92LV3242 chipset, the system would be capable of 0.4 x (1 / 85 MHz) = 4.71 ns of cable skew. If a similar quality MDR cable is used, then the system could handle cables of 4.71 ns / (50 ps/m) = 94.2m, again neglecting any degradation in performance due to the insertion loss of the cable.

5 Using Channel Link II devices to Simplify New Designs

The DS92LV3241/DS92LV3242 were designed to ease the learning curve burden of system designers and to maintain “ease of use.”

The DS92LV3241 can be configured to accept either 1.8V or 3.3V LVCMOS logic levels. This allows the serializer to easily interface to a variety of host devices without the need for input buffers or logic level shifters. The LVCMOS drivers found on the DS92LV3242 are capable of driving 8pF load, allowing them to interface with heavy input capacitance loads found on many ASIC and FPGA devices. In addition, the LVCMOS data busses of the serializer and deserializer can be independently controlled to latch data out on either the rising or falling clock edge to accommodate the interface of the host devices.

New systems can maintain a simple start up sequence, because the deskew process is integrated into the locking sequence and requires no external device manipulation. Unlike other devices with deskew circuits, a DS92LV3241 and DS92LV3242 system need only apply parallel clock and data to the serializer to begin data transmission while properly deskewing the interconnect.

The improved architecture of the DS92LV3241 and DS92LV3242 from first generation Channel Link devices, means that designers no longer have to worry about calculating RSKM down to the tens of picoseconds. Jitter transfer characteristics are provided for the serializer’s phase locked loop (PLL), while input jitter tolerance characteristics are provided for the deserializer’s clock and data recovery modules (CDR). In addition, the method of deskew was improved from the 48-bit versions of Channel Link devices to deskew input serial streams relative to the parallel clock frequency. This allows interconnects to now have greater amounts of inter-pair skew without compromising the integrity of the serial link.

6 Summary

Features such as automatic deskew, transmit pre-emphasis, selectable V_{OD}, data encoding and dc balancing make the DS92LV3241/DS92LV3242 Channel Link II Ser/Des devices well suited for Imaging, Machine Vision, and Display applications. These features allow for more robust serial connections and greatly simplify the design in process over the previous generation of Channel Link products.

(1) RSKM Min Value = 290ps, DS90CR287/DS90CR288A Datasheet July 2004. Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window-RSPOS). This margin allows LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and source clock (less than 150 ps).

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