DS90CR215,DS90CR216A,DS90CR217, DS90CR218A,DS90CR285,DS90CR286A, DS90CR287,DS90CR288A,DS90CR481, DS90CR482,DS90CR483A,DS90CR484A, DS90CR485,DS90CR486

Multi-Drop Channel-Link Operation

Literature Number: SNLA157

Multi-Drop Channel-Link Operation

National Semiconductor
Application Note 1109
John Goldie
Michael Hinh
May 1998

CHANNEL-LINK OPERATION

The Channel-Link chipset is configured to provide high speed data transmission over a reduced size interconnect. With the 7 to 1 mux/demux architecture cable and connector reductions of up to 80% are possible. LVDS also provides a low noise system due to the use of current mode LVDS line drivers, a small signal swing of ~300 mV typical, and differential signaling. LVDS is also very noise tolerant, as the receivers support a tight 100 mV threshold and a wide ±1V common mode operating range. Standard LVDS devices are intended for single termination (100Ω) applications. The transmitter may be connected to a single receiver load (point-to-point) or may be connected to multiple receivers (multi-drop) when certain system design guidelines are adhered to. This is possible since the chipset provides transparent synchronous data transmission and requires no control (other than a power down pin). The transmitter only requires clock and data, and each receiver operates independent of the others. The scope of this application note is to discuss the specific recommendations for multi-drop applications.

CONFIGURATION

The transmission line connecting the transmitter outputs to the receiver inputs and the termination resistor is critical. It must be designed to minimize any transmission line effects (reflections) from mid-stream receivers to the down stream receivers. This can be done by employing a daisy chain bus structure. A daisy chain is formed by running from the transmitter to the first receiver, then the next, and so on. Branches off the main line are minimized, and termination is *only* at the extreme end of the line. A daisy chain is shown in *Figure 1*. Receiver input impedance is in the order of 100's of kΩ, therefore DC loading is not a problem even with a dozen or more receivers connected along the line. The AC loading and any imbalance introduced will be more of the limiting factor in determining how many receivers may be added to the bus. Testing done at National Semiconductor's Interface lab has successfully driven 5 receiver loads across 18 inches of flat ribbon cable in a daisy chain. Greater distances are possible by using higher quality cable such as twisted pair. Other configurations such as "Y" or "T"s as shown in *Figure 2* should be avoided.

The Y and T configurations present two transmission line problems. At point A, a reflection will occur due to the impedance change. The two legs each have an impedance of Z_O, but they are seen in parallel at the point, therefore at point A, there is a change of impedance from Z_O to $Z_O/2$, which will create a −33% reflection. A second problem also exists in regards to termination. Each leg should be terminated, ideally in Z_O Ω. Thus the transmitter will see a 50Ω DC load instead of the intended 100Ω load and this will cut in half the signal swing due to the current mode drivers (fixed amount of current). For these AC (reflection) and DC (50Ω) reasons the Y and T configurations should be avoided.

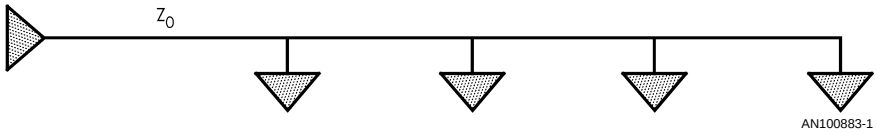

FIGURE 1. Daisy Chain Bus Configuration Supports Multi-drop Applications

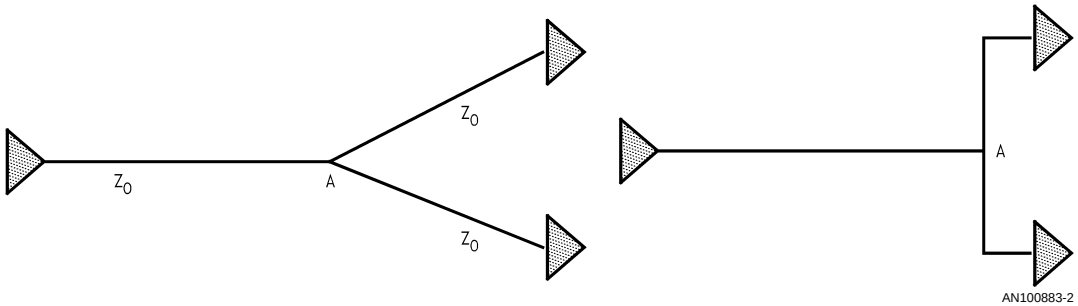

FIGURE 2. Avoid Y and T Configurations for Multi-drop Applications

STUBS & TERMINATION

Stubs are defined as the branch off the main line to the receiver inputs. These should be kept as short as possible to ensure that they appear as a lumped load to the transmission line and that a reflection does not occur at the high impedance inputs of the receiver. Stubs occur at the input of every receiver, including the last receiver. If PCB real estate is available the final receiver's layout may include the termination resistor(s). If PCB real estate is tight at the final receiver, then a fly-by termination may be employed. This is shown in *Figure 3*.

Stubs should be no longer than 1 inch in length, and the shorter the better. The use of surface mount chip resistors for the termination is recommended due to their small form factor, and low parasitics. 0805 packages are commonly employed.

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

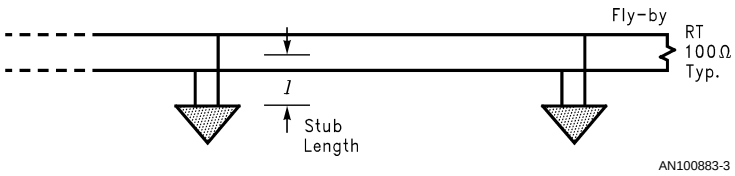

FIGURE 3. Fly-by Termination Provides Room for the Termination

LVDS PCB TECHNIQUES:

LVDS features fast edge rates, therefore the interconnect between transmitters and receivers will act as a transmission line. The PCB traces that form this interconnect must be designed with care. The following general guidelines should be adhered to:

- Hand route or review very closely auto-routed traces.
- Locate the Transmitters and Receivers close to the connectors to minimize PCB trace length for off PCB applications.
- Traces should be laid out for differential impedance control (space between traces needs to be controlled). See *Figure 4* and AN-905 for equations.
- Minimize the distance between traces of a pair to maximize common mode rejection.
- Place adjacent LVDS trace pairs at least twice as far away (as the distance between the conductors of the pair) (see *Figure 4*).
- Place TTL/CMOS (large dV signals) far away from LVDS, at least three times (>3S) away or on a different signal layer. (See *Figure 4*.)
- Match electrical length of all LVDS lines.
- Keep stubs as short as possible.
- Avoid crossing slots in the ground plane.
- Avoid 90˚ bends (use two 45s).
- Minimize the number of via on LVDS traces.
- Maintain equal loading on both traces of the pair to preserve balance.
- Match impedance of PCB trace to connector to media (cable) to termination to minimize reflections (emissions) for cabled applications (typically 100Ω differential mode impedance).
- Select a termination resistor to match the differential mode characteristic impedance of the interconnect, 2% tolerance is recommended.
- Locate the termination within 1/2 (<1) inch of the receiver inputs if not using a fly-by termination method.
- Use surface mount components to minimize parasitic L & C for bypass caps and termination resistors.
- Use a 4 layer PCB (minimum).
- Bypass each LVDS package at the device pin (Bulk bypass nearby also) with parallel capacitors (0.1 µF//0.01 µF//0.001 µF) on each of the supply pins (V_{CC}, $LVDSV_{CC}$, and $PLLV_{CC}$).

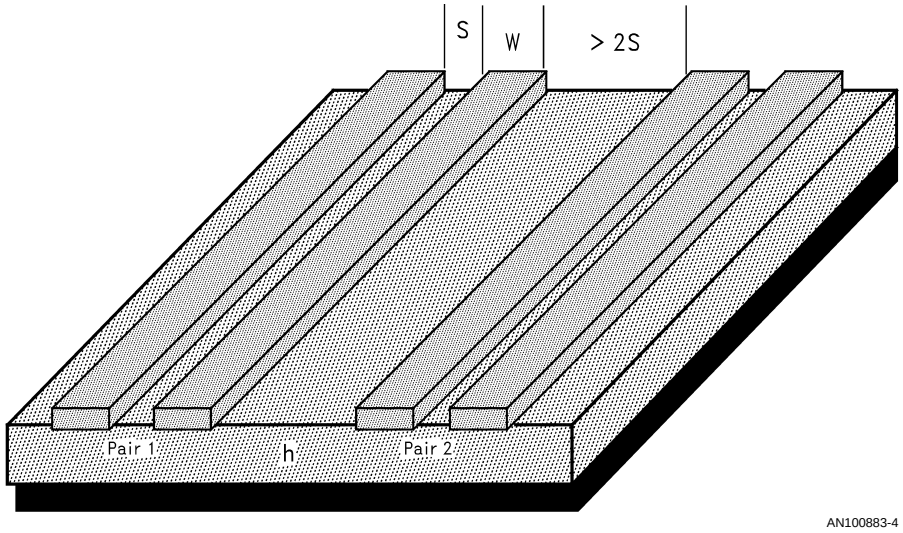

FIGURE 4. Differential Trace Layout (See AN-905)

SUMMARY

Channel-Link provides a versatile high speed data transmission system. It allows for many possibilities of configurations and deployments solving unique problems to special application needs. This application note focused on a distribution application where a Channel-Link Transmitter is connected to several Receivers. Bus configuration along with PCB recommendations were presented. Following these recommendations and guidelines will help ensure that the signal fidelity on the interconnect is maintained and supports error-free transmission.

REFERENCE

For additional information on Channel-Link applications and operation, please see the following application notes located on the National website at:

www.national.com

Topic	AP-Note ##
Channel-Link Overview	AN-1041
Sampling Margin and Skew Budgets	AN-1059
Parallel Application of Channel-Links	AN-1084

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com
www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated