LMH1981

Improving Video Clock Generation in Modern Broadcast Video Systems

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Improving Video Clock Generation in Modern Broadcast Video Systems

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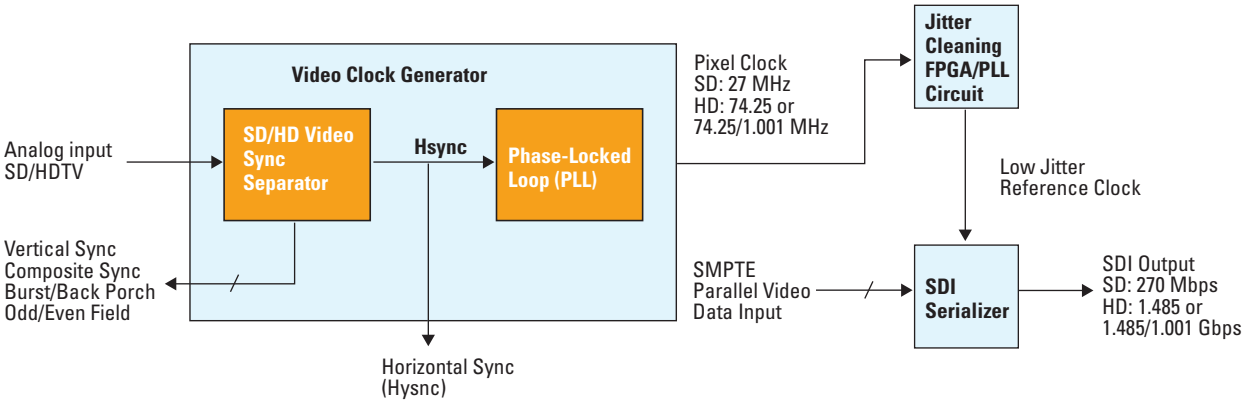

Figure 1. SDI Reference Clock Generator Block Diagram

The old adage "timing is everything" is well embodied in the modern broadcast studio, where precise timing of video clock and synchronization signals are essential to create, acquire, edit, and distribute analog and digital video. Today's broadcast systems must support industry-standard SD/HD formats, such as NTSC, PAL, 720p, 1080i, and 1080p, over analog and digital interfaces such as composite, component, and Serial Digital Interface (SDI). With high-speed SDI video equipment being increasingly used throughout the studio, improved video sync separation can more effectively produce video clocks with low jitter, which is crucial to meeting the stringent specifications of new SDI standards.

A video clock generator which generates various timing and clock signals from an analog video input consists of a video sync separator and Phase-Locked Loop (PLL). These two circuits are illustrated in the SDI application block diagram in *Figure 1*.

The video sync separator accepts a $1V_{p-p}$ analog video input with bi-level or tri-level sync and extracts the standard timing signals, such as Horizontal (Hsync), vertical, and composite sync, burst/back porch, and odd/even field outputs. To meet strict timing requirements of the latest HDTV standards, specifications such as HD tri-level sync separation, low output propagation delay, and 50% sync slicing are imperative. The latter ensures precise sync extraction by slicing at the proper 50% point of the bi-level or tri-level sync reference edges. This provides for improved Hsync jitter performance compared to non-adaptive, fixed-level sync slicing, even under irregular input conditions such as double or no 75Ω load termination or transmission loss. Hsync jitter is defined here as the peak-to-peak time variance in Hsync's falling-edge with respect to the input's sync reference-edge and is critical to the performance of the pixel clocks generated by the subsequent PLL block.

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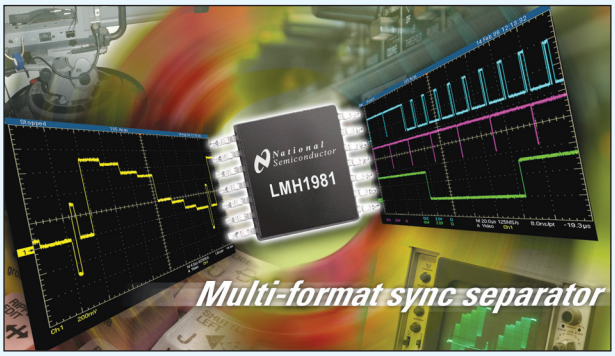
Featured Products

Multi-Format Video Sync Separator

The LMH1981 is a multi-format sync separator for high-definition broadcast and professional video systems. The device automatically detects the input video format and performs all the necessary sync separation to generate low-jitter horizontal and vertical sync signals for standard and high-definition video formats, including NTSC, PAL, SECAM, 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p.

The LMH1981 features the timing outputs needed for any video system, including horizontal, vertical and composite sync, odd/even field, burst/back porch clamp, and a patented automatic video-format detection feature. The device accepts both bi- and tri-level sync video inputs and features 50% slicing to ensure accurate separation of signals that vary in amplitude, offset, and noise. The device has a wide input range, allowing the inputs to accept video signals from 500 mV_{P-P} to 2 V_{P-P}.



Features

- 50% sync slicing
- Low jitter horizontal sync output
- Supports NTSC, PAL, SECAM, 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p
- Accepts video signals from 500 mV_{P-P} to 2 V_{P-P}
- No external programming with µC required
- Horizontal sync output propagation delay <50 ns

The LMH1981 is ideal for use in a wide range of video applications such as, broadcast video equipment, video distribution, DTV and HDTV systems, and is available in TSSOP-14 packaging.

For FREE samples, datasheets, and more, visit
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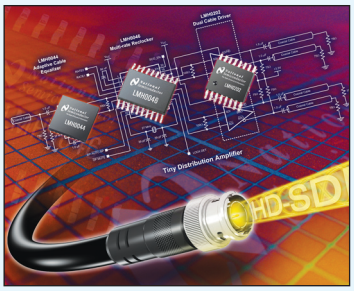
Adaptive Cable Equalizer



The LMH0044 adaptive cable equalizer is a monolithic integrated circuit for equalizing data transmitted over cable (or any media with similar dispersive loss characteristics). The equalizer operates over a wide range of data rates from 143 Mbps to 1.485 Gbps and supports SMPTE 292M, SMPTE 344M, and SMPTE 259M. This device implements DC restoration to correctly handle pathological data conditions (DC restoration may be bypassed for low data rate applications). The equalizer may be driven in either a single-ended or differential configuration.

Additional features include separate carrier detect and output mute pins which may be tied together to mute the output when no signal is present. A programmable mute reference is provided to mute the output at a selectable level of signal degradation.

Features

- SMPTE 292M, SMPTE 344M, and SMPTE 259M compliant
- High data rates: 143 Mbps to 1.485 Gbps
- Equalizes up to 200m of Belden 1694A at 1.485 Gbps or up to 400m of Belden 1694A at 270 Mbps
- 208 mW typical power consumption with 3.3V supply
- Manual bypass and output mute with a programmable threshold
- Single-ended or differential input
- Supports DVB-ASI at 270 Mbps
- 50Ω differential outputs
- Single 3.3V supply operation

The LMH0044 is ideal for SMPTE 292M/344M/259M serial interfaces, serial digital data equalization and reception, and data recovery equalization. The LMH0044 is available in LLP-16 packaging.

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Improving Video Clock Generation in Modern Broadcast Video Systems

The PLL block can generate one or more pixel clocks, which should be phase-locked to the leading-edge of Hsync, the PLL's reference input. To produce both SD and HD pixel clocks will require two PLLs, both designed to give the appropriate output frequency for any given Hsync frequency. Since the PLL derives a higher frequency pixel clock from a lower frequency Hsync, pixel clock jitter will be determined by different sources at different frequencies. Below the loop bandwidth, the clock jitter output by the PLL will be dominated by Hsync jitter, which can be a significant amount depending on the performance and quality of the sync separator. Above the loop bandwidth, it will be dominated by its PLL oscillator, typically a Voltage-Controlled Crystal Oscillator (VCXO) chosen properly for low phase noise and frequency tuning, among other characteristics.

In the block diagram, a pixel clock generator is used to derive a reference clock for an SDI serializer which receives SMPTE-compliant parallel digital video data and then encodes, serializes, and transmits uncompressed serial digital video over coax cable. A serializer requires a clean reference clock for its internal PLL to generate a bit rate clock that maintains the serializer and clocks its output bit-stream. If used to directly clock the serializer, any jitter on the reference clock could potentially transfer to the bit rate clock and consequently appear as SDI output jitter. As shown in ***Table 1***, SDI formats use increasingly high data rates and thus require clock sources with sufficient jitter performance.

For example, SMPTE 292M specifies the "timing" and "alignment" jitter requirements for an HD-SDI serializer's output bit-stream. Referring to the table, timing jitter should not be more than 1.0 UI[1] for jitter frequency components from B1 to B3, or 10 Hz to 1485 MHz, per SMPTE 292M. Alignment jitter—which is the high-frequency subset of timing jitter—should be no more than 0.2 UI from B2 (100 kHz) to B3. Outside of their respective frequency limits, both the timing and alignment jitter specifications roll off at 20 dB per decade. Output jitter above the jitter specifications can result in degradation of error performance at the SDI deserializer. Please see the SDI standards for more information.

The stringent jitter specifications of SDI standards demonstrate the profound need for a low-jitter pixel clock. In most cases, however, a generated pixel clock will have an intolerable amount of jitter, up to 6 ns_{p-p} for a typical SD pixel clock, which precludes direct application as a reference clock. Jitter reduction is therefore required to improve such unacceptable clock performance. The most common way to reduce pixel clock jitter is to use jitter-cleaning circuitry, usually implemented with additional Field-Programmable Gate Array (FPGA) or PLL stages. While jitter-cleaning circuitry is routinely applied by system designers, this can add significantly to component count, PCB area, power, and design cost and time.

A more effective way to reduce pixel clock jitter and thus improve SDI output jitter is to use a broadcast-quality video sync separator that has very low Hsync jitter, such as the LMH1981. This improved performance gives designers the flexibility to use smaller FPGAs or otherwise reduce jitter-cleaning circuitry and still produce an SDI output that complies to the jitter specifications.

Although broadcast systems are rapidly transitioning to high-speed SDI formats, the need to generate accurate video clocks from analog sources to process digital video data will be around for years to come. Current solutions require extensive jitter-cleaning circuits for generating an accurate reference clock to produce a SMPTE-compliant SDI output. However, the most fundamental and effective solution is to minimize jitter on the most critical timing reference, Hsync. This can only be accomplished using a high-performance analog video sync separator such as the LMH1981 in the clock generation signal path because, as we now know, timing is everything. ■

Access interactive broadcast video solutions diagrams at solutions.national.com

Table 1

Format	Standard	Bit Rate	Output Timing Jitter (B1 to B3)*	Output Alignment Jitter (B2 to B3)*
SD-SDI Standard- definition	SMPTE 259M, 334M	270 Mbps, others not widely used	1.0 UI[1] or 3.7 ns_{p-p}	0.2 UI or 740 ps_{p-p}
HD-SDI High-Definition; HD/SD-SDI Mulit-rate	SMPTE 292M	1.485 Gbps 1.485/1.001 Gbps	1.0 UI or 673 ps_{p-p}	0.2 UI or 135 ps_{p-p}
3-Gbps SDI up to 1080p/60 over a single link	SMPTE 424M	2.970 Gbps 2.970/1.001 Gbps	2.0 UI or 673 ps_{p-p}	0.3 UI maximum, 0.2 UI recommended

*B1, B2, and B3 are the jitter frequency band limits specified in the SMPTE standards.
[1]One UI, or Unit Interval, is equal to one bit period (1/bit rate) of the serial bit-stream.

Featured Products

Digital Video Serializer with Ancilliary Data FIFO and Integrated Cable Driver

The LMH0030 is a monolithic integrated circuit that encodes, serializes, and transmits bit-parallel digital video data. The serial data clock frequency is internally generated and requires no external frequency setting, trimming, or filtering components. The LMH0030 performs functions which include: parallel-to-serial data conversion, SMPTE standard data encoding, NRZ to NRZI data format conversion, serial data clock generation and encoding with the serial data, automatic video rate and format detection, ancillary data packet management and insertion, and serial data output driving.

Features

- SDTV/HDTV serial digital video standard compliant
- Supports 270 Mbps, 360 Mbps, 540 Mbps, 1.4835 Gbps, and 1.485 Gbps SDV data rates with auto-detection
- Low output jitter: 85 ps (typ), 125 ps (max)
- Low power consumption: 430 mW (typ) from 3.3V
- No external VCO required
- Fast PLL lock time: < 150 µs (typ) at 1.485 Gbps
- LVCMOS compatible data and control inputs and outputs
- 75Ω ECL-compatible, differential, serial cable-driver outputs
- 3.3V I/O power supply and 2.5V logic power supply operation

The LMH0030 SDTV/HDTV serial-to-parallel digital video interfaces for video cameras, VTRs, telecines, digital video routers and switchers, digital video processing and editing equipment, video test pattern generators and digital video test equipment, and video signal generators. The LMH0030 is available in TQFP-64 packaging.

For FREE samples, datasheets, and more, visit
www.national.com/pf/LM/LMH0030.html

Digital Video Deserializer / Descrambler with Video and Ancillary Data FIFOs

The LMH0031 is a monolithic integrated circuit that deserializes and decodes SMPTE 292M, 1.485 Gbps (or 1.483 Gbps) serial component video data, to 20-bit parallel data with a synchronized parallel word-rate clock. It also deserializes and decodes SMPTE 259M, 270 Mbps, 360 Mbps, and SMPTE 344M (proposed) 540 Mbps serial component video data, to 10-bit parallel data. Functions performed by the LMH0031 include clock/data recovery from the serial data, serial-to-parallel data conversion, SMPTE standard data decoding, NRZI-to-NRZ conversion, parallel data clock generation, word framing, CRC and EDH data checking and handling, Ancillary Data extraction, and automatic video format determination.

Features

- SDTV/HDTV serial digital video standard compliant
- Supports 270 Mbps, 360 Mbps, 540 Mbps, 1.483 Gbps, and 1.485 Gbps serial video data rates with auto-detection
- Low power: 850 mW (typ)
- Uses 27 MHz crystal or clock oscillator reference
- Fast VCO lock time: < 500 µs at 1.485 Gbps
- Built-in self-test and video test pattern generator
- LVDS and ECL-compatible, differential, serial inputs
- 3.3V I/O power supply and 2.5V logic power supply operation

The LMH0031 SDTV/HDTV serial-to-parallel digital video interfaces for video editing equipment, VTRs, standard converters, digital video routers and switchers, digital video processing and editing equipment, video test pattern generators and digital video test equipment, and video signal generators. Operating over the commercial temperature range (0°C to +70°C), the LMH0031 is available in TQFP-64 packaging.

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