DS15BA101,DS15EA101,DS25BR110

Extending the Signal Path Over Data Transmission Lines Using LVDS Signal Conditioning

Literature Number: SNLA209

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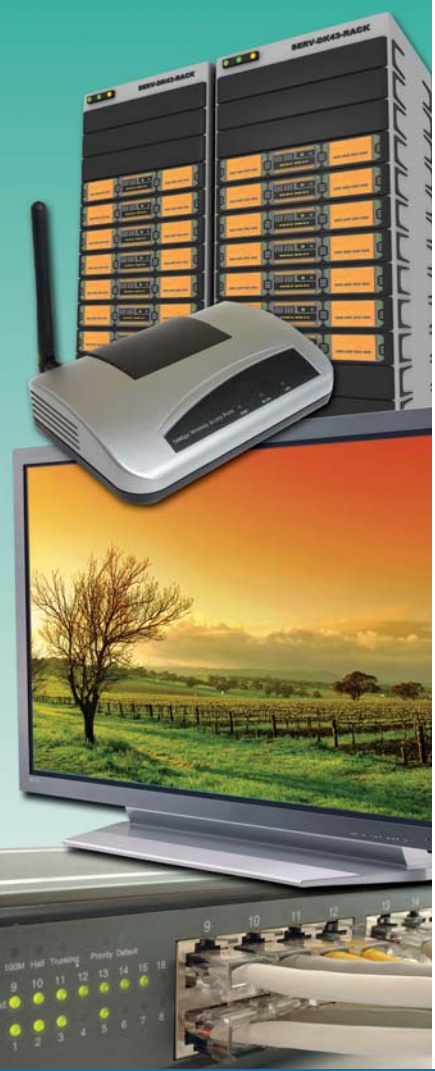

Extending the Signal Path Over Data Transmission Lines

— By Lee Sledjeski, Applications Engineer

After using an ADC to convert an RF signal to the digital domain, this signal often needs to be sent across a backplane or cable to an FPGA for additional processing. As sampling speeds continue to increase, the challenge becomes driving this signal more than a few dozen centimeters without bit errors. This article examines how to solve the challenges of extending high-speed signal paths over FR-4 traces and copper cables.

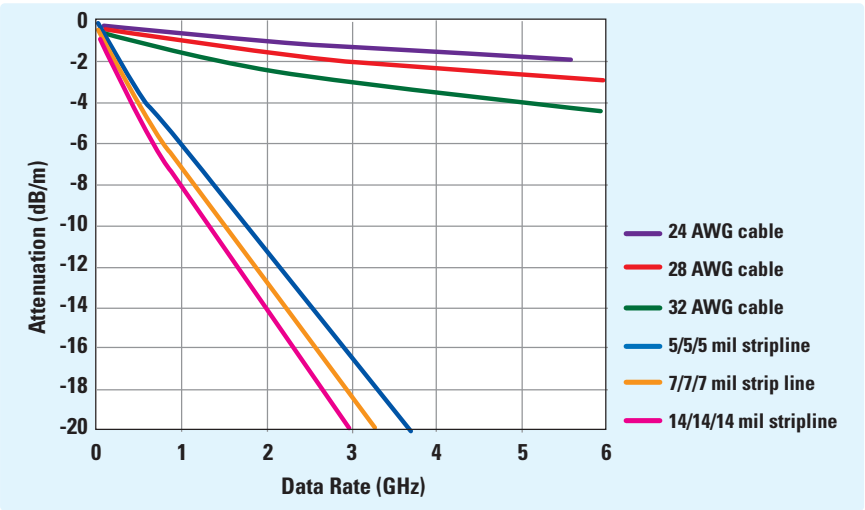

Figure 1. Transmission Media Loss (Differential) Shows the Low Pass Filter Effect

As an example of these high-speed signal challenges, consider the graph in ***Figure 1***. When a 2.5 Gbps NRZ signal transitions every bit cycle it generates the equivalent of a 1.25 GHz clock signal. This component of the 2.5 Gbps signal sees up to 10 dB loss after just 1 meter of 100Ω differential FR-4 stripline. It takes as much as 10 meters of twinaxial cable to generate a similar media loss. This transmission loss creates jitter that eventually closes the signal "eye" or sampling window as seen in ***Figure 2a***.

For high-speed signals, a low pass filter (***Figure 1***) represents the transmission media. The highest frequency that passes through the media with less than 3 dB of attenuation defines the filter bandwidth. Signal components within the

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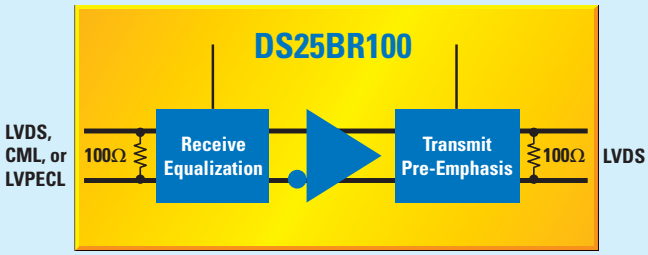

Signal Conditioning

Product ID	LVDS Buffer Function	Inputs	Outputs	Input Compatibility	Output	Pre-emphasis (dB)	Receive Equalization (dB)	Max Speed/Ch (Mbps)	Packaging	Comments
DS25BR100	Single	1	1	LVDS/LVPECL/CML	LVDS	0/6	3/6	3125	LLP-8	Int termination, 8 kV ESD
DS25BR110	Single	1	1	LVDS/LVPECL/CML	LVDS	—	0/3/6/9	3125	LLP-8	Int termination, 8 kV ESD
DS25BR120	Single	1	1	LVDS/LVPECL/CML	LVDS	0/3/6/9	—	3125	LLP-8	Int termination, 8 kV ESD
DS90LV804	Quad	4	4	LVDS/LVPECL/CML	LVDS	—	—	800	LLP-32	Int termination, 15 kV ESD
DS90LV004	Quad	4	4	LVDS/LVPECL/CML	LVDS	0/2/4/6	—	1500	TQFP-48	Int termination, 15 kV ESD
DS15BR400	Quad	4	4	LVDS/LVPECL/CML	LVDS	0/6	—	2000	LLP-32, TQFP-48	Int termination, 15 kV ESD
DS15BR401	Quad	4	4	LVDS/LVPECL/CML	LVDS	0/6	—	2000	LLP-32, TQFP-48	15 kV ESD

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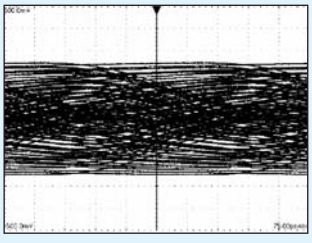
media bandwidth pass through with minimal attenuation. Furthermore, the media attenuates the amplitude of signal components and harmonics beyond the -3 dB point or transmission line bandwidth. Data-dependent jitter due to Inter-Symbol Interference (ISI) results from this non-linear, frequency-dependent loss. Therefore, signal conditioning refers to the compensation techniques used to mitigate the effects of high-frequency transmission losses. Conditioning input and output signals enhance the performance and extend the signal-path distance.

Input and Output Signal Conditioning

Measured at the Equalizer Input

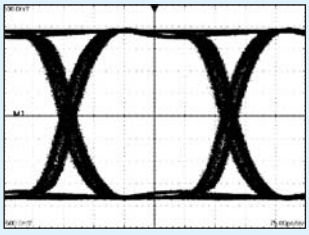


2.5 Gbps NRZ PRBS-7 after 70" Differential FR-4
Stripline V:100 mV/DIV, H:75 ps/DIV

Figure 2a. 2.5 Gbps NRZ Signal After 70 Inches of FR-4 Without Equalization

Signal integrity designers use equalizers to condition input signals. The equalizer circuit goal is to reverse the signal losses incurred during transmission by "flattening" the frequency response of the system and thereby reducing the distortion or "smearing" that the signal encounters. The equalizer flattens the transmission frequency response by acting as a high-pass filter that approximately complements the low-pass effect of the transmission medium within the signal's frequency band. As a general rule of thumb, the equalization should flatten the frequency response up to the frequency produced by the highest transition density data pattern possible. For example, a 2.5 Gbps data rate signal in a 1-0-1-0 NRZ pattern would require a flat frequency response out to 2.5 GHz (***Figure 1***). When properly tuned, equalization can significantly reduce the ISI effects from the transmission media as shown in ***Figure 2b***. Even for 29.5" stripline, attenuation

Measured at the Equalizer Output



Equalized 2.5 Gbps NRZ PRBS-7 after 70" Differential FR-4
Stripline V:100 mV/DIV, H:75 ps/DIV

Figure 2b. 2.5 Gbps NRZ Signal After 70 Inches of FR-4 With Equalization (b)

approaches -6 dB at 2.5 Gbps, and it is safe to say that reliable communication across the transmission link requires some equalization.

High-speed devices such as the DS25BR110 feature a receiver input equalization circuit to reduce the effects of frequency dependent losses caused by the transmission medium (***Figure 2***). Four levels of EQ control ranging from 0 to 16 dB allow for easy optimization of signal quality across a broad range of typical transmission media lengths.

Transmitter output signal conditioning is used to produce a similar overall net effect. While input equalization acts to cancel frequency-dependent losses, output Pre-Emphasis (PE) alters the frequency content of a clean, unattenuated signal with the expectation that the transmission media attached to the driver will attenuate the signal. This results in a clean signal at the receiver positioned on the far end of the transmission line. By applying PE to the output waveform, the highest frequency components of the signal are emphasized at the driving device. Because signal conditioning requirements increase with higher data rates, multiple levels from 0 to 9 dB can be selected to optimize the signal integrity at the receiver for most common PCB and copper cable transmission distances (***Figure 3***).

Setting Pre-Emphasis and Equalization

Signal conditioning is designed to compensate for the low-pass filter effect of the transmission medium. As a starting point, adjust the level to match the loss of

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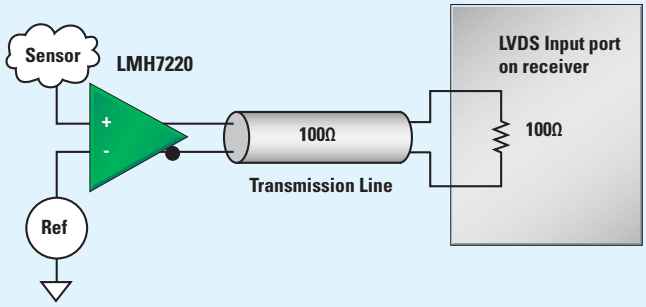

ADC12V170 and ADC14V155 Features

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- Dual 3.3V, 1.8V supply operation
- Dual data rate parallel LVDS outputs
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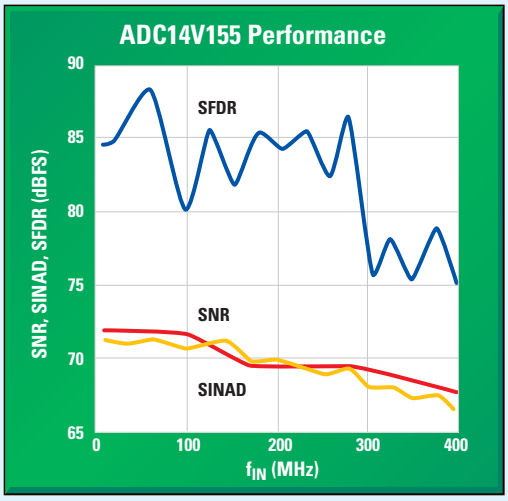
- Internal sample-and-hold circuit
- Internal precision 1.0V reference
- Available in LLP-48 packaging (7 x 7 x 0.8mm)



Product ID	Resolution (Bits)	Speed (MSPS)	Output Format	Power (mW)	SNR (dB)	SFDR (dB)	Packaging
ADC14V155	14	155	DDR Parallel LVDS	951	71.7	86.9	LLP-48
ADC12V170	12	170	DDR Parallel LVDS	781	67.2	85.8	LLP-48
ADC14155	14	155	CMOS	967	71.3	87.0	LLP-48
ADC12C170	12	170	CMOS	715	67.2	85.4	LLP-48

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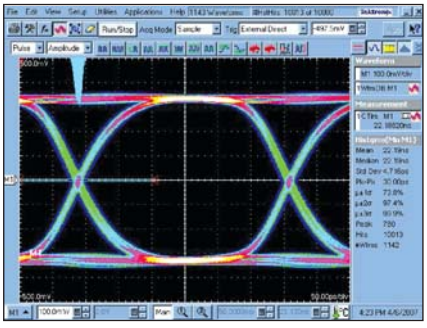
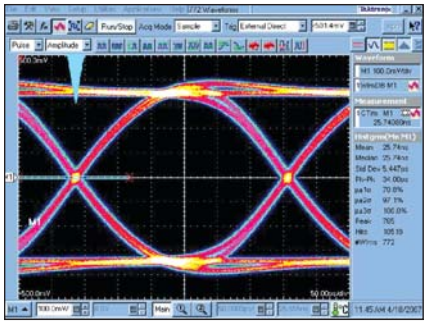
a.



DS25BR120 Pre-Emphasis: OFF
3.125 Gbps with a PRBS7 pattern
Output load: 4" FR-4 100Ω differential trace

b.



DS25BR120 Pre-Emphasis: ON (6 dB setting)
3.125 Gbps with a PRBS7 pattern
Output load: 20" FR-4 100Ω differential trace

Figure 3. 3.125 Gbps LVDS Output Without Pre-Emphasis After 4" FR-4 (a), and With PE After 20" FR-4 (b)

your transmission line at the primary frequency of interest, tweaking one level up and down to ensure optimal quality of the received waveform eye pattern. When considering signal conditioning, the primary frequency of interest is normally the data rate divided by 2 (e.g., for a 2.5 Gbps signal use 2.5÷2=1.25 GHz, for a 1 Gbps signal use 500 MHz). This is the frequency of the data pattern with the highest level of attenuation. A network analyzer is the easiest way to generate a loss graph like that in ***Figure 1***. If a network analyzer is unavailable, it is also possible to send a sine wave at the frequency of interest across your transmission line and use the attenuation value as your loss value.

Input EQ, output signal conditioning, or a combination of both can be used to compensate for lossy transmission lines. Each method has advantages and disadvantages and the choice of which one to use depends on the application and personal preference. Output PE has the advantage of being easily measurable. Its effect is visible at the receiver and can be easily monitored and adjusted. Receive EQ is often used in crosstalk-sensitive and low-power applications since it does not add extra energy to the transmission line. In very lossy applications where EQ or PE alone is not sufficient, both input and output signal conditioning may need to be used in combination, e.g. 9 dB of pre-emphasis with 9 dB of receive equalization.

Should I use LVDS or CML?

Discrete LVDS implementations can be used effectively to data rates in excess of 3 Gbps. Current Mode Logic (CML) is the I/O of choice at speeds of 3.5 Gbps (***Figure 4***) and beyond. LVDS generally has lower power and less EMI and is well-defined as an interface standard. CML is capable of higher speeds and typically has higher drive strength than LVDS. Either signaling technology can often be used at rates between 1 and 3.125 Gbps so a good translation strategy is important for optimal signal integrity.

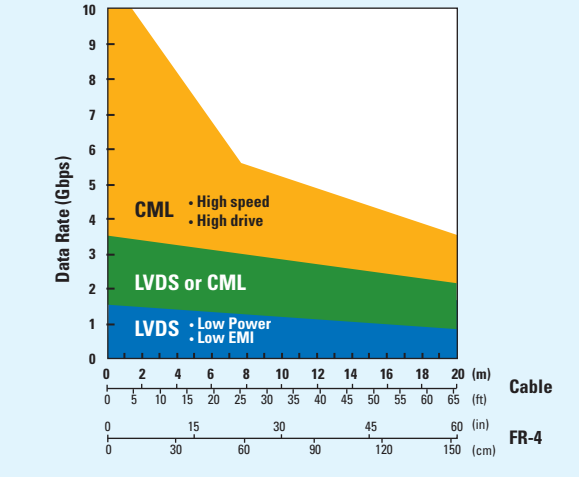


Figure 4: Typical LVDS and CML Applications

For successful level translation, the driver's differential output voltage (V_{OD}) and common mode voltage (V_{CM}) must fall within the receiver's input range. For LVDS the V_{OD} (as defined in the EIA/TIA-644A standard) is the voltage difference across the driver outputs with a 100Ω resistive load.

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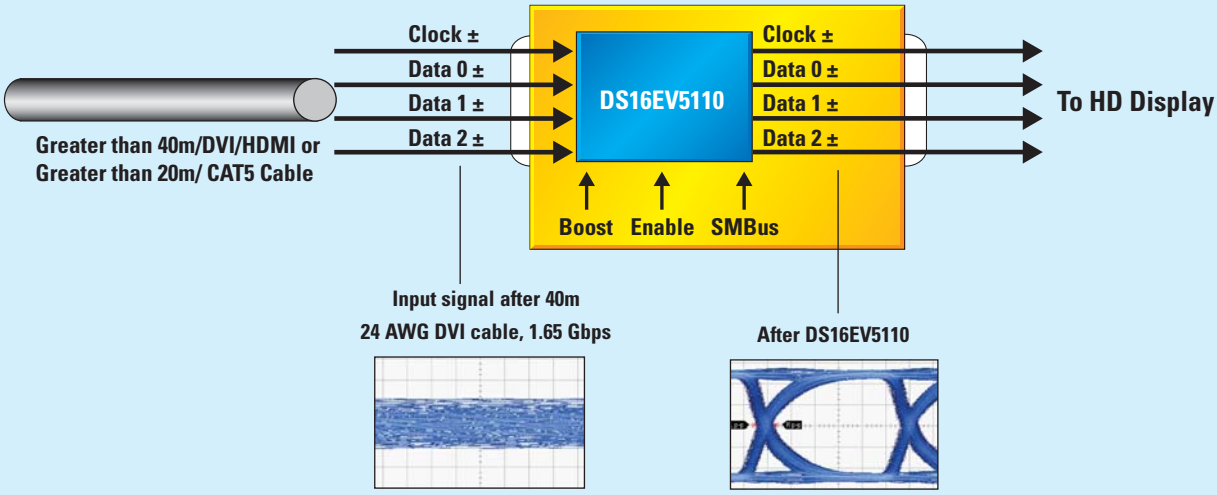

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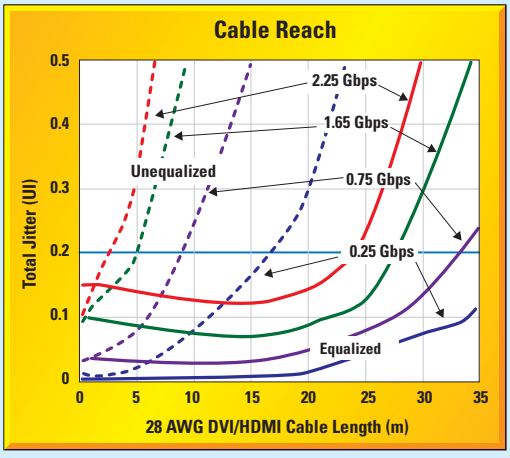

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Other differential standards specify the output voltage amplitude as a peak to peak number. As an example, a 400 mV LVDS V_{OD} is exactly equal in amplitude to an 800 mV peak-to-peak CML output, but located at a different offset voltage with respect to GND.

LVDS receiver devices offer the greatest flexibility of any differential technology because their wide input common mode range easily accepts the signal swings of 1.2V/1.5V/2.5V CML and LVPECL differential I/O. This allows for a direct DC connection between most differential outputs and LVDS inputs, minimizing the added PCB real estate and cost of multiple AC-coupling capacitors.

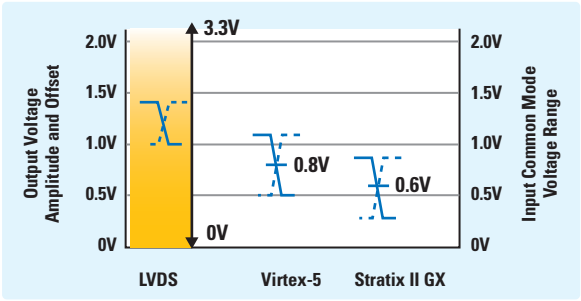

Figure 5. Standard and FPGA Differential I/O Signaling Levels

The LVDS transmitter output V_{OD} is specified to be 250 mV minimum (500 mV peak-to-peak) for high performance with low EMI and low-power consumption. Adding output signal conditioning enables LVDS to drive extended lengths of cable or large backplanes. The LVDS output rides on a 1.2V common mode voltage developed from an internal bandgap reference and can be DC coupled to many LVPECL inputs. CML inputs with a limited common mode range, however, require an AC-coupled interface because the LVDS output voltage swing does not meet the minimum common mode requirements for most CML inputs.

Many LVDS and CML buffer chips offer pre-emphasis and/or receive equalization to boost signals coming from ADCs, DACs, FPGAs, and DSPs, and some have multiplexing functions for switching/redundancy applications. A low-power solution for redundancy, multiplexing, and signal distribution can be achieved with a combination of high-performance LVDS crosspoint switches and high-speed FPGA CML I/O. Programming CML outputs for 600 mV to 800 mV will reduce transmit power expended by the FPGA integrated SerDes, lower the overall EMI signature of the interface, and provide the optimum signal for LVDS inputs with EQ.

The latest generation FPGAs with CML I/O have common-mode output voltages lower than the nominal 1.2V stated in the LVDS standard (***Figure 5***). The extended input common mode range allows the high-speed FPGA I/O to interoperate with LVDS devices.

Driving Over 20 Meters

LVDS and CML signal conditioners are capable of extending signal paths up to a maximum of 20m at multi-Gbps speeds. For longer distances, Ethernet can be used but requires additional protocol and timing overhead to fit the signal path raw data into Ethernet packets. Alternatively, a cable driver and adaptive equalizer can be used to extend serialized data up to 100s of meters. The DS15BA101/EA101 is a 1.5 Gbps cable extension chipset for 100Ω twisted pair and 50Ω coaxial cables up to hundreds of meters. Unlike many other signal conditioners with equalization, this chipset automatically compensates for various cable lengths and types. Adaptive equalization is critical to the success of long distance cable driving. The adaptive nature of the equalizer ensures minimal added signal noise and jitter caused during the amplification of high-frequency energy. An evaluation reference design, number DriveCable02EVK, is available for quick evaluation and design implementation.

Conclusion

Today many signal paths contain separate signal acquisition and processing modules. As sampling speeds increase, it becomes harder to transfer the signal-path data between modules due to the lossy effects of the transmission medium. In fact, even if the transmission distance is constant, losses and therefore jitter increases as signaling speed increases. Luckily, it is easy to estimate and overcome these loss effects through the use of signal conditioners with pre-emphasis and equalization. ■

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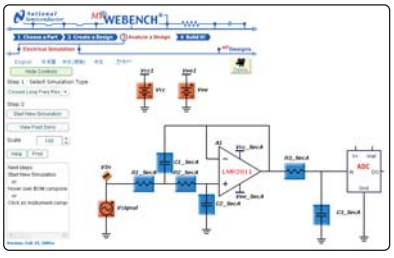

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