National Semiconductor™

Channel Link Demonstration Kit User Manual

P/N CLINK3V48BT-112

Rev 2.2

Interface Products

Information contained in this document is subject to change

Table of Contents:

Introduction

National Semiconductor's Interface Products Group Channel Link demo kit contains a Transmitter (Tx) demo board and a Receiver (Rx) demo board along with an interface cable. This kit will demonstrate the chipsets transmitting data streams using Low Voltage Differential Signaling (LVDS) through a cable at seven times the input clock rate.

The Transmitter board accepts 3V TTL/CMOS data signals from an incoming data source along with the clock signal. The LVDS Transmitter converts the TTL/CMOS parallel lines into serialized LVDS pairs. The serial data streams toggle at 7 times the clock speed.

The Receiver board accepts the LVDS serialized data (and clock) and converts them back into parallel 3V TTL/CMOS data out signals.

The user needs to provide the proper data inputs to the Transmitter and also to provide a proper interface from the Receiver output to the receiver devices. A cable harness scramble may be necessary depending on type of cable/connector interface used.

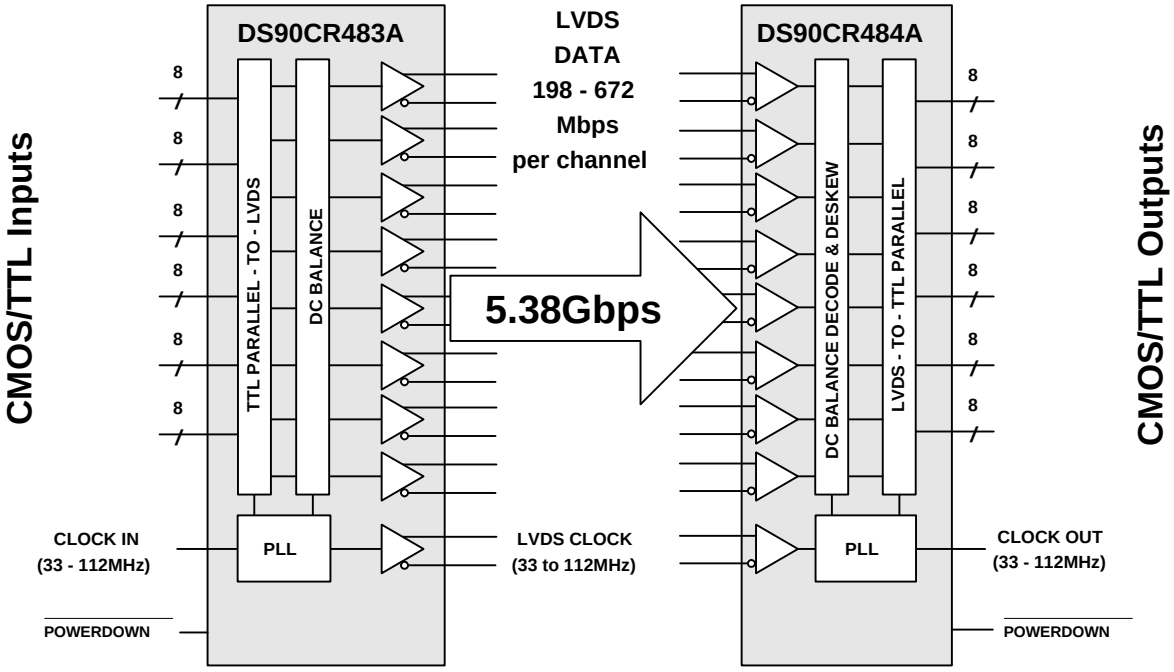
Warnings:
The maximum voltage that should ever be applied to the Channel Link Transmitter or Receiver Vcc is 4V. The Transmitter and Receiver power supply pins (Vccs) are **NOT** 5V tolerant. The Transmitter can however accept a 3.3V or 5V TTL/CMOS level on the inputs (TxIN). The Transmitter inputs are 5V tolerant. The maximum voltage that can be applied to any input pin is 5.0V.

Contents of Demo Kit

1) One Transmitter board* with IDC connectors on Tx input
   DS90CR483AVJD - 48 bit Transmitter
2) One Receiver board* with IDC connectors on Rx output
   DS90CR484AVJD - 48 bit Receiver
3) One 2-meter 3M MDR LVDS Cable interface to connect TxOUT to RxIN. Note: The MDR footprint has been set to accept a D26-1 pinout.
4) Demonstration Kit Documentation
5) DS90CR483A/484A Datasheet

*Note: The demo board trace layout is designed for minimum skew between channels. It is not absolutely required in most applications but be aware that the skew margins will be reduced if your board layout is not optimized.

Applications



Channel Link Application

The diagram above illustrates the use of the Chipset (Tx/Rx). This chipset is able to transmit 48 bits of TTL/CMOS data using eight LVDS channels at the speed of 5.38Gbps.

Refer to the proper datasheet information on Chipsets (Tx/Rx) provided on each board for more detailed information.

Tx Features and Explanations

Pre-emphasis (PRE - pin 14/JP1):

1. This feature enables you to overcome cable capacitance through the LVDS interface. This function provides additional instantaneous current during switching transitions. NOTE: This function does NOT affect Rx output drive.
2. It affects Tx A0-A7 and CLKs LVDS outputs only.
3. To disable this function, pin 14 must be tied “low”. LVDS output drive will then be at its standard value of 3.5mA.
4. The input will be pulled low (0.7V) if no jumper is used. To adjust the level of pre-emphasis, place a jumper on JP1 to Vcc. R48 will now be connected. R48 is a 2K potentiometer. Use a number 1.4mm jewelers screwdriver to adjust R48. Turning clockwise will increase the pre-emphasis value. Turning counterclockwise will decrease the pre-emphasis value. R48 should be adjusted to reduce overshoot. Too much pre-emphasis can create an overshoot condition at the rising edge and an undershoot condition on the falling edge. Icc will increase but allows you to drive longer cables. Too little pre-emphasis will not allow you to drive longer cables. Monitor any one of the LVDS lines (A0-A7) or CLK1 for a visual confirmation of its effect. It is recommended that you monitor the LVDS signals with a differential probe. If a differential probe is not used, a single ended probe can be used for a quick check.

PLL range select (PLLSEL - pin 15/JP5):

1. High-range is selected by tying pin 15 “high”.
2. Low-range is selected by tying pin 15 “low”. This feature provides lower noise in the lower range of the PLL.

NOTE: Refer to the “Application Notes” on the back of the data sheet for complete description of each feature.

Rx Features and Explanations

PLL range select (PLLSEL - pin 5/JP5):

1. High-range is selected by tying pin 5 HIGH.
2. Low-range is selected by tying pin 5 LOW. This feature provides lower noise in the lower range of the PLL.

NOTE: Refer to the “Application Notes” section on the back of the data sheet for complete description of each feature.

How to hook up the demo boards (overview)

The Tx demo board TxIN has been laid out to accept two 50 pin IDC connectors from the incoming data. The TxOUT/RxIN interface uses the 3M MDR connector and 3M MDR cable with a D26-1 pin out. This combination provides minimal skew between LVDS channels.

1) Connect one end of the D26-1 MDR cable to the transmitter board and the other end to the receiver board. This is a standard pinout cable, longer lengths are available for purchase from 3M - see http://www.mmm.com
2) Jumpers have been configured from the factory (Refer to Tx and Rx "Jumper Default Settings" on pages 11 and 16) to run in normal mode with pre-emphasis ON. Jumpers are also provided on both boards so make sure that they are positioned correctly. See pages 8 and 16 for different configurations.
3) From the incoming data, connect the appropriate IDC cable to the transmitter board and connect two (2) 50-pin IDC cables from the receiver boards to the receiver load. Note that pin 1 on the connector should be connected to pin 1 of the cable.
4) Power for the Tx and Rx boards are supplied externally through Test Pad (TP) TP1. Grounds for both boards are connected through TP2.

Power Connections

The Transmitter and Receiver boards can only be powered by supplying power externally through TP1 (Vcc) and TP2 (GND). The **maximum voltage** that should ever be applied to the Channel Link Transmitter or Receiver **Vcc is 4V**. For the transmitter and the receiver to be operational, /PD must be tied to Vcc which is labeled as “JP3” and "JP1", respectively.

Note: J4 on Tx and J1 on the Rx provide the interface for LVDS signals.

Transmitter Board

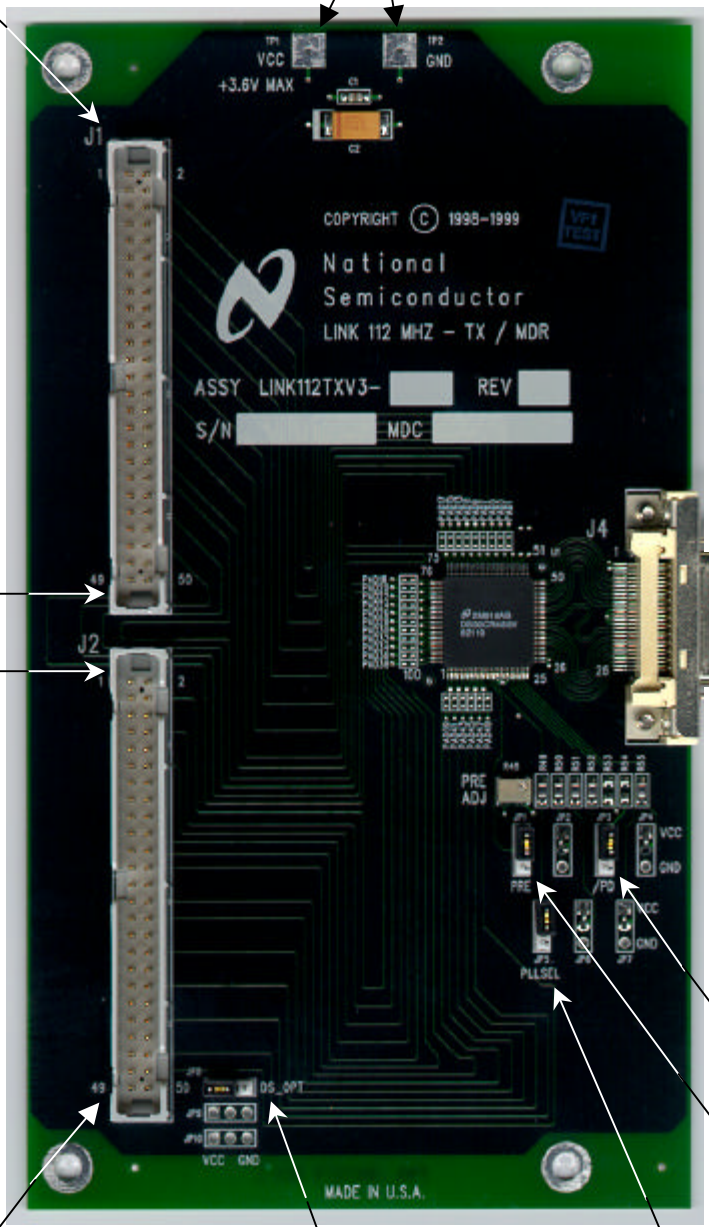
J1

gnd	$TxIN_{47}$
gnd	$TxIN_{46}$
gnd	$TxIN_{45}$
gnd	$TxIN_{44}$
gnd	$TxIN_{43}$
gnd	$TxIN_{42}$
gnd	$TxIN_{41}$
gnd	$TxIN_{40}$
gnd	$TxIN_{39}$
gnd	$TxIN_{38}$
gnd	$TxIN_{37}$
gnd	$TxIN_{36}$
gnd	$TxIN_{35}$
gnd	$TxIN_{34}$
gnd	$TxIN_{33}$
gnd	$TxIN_{32}$
gnd	$TxIN_{31}$
gnd	$TxIN_{30}$
gnd	$TxIN_{29}$
gnd	$TxIN_{28}$
gnd	$TxIN_{27}$
gnd	$TxIN_{26}$
gnd	$TxIN_{25}$
gnd	$TxIN_{24}$
gnd	*gnd*

gnd	$TxIN_{23}$
gnd	$TxIN_{22}$
gnd	$TxIN_{21}$
gnd	$TxIN_{20}$
gnd	$TxIN_{19}$
gnd	$TxIN_{18}$
gnd	$TxIN_{17}$
gnd	$TxIN_{16}$
gnd	$TxIN_{15}$
gnd	$TxIN_{14}$
gnd	$TxIN_{13}$
gnd	$TxIN_{12}$
gnd	$TxIN_{11}$
gnd	$TxIN_{10}$
gnd	$TxIN_{9}$
gnd	$TxIN_{8}$
gnd	$TxIN_{7}$
gnd	$TxIN_{6}$
gnd	$TxIN_{5}$
gnd	$TxIN_{4}$
gnd	$TxIN_{3}$
gnd	$TxIN_{2}$
NC	$TxIN_{1}$
NC	$TxIN_{0}$
DS_ OPT	**CLKIN**

J2

Vcc and Gnd **MUST** be applied **externally** here



TxOUT LVDS signals
3M MDR connector

PIN #	NAME
1	***NC***
2	*GND*
3	**A0+**
4	**A1+**
5	**A2+**
6	**CLK+**
7	*GND*
8	*GND*
9	**A3+**
10	**A4+**
11	**A5+**
12	**A6+**
13	**A7+**
14	***NC***
15	**A0-**
16	**A1-**
17	**A2-**
18	**CLK-**
19	*GND*
20	*GND*
21	**A3-**
22	**A4-**
23	**A5-**
24	**A6-**
25	**A7-**
26	*GND*

J4

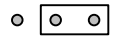
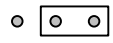
/PD

PRE

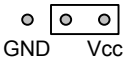
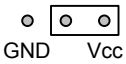
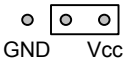
PLLSEL

DS_OPT

Selectable jumper settings for the Tx board

Jumper	Purpose	Settings
PRE (JP1)	**PRE**-emphasis	 = NONE  = ON GND Vcc GND Vcc (NONE: NO pre-emphasis; ON: pre-emphasis is adjusted through R48) When NO jumper is used, pre-emphasis is at 0.7V value.
/PD (JP3)	**P**ower**D**own	 = OFF  = ON GND Vcc GND Vcc (OFF: Tx powers down; ON: Tx is operational)
PLLSEL (JP5)	**PLL SEL**ect (High-range)	 = LOW  = HIGH GND Vcc GND Vcc (LOW: High-range OFF; HIGH: High-range ON)

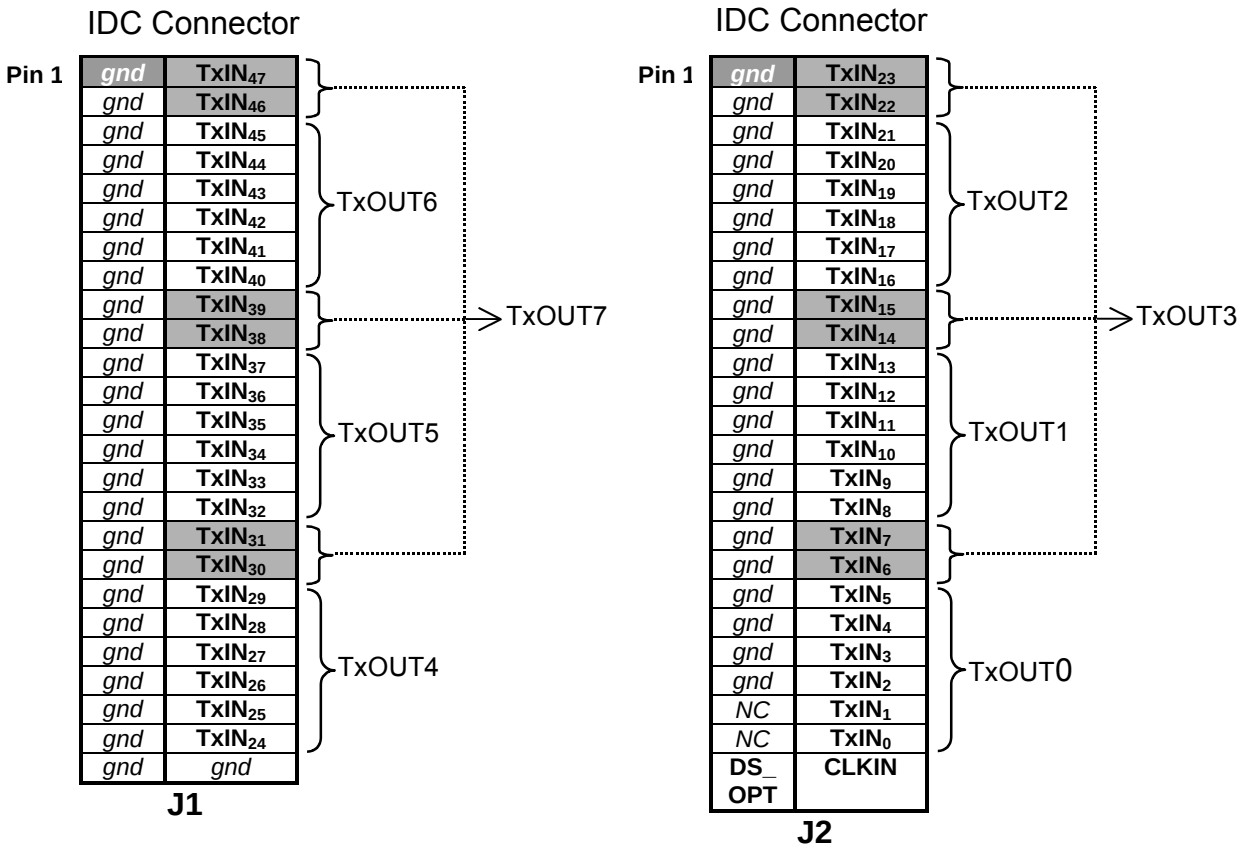
Tx Jumper Default Settings

Jumper Name	Purpose	Settings	Jumper Number
PRE	**PRE**-Emphasis[1]		JP1
/PD	**P**ower**D**own		JP3
PLLSEL	**PLL SEL**elect (High-range)		JP5

[1] An adjustable potentiometer (2K ohm) is mounted at location R48. This allows pre-emphasis to be adjusted (only if JP1 has a jumper to VCC). Use a number 1.4mm jewelers screwdriver to adjust R48. Turning clockwise will increase the pre-emphasis value. Turning counterclockwise will decrease the pre-emphasis value. R48 should be adjusted to reduce overshoot. If no jumper is used, the pre-emphasis value will be 0.7V.
See Tx Features and Explanations (Page 6) - Pre-Emphasis for description of feature.

LVDS Mapping by IDC Connector

The following two figures show how the Tx inputs are mapped to the IDC connector and to each of the eight LVDS channels.



Transmitter Board

Tx Optional: Parallel Termination for TxIN

On the Tx demo board, there are 50 inputs that have an 0402 pad on one side and the other side tied to ground. These pads are unpopulated from the factory but are provided if the user needs to adjust the input termination to match the impedance of the input signal. PAD1 TO PAD48 are associated with the Tx data input lines. PAD49 is associated with CLKIN.

Mapping for Transmitter Inputs for the Optional Parallel Termination Resistors:

Tx Pin Names	Tx Pin Number	Parallel Termination Resistor
TxIN0	10	PAD48
TxIN1	9	PAD47
TxIN2	8	PAD46
TxIN3	7	PAD45
TxIN4	6	PAD44
TxIN5	5	PAD43
TxIN6	4	PAD42
TxIN7	3	PAD41
TxIN8	2	PAD40
TxIN9	1	PAD39
TxIN10	100	PAD38
TxIN11	99	PAD37
TxIN12	96	PAD36
TxIN13	95	PAD35
TxIN14	94	PAD34
TxIN15	93	PAD33
TxIN16	92	PAD32
TxIN17	91	PAD31
TxIN18	90	PAD30
TxIN19	89	PAD29
TxIN20	88	PAD28
TxIN21	87	PAD27
TxIN22	86	PAD26
TxIN23	85	PAD25
TxIN24	84	PAD24

Tx Pin Names	Tx Pin Number	Parallel Termination Resistor
TxIN25	81	PAD23
TxIN26	80	PAD22
TxIN27	79	PAD21
TxIN28	78	PAD20
TxIN29	77	PAD19
TxIN30	76	PAD18
TxIN31	75	PAD17
TxIN32	74	PAD16
TxIN33	73	PAD15
TxIN34	72	PAD14
TxIN35	71	PAD13
TxIN36	70	PAD12
TxIN37	69	PAD11
TxIN38	66	PAD10
TxIN39	65	PAD9
TxIN40	64	PAD8
TxIN41	63	PAD7
TxIN42	62	PAD6
TxIN43	61	PAD5
TxIN44	60	PAD4
TxIN45	59	PAD3
TxIN46	58	PAD2
TxIN47	57	PAD1
CLKIN	11	PAD49

BOM (Bill of Materials)

Bill of Materials CLINK_112_MHz_Tx_RevC_Bom

Type	Pattern	Value	Designators
3M_MDR_D26-1 Qty = 1			J4
3_PIN_HEADER Qty = 10	.1" spacing		JP1 JP2 JP3 JP4 JP5 JP6 JP7 JP8 JP9 JP10
25X2_IDC_CONN Qty = 2			J1 J2
PAD Qty = 52	0402		PAD1 PAD2 PAD3 PAD4 PAD5 PAD6 PAD7 PAD8 PAD9 PAD10 PAD11 PAD12 PAD13 PAD14 PAD15 PAD16 PAD17 PAD18 PAD19 PAD20 PAD21 PAD22 PAD23 PAD24 PAD25 PAD26 PAD27 PAD28 PAD29 PAD30 PAD31 PAD32 PAD33 PAD34 PAD35 PAD36 PAD37 PAD38 PAD39 PAD40 PAD41 PAD42 PAD43 PAD44 PAD45 PAD46 PAD47 PAD48 PAD49 PAD50 PAD51 PAD52
CAP Qty = 2	CC0805	.001uF	C4 C10
CAP Qty = 4	CC0805	.01uF	C5 C6 C8 C11
CAP Qty = 5	CC0805	.1uF	C1 C3 C7 C9 C12
DS90CR483A Qty = 1			U1
POT Qty = 1		10Kohm	R48
RES Qty = 7		10ohm	R49 R50 R51 R52 R53 R54 R55
TESTPAD_.2"X.2" Qty = 2			TP1 TP2
CAP100P Qty = 4	CAP100P	10uF	C2 C13 C14 C15

Receiver Board

Vcc and Gnd **MUST** be applied **externally** here

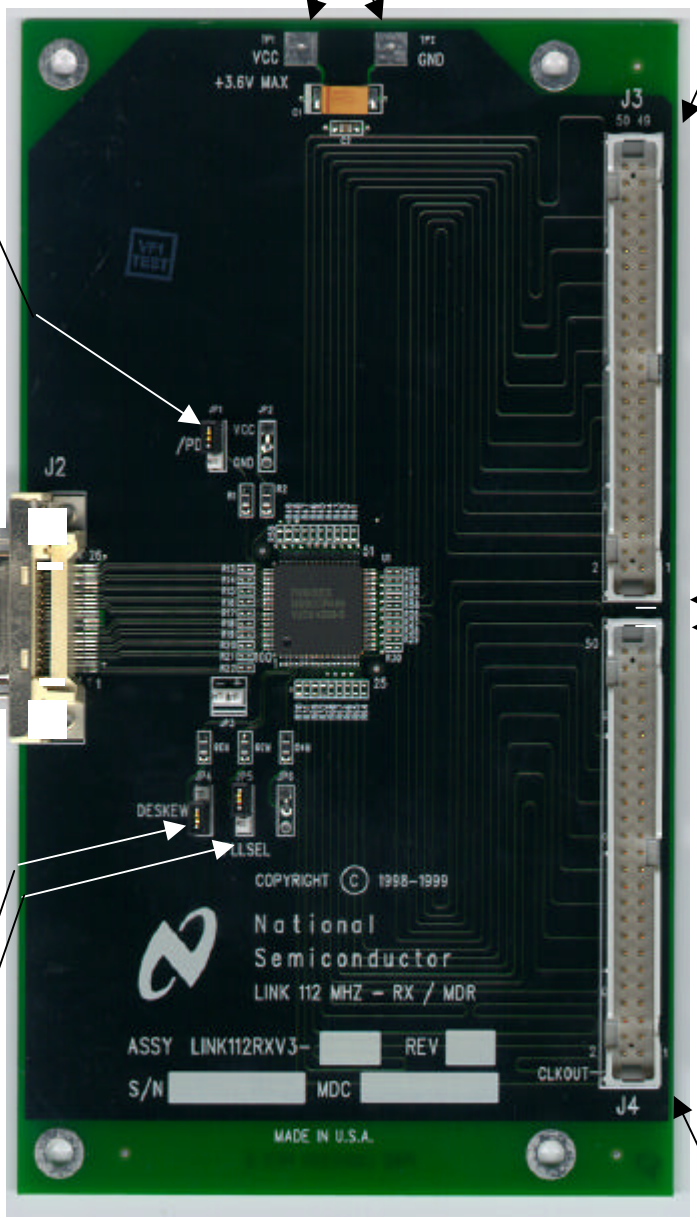
PowerDown (bar) Jumper

RxIN LVDS signals
3M MDR connector

PIN #	NAME
1	***NC***
2	*GND*
3	**A0+**
4	**A1+**
5	**A2+**
6	**CLK+**
7	*GND*
8	*GND*
9	**A3+**
10	**A4+**
11	**A5+**
12	**A6+**
13	**A7+**
14	***NC***
15	**A0-**
16	**A1-**
17	**A2-**
18	**CLK-**
19	*GND*
20	*GND*
21	**A3-**
22	**A4-**
23	**A5-**
24	**A6-**
25	**A7-**
26	*GND*

J2

DESKEW Jumper
PLLSEL Jumper



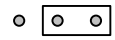
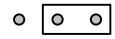
J3

$RxOUT_{47}$	*gnd*
$RxOUT_{46}$	*gnd*
$RxOUT_{45}$	*gnd*
$RxOUT_{44}$	*gnd*
$RxOUT_{43}$	*gnd*
$RxOUT_{42}$	*gnd*
$RxOUT_{41}$	*gnd*
$RxOUT_{40}$	*gnd*
$RxOUT_{39}$	*gnd*
$RxOUT_{38}$	*gnd*
$RxOUT_{37}$	*gnd*
$RxOUT_{36}$	*gnd*
$RxOUT_{35}$	*gnd*
$RxOUT_{34}$	*gnd*
$RxOUT_{33}$	*gnd*
$RxOUT_{32}$	*gnd*
$RxOUT_{31}$	*gnd*
$RxOUT_{30}$	*gnd*
$RxOUT_{29}$	*gnd*
$RxOUT_{28}$	*gnd*
$RxOUT_{27}$	*gnd*
$RxOUT_{26}$	*gnd*
$RxOUT_{25}$	*gnd*
$RxOUT_{24}$	*gnd*
gnd	***gnd***

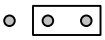
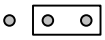
$RxOUT_{23}$	*gnd*
$RxOUT_{22}$	*gnd*
$RxOUT_{21}$	*gnd*
$RxOUT_{20}$	*gnd*
$RxOUT_{19}$	*gnd*
$RxOUT_{18}$	*gnd*
$RxOUT_{17}$	*gnd*
$RxOUT_{16}$	*gnd*
$RxOUT_{15}$	*gnd*
$RxOUT_{14}$	*gnd*
$RxOUT_{13}$	*gnd*
$RxOUT_{12}$	*gnd*
$RxOUT_{11}$	*gnd*
$RxOUT_{10}$	*gnd*
$RxOUT_{9}$	*gnd*
$RxOUT_{8}$	*gnd*
$RxOUT_{7}$	*gnd*
$RxOUT_{6}$	*gnd*
$RxOUT_{5}$	*gnd*
$RxOUT_{4}$	*NC*
$RxOUT_{3}$	*NC*
$RxOUT_{2}$	*NC*
$RxOUT_{1}$	*NC*
$RxOUT_{0}$	*NC*
CLKOut	***NC***

J4

Selectable jumper settings for the Rx board

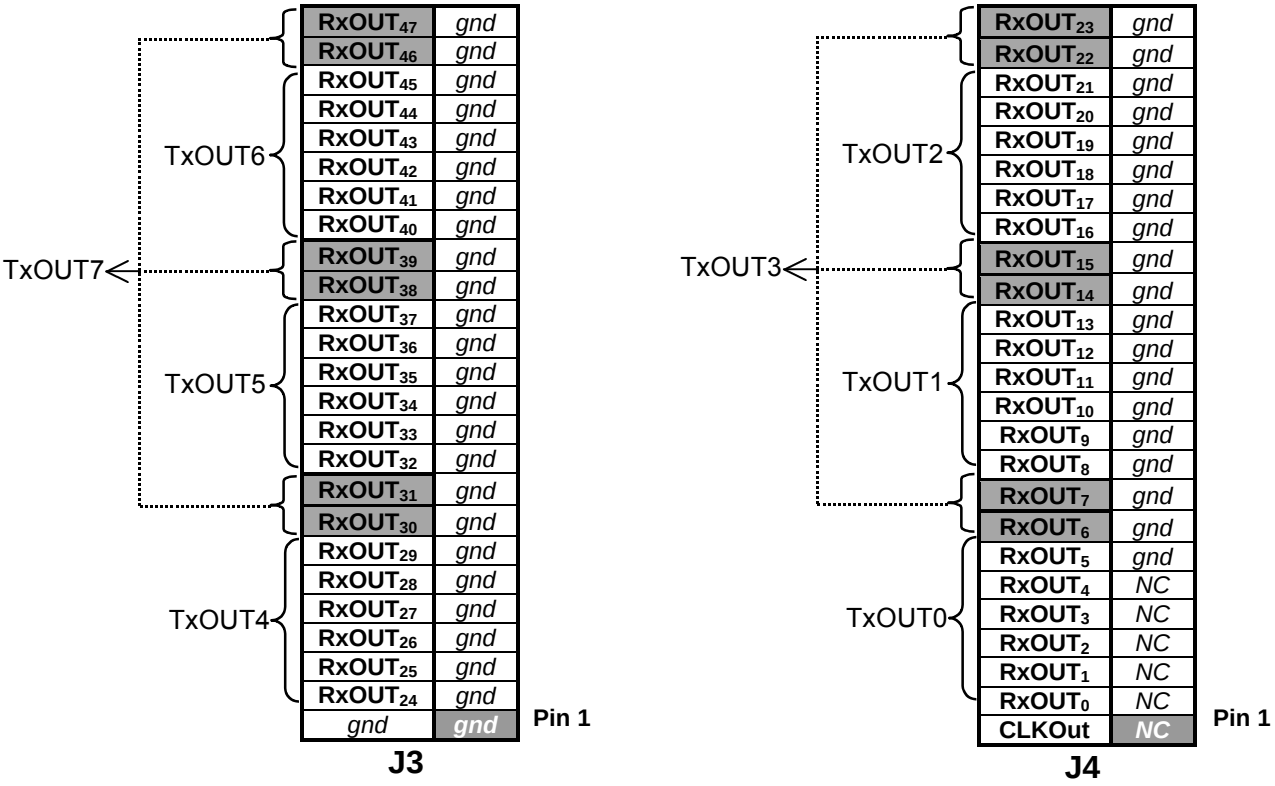
Jumper	Purpose	Settings
/PD (JP1)	**P**ower**D**own	 = OFF GND Vcc  = ON GND Vcc (OFF Tx powers down; ON Tx is operational)
PLLSEL (JP5)	**PLL SEL**ect (High range)	 = OFF GND Vcc  = ON GND Vcc

Rx Jumper Default Settings

Jumper Name	Purpose	Settings	Jumper Number
/PD	**P**ower**D**own – ON (Part is enabled)	 GND Vcc	JP1
PLLSEL	**PLL SEL**ect (High-range)	 GND Vcc	JP5

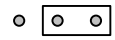
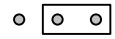
LVDS Mapping by IDC Connector

The following two figures show how the Rx outputs are mapped to the IDC connector and to each of the eight LVDS channels.

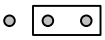
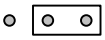


Receiver Board

Selectable jumper settings for the Rx board

Jumper	Purpose	Settings
/PD (JP1)	**P**ower**D**own	 = OFF GND Vcc  = ON GND Vcc (OFF Tx powers down; ON Tx is operational)
PLLSEL (JP5)	**PLL SEL**ect (High range)	 = OFF GND Vcc  = ON GND Vcc

Rx Jumper Default Settings

Jumper Name	Purpose	Settings	Jumper Number
/PD	**P**ower**D**own – ON (Part is enabled)	 GND Vcc	JP1
PLLSEL	**PLL SEL**ect (High-range)	 GND Vcc	JP5

BOM (Bill of Materials)

Bill of Materials CLINK_112_MHz_Rx_RevC_bom

Type	Pattern	Value	Designators
2_PIN_HEADER Qty = 1	.1" spacing		JP3
3M_MDR_D26--1 Qty = 1			J2
3_PIN_HEADER Qty = 5	.1" spacing		JP1 JP2 JP4 JP5 JP6
25X2_IDC_R Qty = 2			J3 J4
PAD Qty = 6	0402		PAD1 PAD2 PAD3 PAD4 PAD5 PAD6
CAP Qty = 2	CC0805	.001uF	C4 C10
CAP Qty = 4	CC0805	.01uF	C5 C6 C8 C11
CAP Qty = 5	CC0805	.1uF	C2 C3 C7 C9 C12
DS90CR484A Qty = 1			U1
R0402 Qty = 55		0ohm	R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R41 R42 R43 R44 R45 R46 R47 R48 R49 R50 R51 R52 R53 R54 R55 R56 R57 R58 R59 R60 R61 R62 R63 R64 R65 R66 R67 R68 R69 R70
Qty = 10		100ohm	R13 R14 R15 R16 R17 R18 R19 R20 R21 R22
RES Qty = 5		10ohm	R1 R2 R38 R39 R40
TESTPAD_.2"X.2" Qty = 2			TP1 TP2
CAP100P Qty = 4	CAP100P	10uF	C1 C13 C14 C15

Troubleshooting

If the demo boards are not performing properly, use the following as a guide for quick solutions to common problems. If the problem persists, contact the hotline number listed under Additional Information section of this document.

Check the following:
1. Power and Ground are connected to both Tx AND Rx boards.
2. Supply voltage (typical 3.3V) and current (It's around 200mA with clock and one data bit at 66MHz.) are correct.
3. Input clock and input data (It's best to start with one data bit.) to the Tx board.
4. Jumpers are set correctly or to default settings.
5. The 2 meter cable is connecting the Tx and Rx boards.
6. Make sure all of the connections are good.
7. Start with a low clock frequency (40 or 66 MHz) and work from there.

Trouble shooting chart:

Problem…	**Solution…**
There is only the output clock. There is no output data.	Make sure the data scramble/mapping is correct. Make sure there is data input.
No output data and clock.	Make sure Power is on. Input data and clock are active and connected correctly. Make sure that the 2 meter cable is secured to both demo boards.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the Power Down pins of both boards and make sure the devices are enabled (/PD=ON) for operation.
The devices are pulling more than 1A of current.	Check for shorts on the demo boards.
After powering up the demo boards, the power supply reads less than 3V when it is set to 3.3V.	Use a larger power supply that will provide enough current for the demo boards.

Additional Information

For more information on Channel-Link Transmitters/Receivers, refer to the National Semiconductor URL: http://www.national.com/pf/DS/DS90CR483A.html

Application Notes

- AN-1041 CHANNEL LINK Application Note
- AN-971 An Overview of LVDS technology
- AN-1035 PCB design guidelines using LVDS technology
- AN-977 LVDS Signal Quality: Jitter measurement using Eye pattern
- AN-1059 High Speed Transmission with LVDS Devices

Information available on the Internet: http://www.national.com/apnotes/ChannelLink.html

Interface Hotline:
The Interface Hotline number is: (408) 721-8500

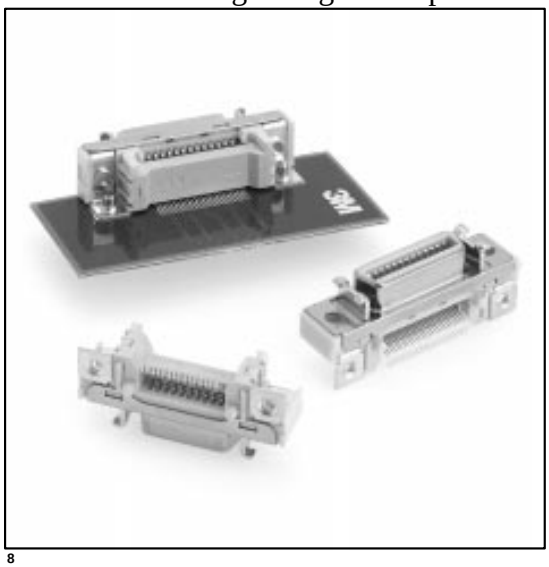
3M 26-Mini D Ribbon cable and connector

The next few pages provide a full description of the cable and connector. For product request please contact 3M.

3M Cable and Connector Data is available at: http://www.mmm.com/Interconnects

.050″ Mini D Ribbon (MDR) Connectors

Surface Mount Right Angle Receptacle — Shielded 102XX-1210VE Series



8

- Surface mount right angle shielded I/O receptacle
- MDR digital LCD interface — 20 and 26 position
- Ultra-low signal skew design for high data rate transmission
- Ribbon type contact — industry preferred
- Reliable repetitive plugging/unplugging
- Latch design for easy use
- Positions: 14,20, 26, 40 and 50

Date Modified: August 2, 1999

TS-0755-06
Sheet 1 of 3

Physical

Insulation	
Material:	Glass Reinforced Polyester (PCT)
Flammability:	UL 94V-0
Color:	Beige
Contact	
Material:	Copper Alloy (C521)
Plating	
Underplate:	80 μ″ [2.0 μm] Nickel — QQ-N-290, Class 2
Wiping Area:	20 μ″ [0.50 μm] Min Gold — MIL-G-45204, Type II, Grade C
Shroud and Latch Hook	
Material:	Steel
Plating:	Nickel
Screw Lock	
Material:	Copper Alloy (C521)
Plating:	Tin
Marking:	3M Logo and Part Number

Electrical

Current Rating:	1 A
Insulation Resistance:	$> 5 \times 10^8 \Omega$ at 500 VDC
Withstanding Voltage:	500 Vrms for 1 Minute

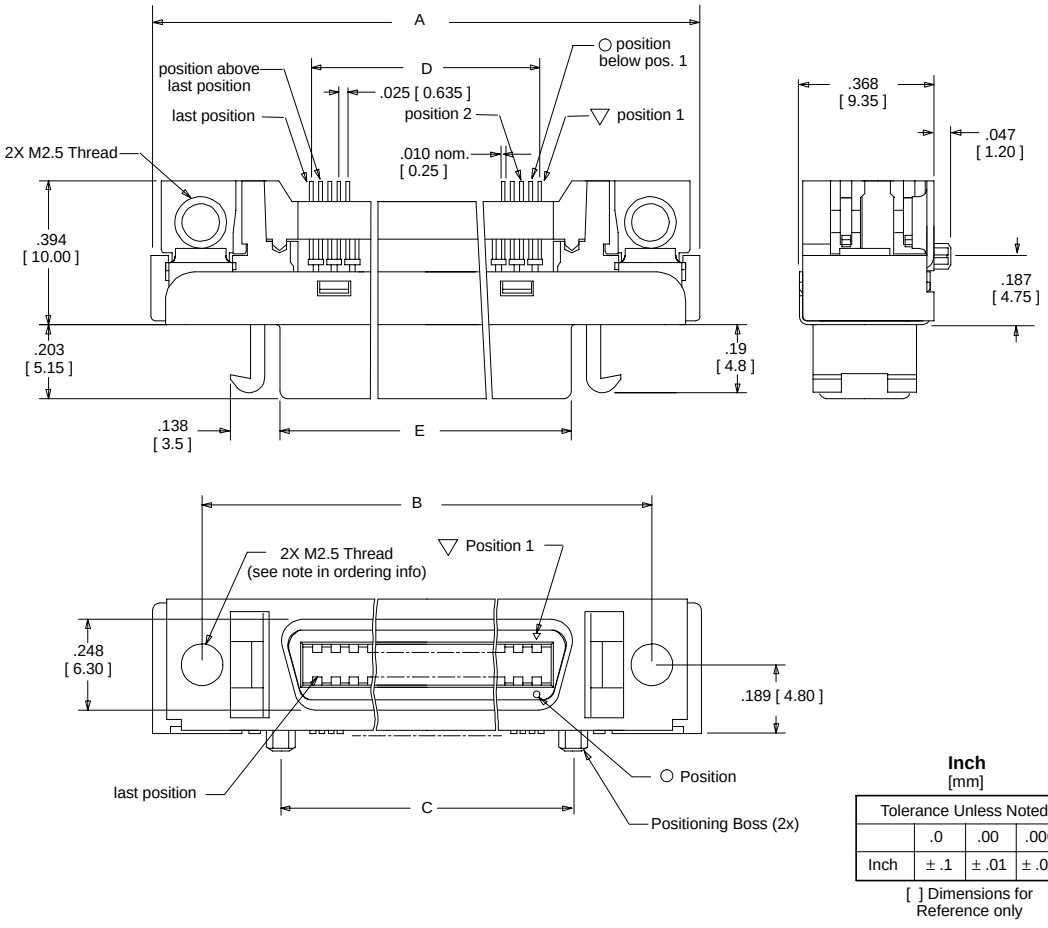
3M Interconnect Solutions Division
6801 River Place Blvd.
Austin, TX 78726-9000

For technical, sales or ordering information call
800-225-5373

.050″ Mini D Ribbon (MDR) Connectors

Surface Mount Right Angle Receptacle — Shielded 102XX-1210VE Series

Contact Quantity	3M Part Number	Dimensions				
		A±.008	B±.006	C±.006	D±.006	E±.006
14	**10214-1210 VE**	1.16 [29.5]	.93 [23.64]	.47 [12.70]	.33 [8.26]	.50 [12.6]
20	**10220-1210 VE**	1.32 [33.4]	1.081 [27.45]	.650 [16.51]	.475 [12.07]	.646 [16.4]
26	**10226-1210 VE**	1.50 [38.2]	1.231 [31.26]	.800 [20.32]	.625 [15.88]	.795 [20.2]
40	**10240-1210 VE**	1.85 [47.1]	1.581 [40.15]	1.150 [29.21]	.975 [24.77]	1.150 [29.2]
50	**10250-1210 VE**	2.06 [52.4]	1.831 [46.50]	1.400 [35.56]	1.225 [31.12]	1.40 [35.5]



Inch [mm]

Tolerance Unless Noted			
	.0	.00	.000
Inch	± .1	± .01	± .005

[ ] Dimensions for Reference only

Ordering Information

102XX-1210VE

Contact Quantity (See Table)

Note: Use (M2.5x8mm) screws to mount to panel with max. thickness of 2.0 mm.

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Sheet 2 of 3

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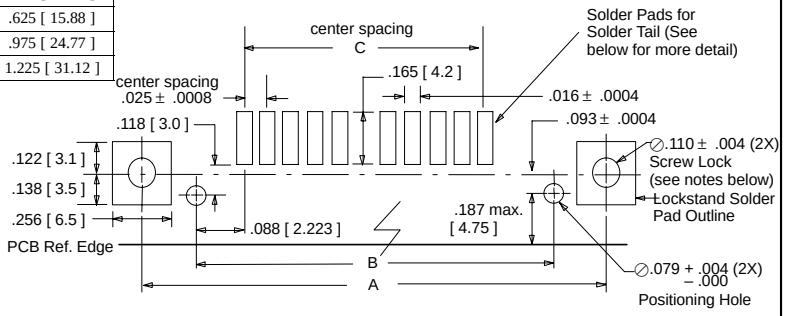
.050″ Mini D Ribbon (MDR) Connectors

Surface Mount Right Angle Receptacle — Shielded 102XX-1210VE Series

Contact Quantity	Dimensions		
	A ± .002	B ± .002	C ± .002
14	.930 [23.64]	.500 [12.70]	.325 [8.26]
20	1.081 [27.45]	.650 [16.51]	.475 [12.07]
26	1.230 [31.26]	.800 [20.32]	.625 [15.88]
40	1.581 [40.15]	1.150 [29.21]	.975 [24.77]
50	1.831 [46.50]	1.400 [35.56]	1.225 [31.12]

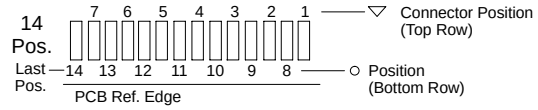
Recommended Board Layout

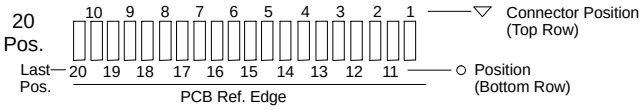
(viewed from connector side)

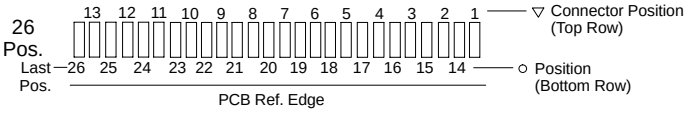


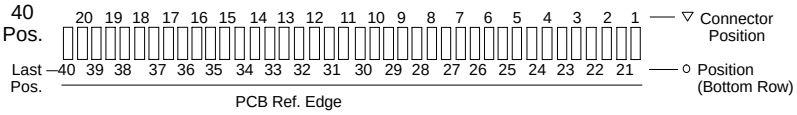
Solder Tail Layout Detail

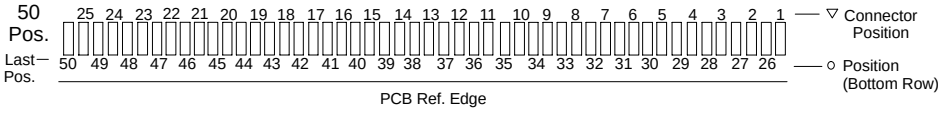
(#'s Correspond to Connector Contact # Shown on Previous Page)







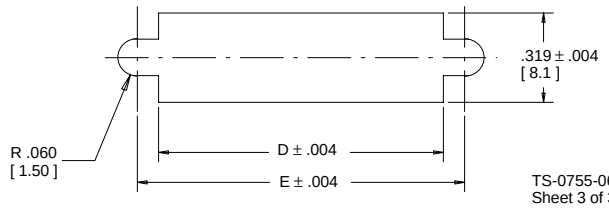




Contact Quantity	D	E
14	1.10 [19.9]	.931 [23.64]
20	.94 [23.8]	1.081 [27.45]
26	1.09 [27.6]	1.231 [31.26]
40	1.44 [36.5]	1.581 [40.15]
50	1.69 [42.8]	1.830 [46.50]

Recommended Panel Cut-out

Note: Panel thickness .079 [2.00] Max.



**Notes:

1. Plated through holes for .062″ board thickness.
2. Use mounting screws (M2.5) to fasten to board.

TS-0755-06
Sheet 3 of 3

.050″ Mini D Ribbon (MDR) Cable Assembly

High Speed Digital Data Transmission System — 26 Position 14526-EZHB-XXX-0QC

91

- 10 shielded pairs plus 4 individual wires
- The solution for high speed datacom and telecom applications
- Each differential pair is shielded with foil; entire cable bundle is shielded with foil and braid
- Rugged MDR ribbon type contact
- Quick release latches

Date Modified: February 23, 2000

TS-0891-05
Sheet 1 of 3

Physical

Connector Contact Plating
Wiping Area: 30μ″ [0.76μm] Min. Gold
Shell
Color: Parchment/Beige
Material: Acrylonitrile Butadiene Styrene (ABS)
Cable
Color: Parchment/Beige
Jacket Material: Polyvinyl Chloride (PVC)
Flammability: AWM VW-1

Electrical

Voltage Rating: 30 V
Current Rating: 1 A
Insulation Resistance: $> 1 \times 10^8 \Omega$ at @100 Vdc
Withstanding Voltage: 350 Vrms for 1 minute
Individually Shielded Twisted Pairs
Characteristic Impedance: $100 \pm 10\Omega$ (USB 90Ω)
Conductor Size: 28 AWG Stranded
Propogation Velocity: 1.25 ns/ft [4.1 ns/m]

Environmental

Temperature Rating: –20°C to +75°C

UL File No.: E86982

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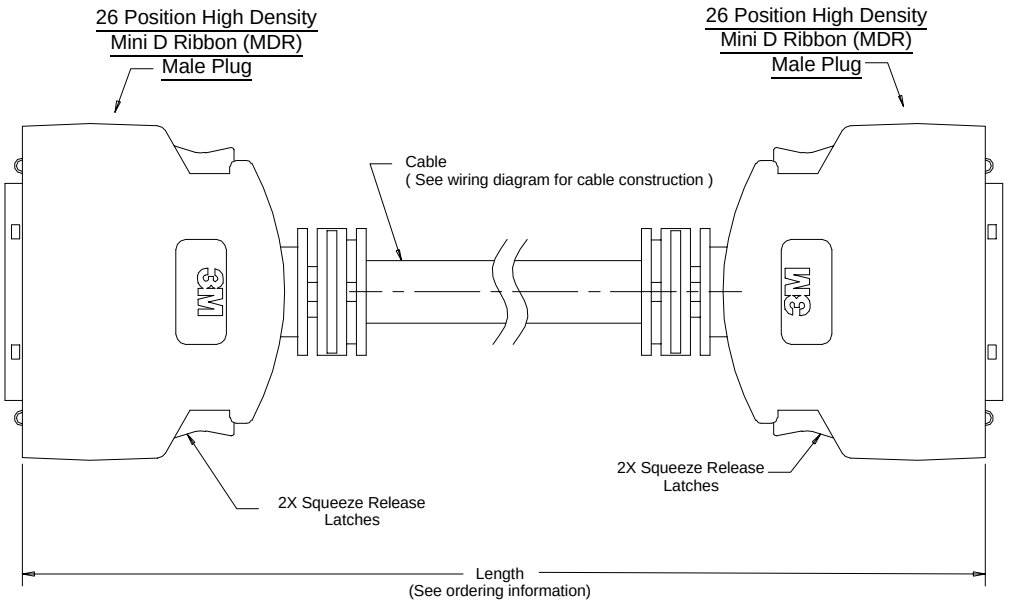
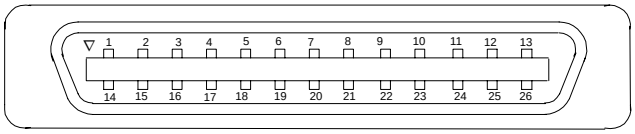
.050″ Mini D Ribbon (MDR) Cable Assembly

High Speed Digital Data Transmission System — 26 Position 14526-EZHB-XXX-0QC





MDR 26 Position Plug
(Both Ends)

Ordering Information

14526-EZHB-XXX-0QC

Length
100 = 1 meter
200 = 2 meter
500 = 5 meter
A00 = 10 meter

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Sheet 2 of 3

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3M - Preliminary Channel Link Cable

Rev A
3/3/99

Assembly Specification

Cable: v24.0

Connector: Plug type 10126-6000

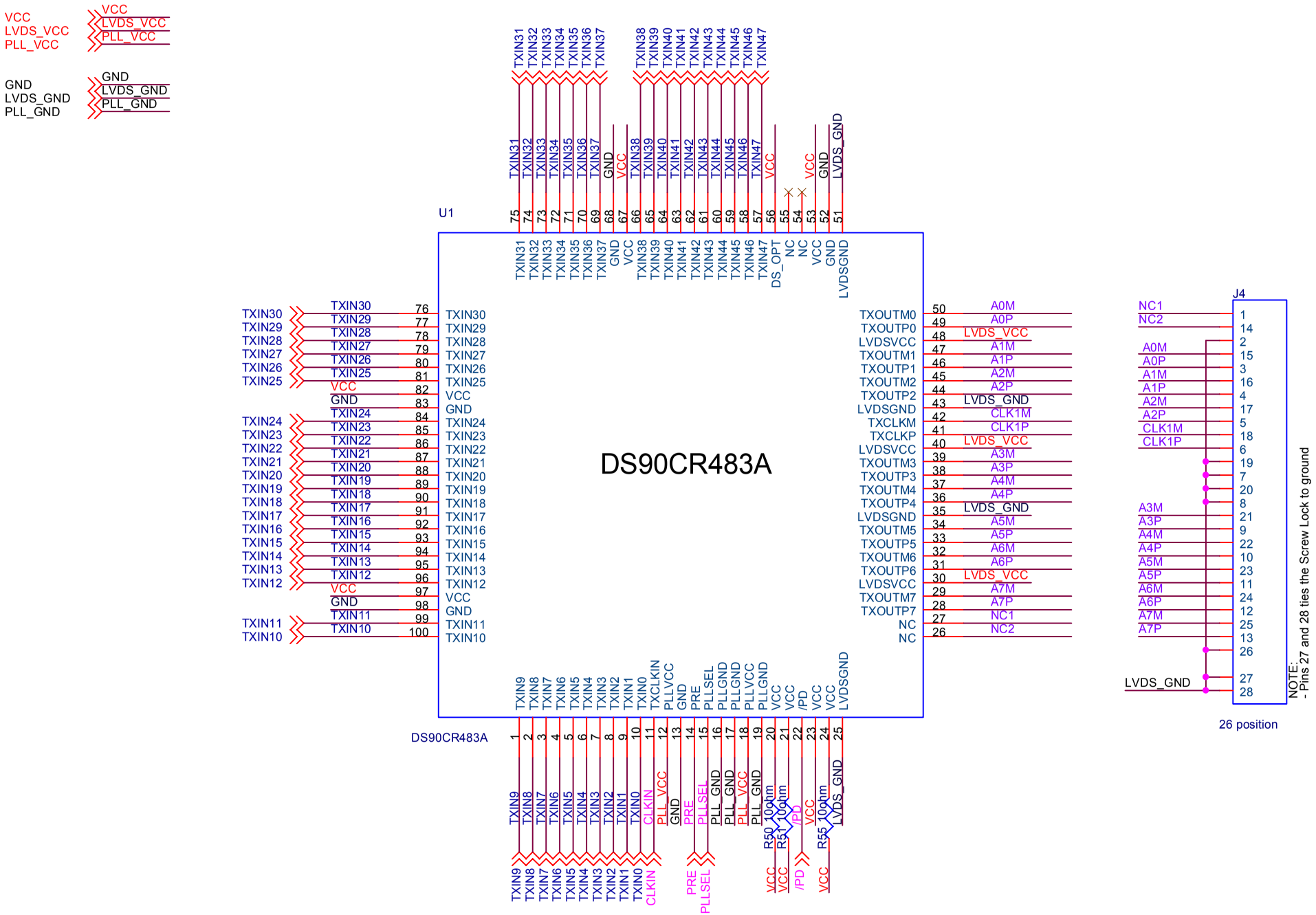
D26-1 wiring diagram for cable assembly and board layout

MDR 26 position right angle surface mount receptacle 10226-1210 VE

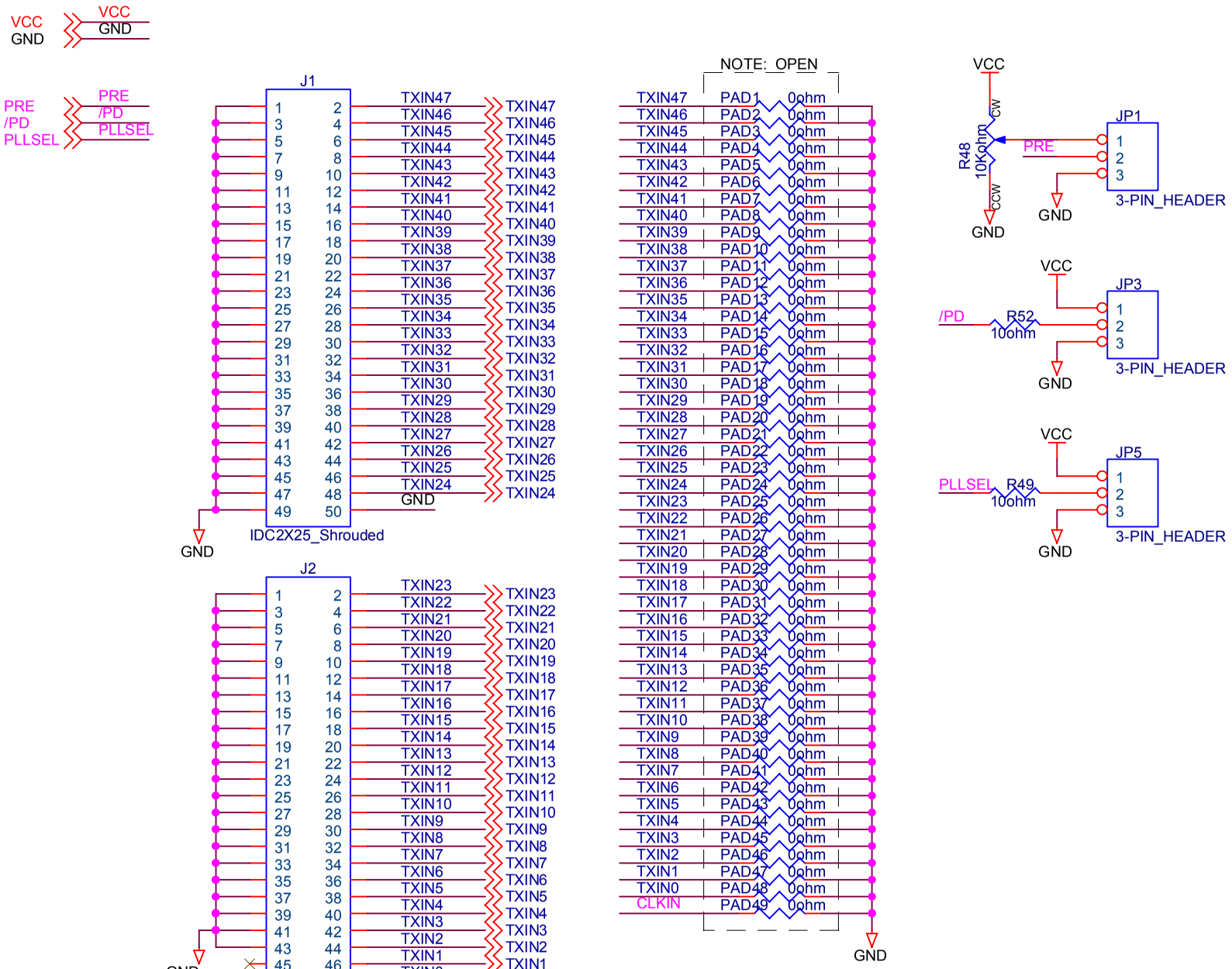
Note: "pad" column represents actual position of solder pad on board layout.
"pin #" column specifies corresponding receptacle contact #.

**** Note: Temporary pinout for Channel Link testing purposes only.****

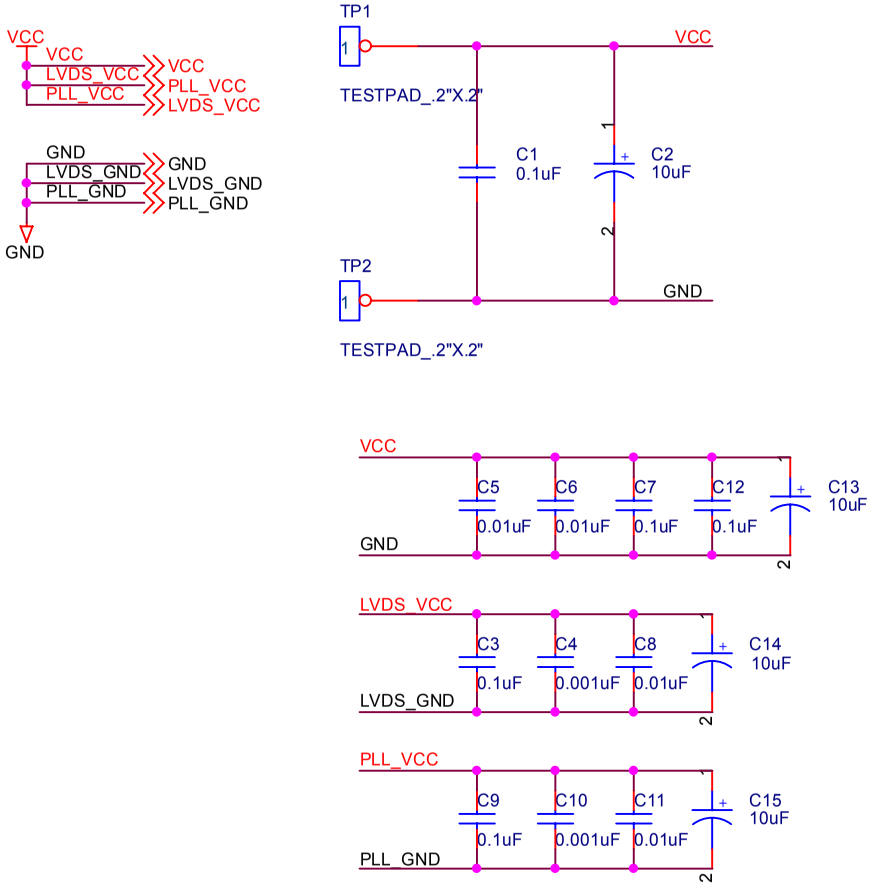
Tx-483A pin #	Transmitter receptacle pad	pin #	signal type	Cable Assembly	signal type	pin #	Receiver receptacle pad	Rx-484A pin #
		1	Extra 1		LVDS gnd	26		
		14	Extra 2		A7P	13		79
		2	Extra 3		A7M	25		80
50		15	A0M		A6P	12		82
49		3	A0P		A6M	24		83
47		16	A1M		A5P	11		84
46		4	A1P		A5M	23		85
45		17	A2M		A4P	10		86
44		5	A2P		A4M	22		87
42		18	CLK1M		A3P	9		89
41		6	CLK1P		A3M	21		90
		19	Control 1		Control 4	8		
		7	Control 2		Control 3	20		
		20	Control 3		Control 2	7		
		8	Control 4		Control 1	19		
39		21	A3M		CLK1P	6		91
38		9	A3P		CLK1M	18		92
37		22	A4M		A2P	5		94
36		10	A4P		A2M	17		95
34		23	A5M		A1P	4		96
33		11	A5P		A1M	16		97
32		24	A6M		A0P	3		98
31		12	A6P		A0M	15		99
29		25	A7M		Extra 3	2		
28		13	A7P		Extra 2	14		
		26	LVDS gnd		Extra 1	1		



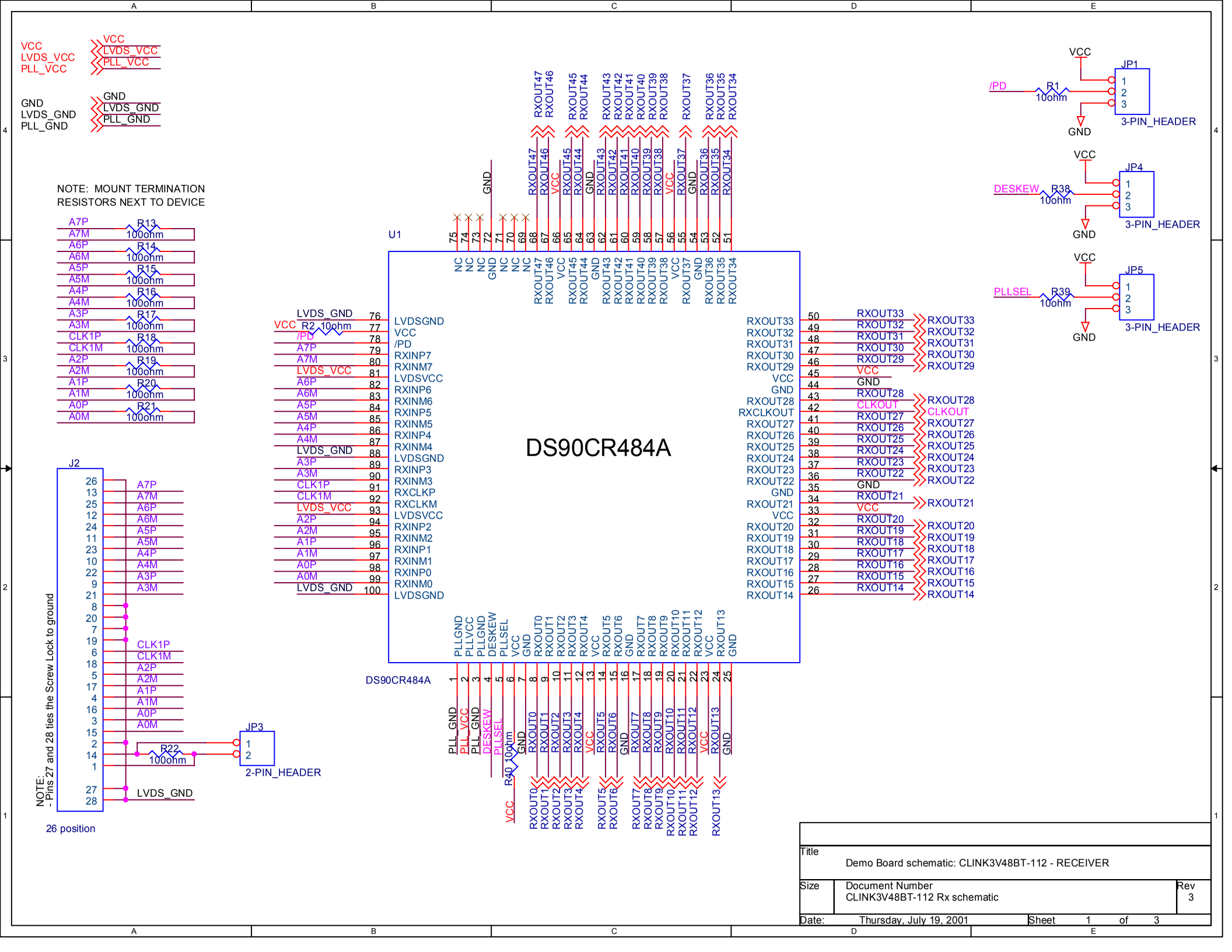
Title	Demo Board schematic: CLINK3V48BT-112 - TRANSMITTER	
Size	Document Number CLINK3V48BT-112 Tx schematic	Rev 3
Date: Thursday, July 19, 2001	Sheet 1 of 3	

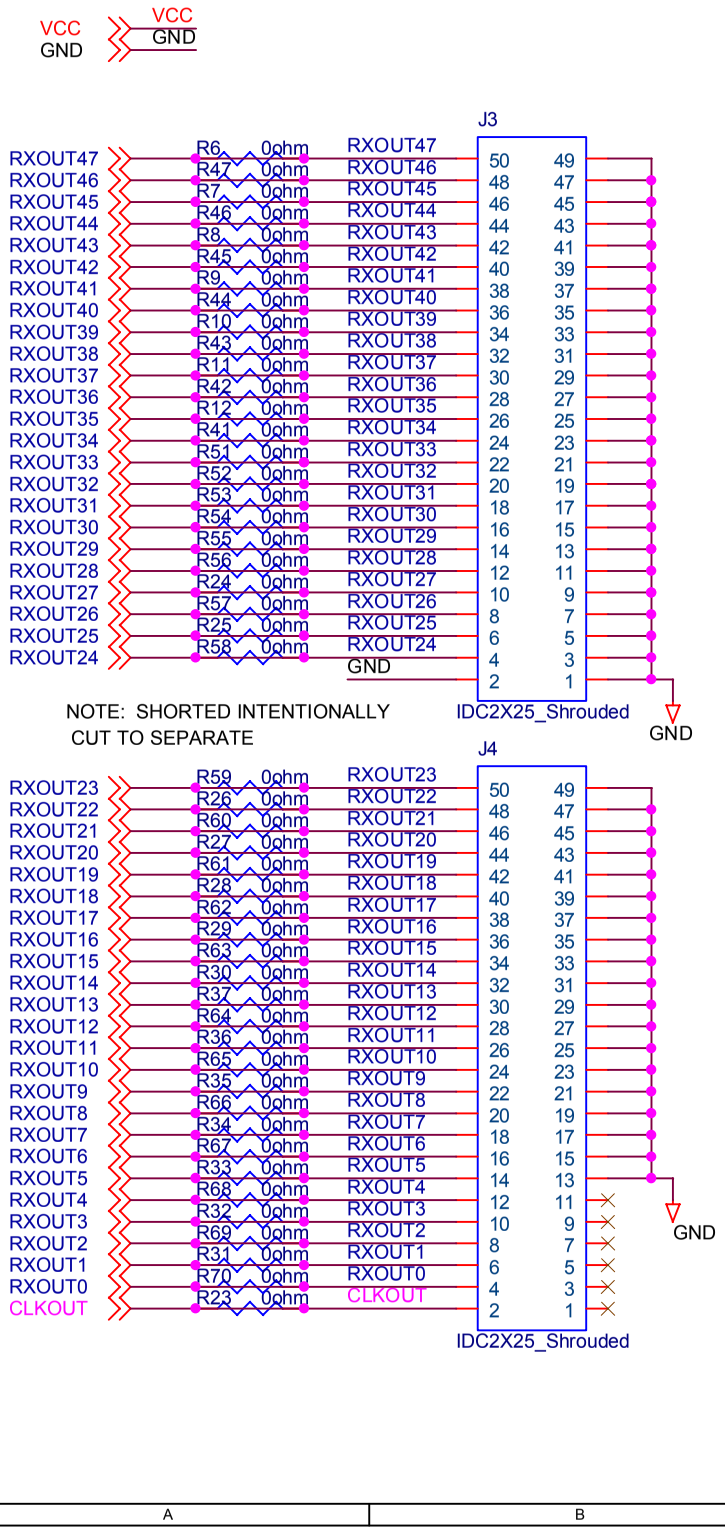


Title	Demo Board schematic: CLINK3V48BT-112 - INPUTS	
Size A	Document Number CLINK3V48BT-112 Tx schematic	Rev 3
Date: Thursday, July 19, 2001	Sheet 2 of 3	

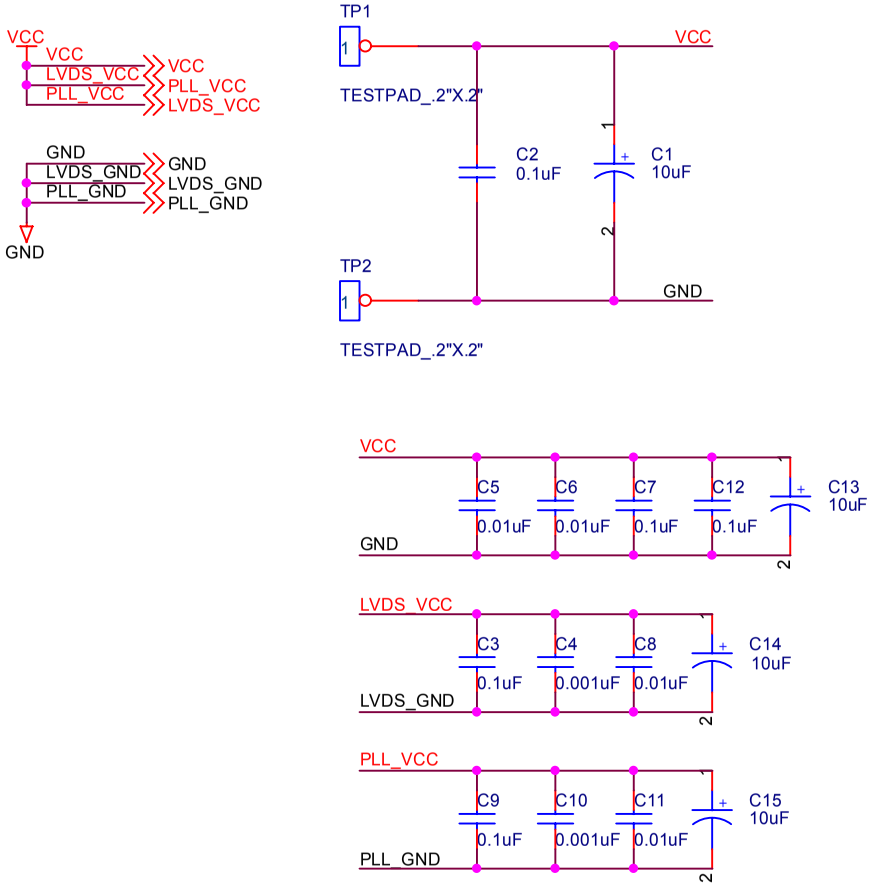


Title	Demo Board schematic: CLINK3V48BT-112 - POWER	
Size	Document Number CLINK3V48BT-112 Tx schematic	Rev 3
Date: Thursday, July 19, 2001	Sheet 3 of 3	


VCC
LVDS_VCC
PLL_VCC
GND
LVDS_GND
PLL_GND
NOTE: MOUNT TERMINATION RESISTORS NEXT TO DEVICE
R13 100ohm
R14 100ohm
R15 100ohm
R16 100ohm
R17 100ohm
R18 100ohm
R19 100ohm
R20 100ohm
R21 100ohm
U1
DS90CR484A
R2 10ohm
/PD
J2
26 position
NOTE:
- Pins 27 and 28 ties the Screw Lock to ground
R22 100ohm
JP3
2-PIN_HEADER
R40 10ohm
JP1
R1 10ohm
3-PIN_HEADER
JP4
DESKEW
R38 10ohm
JP5
PLLSEL
R39 10ohm
Title
Demo Board schematic: CLINK3V48BT-112 - RECEIVER
Size
Document Number
CLINK3V48BT-112 Rx schematic
Rev
3
Date:
Thursday, July 19, 2001
Sheet 1 of 3



Title	Demo Board schematic: CLINK3V48BT-112 - OUTPUTS	
Size A	Document Number CLINK3V48BT-112 Rx schematic	Rev 3A
Date: Tuesday, July 15, 2008	Sheet 2 of 3	



Title	Demo Board schematic: CLINK3V48BT-112 - POWER	
Size	Document Number CLINK3V48BT-112 Rx schematic	Rev 3A
Date: Tuesday, July 15, 2008	Sheet 3 of 3	

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