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1 DS90UH928QEVM Introduction

The Texas Instruments DS90UH928QEVM evaluation module (EVM) helps system designers evaluate the operation and performance of the DS90UH928Q 5MHz-85MHz FPD-Link III Deserializer (DES). The device translates a high-speed serialized FPD-Link III interface transported over a single shielded twisted pair (STP) into four FPD-Link compatible LVDS data output pairs and one LVDS clock.

The DS90UH928QEVM board features a 20-position IDC connector for connecting to the FPD-Link outputs, and a HSD Automotive Connector for connecting an automotive-grade STP cable to the FPD-Link III input. The included SMA connectors can also be configured as the FPD-Link III data input, enabling evaluation of other connectors and cable configurations.

The EVM contains one deserializer device.

Table 1-1. Device and Package Configurations

Reference	IC	Package
U1	DS90UH928QSQ	WQFN48

1.1 DS90UH928QEVM Kit Contents

The DS90UH928QEVM Kit contains the following items:

- DS90UH928QEVM Evaluation Board
- USB Cable

1.2 System Requirements

The ALP software installation requires a PC with a USB interface, running the Windows XP or greater operating system.

1.3 DS90UH928QEVM Overview

The DS90UH928Q deserializer supports rich audiovisual applications in automotive navigation and rear seat entertainment systems. The DS90UH928Q receives video data, I2S audio, GPIO, and I2C control over a single shielded twisted pair cable. The evaluation board and included software enables easy evaluation of the deserializer features, including:

- Support of 720p video applications with a pixel clock frequency up to 85MHz
- Surround sound I2S Digital Audio Applications with up to 4 I2S data outputs
- Low EMI FPD-Link video output interface
- Bidirectional control channel including GPIO (with 2 dedicated pins), interrupt, and I2C interface
- Up to 10 configurable I2C addresses
- Flexible 3.3V or 1.8V LVCMOS I/O interface
- Adaptive cable equalization
- @SPEED Link BIST Mode and LOCK status indicator LED
- Image Enhancement (White Balancing & Hi-FRC Dithering)
- Backwards compatibility mode allowing pairing with DS90UR905Q and DS90UR907Q serializers
- Internal Pattern Generation
- Loop-through monitor outputs for observing link integrity

1.4 Typical Application

The following diagram illustrates a typical rear seat entertainment application that utilizes the DS90UH928Q deserializer and a compatible serializer (DS90UH925Q or DS90UH927Q). The DS90UH928Q accepts FPD-Link III data transported over an automotive-grade STP cable and deserializes the data stream into video, audio, and control information intended for a display and other local peripherals.

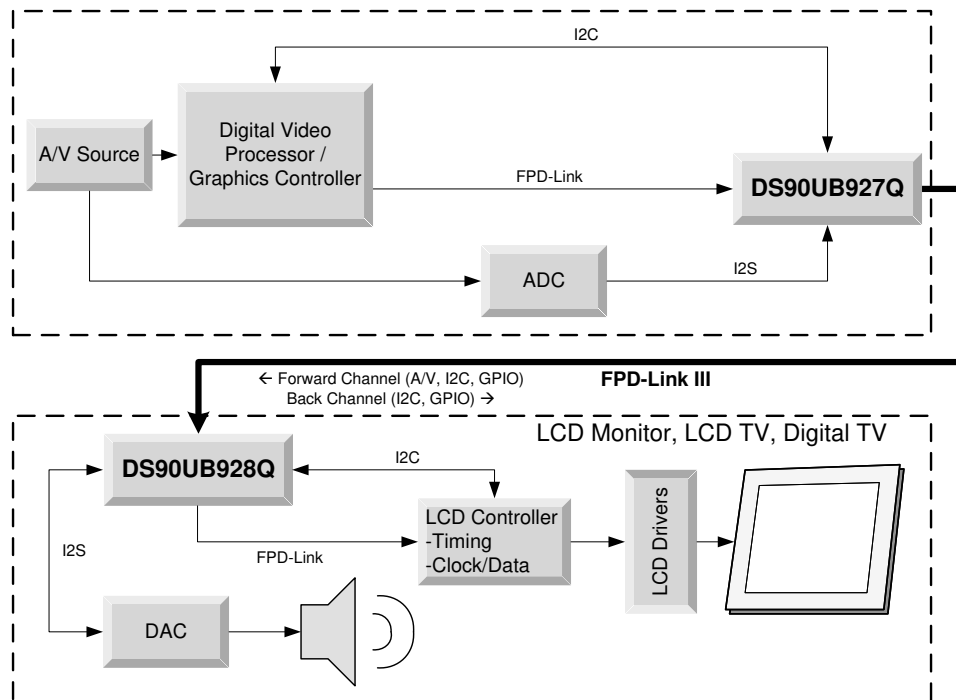


Figure 1-1. Typical Application/Evaluation Configuration

2 Quick Start Guide

2.1 Board Setup

This section describes how to quickly set up the DS90UH928QEVM with an appropriate serializer for evaluation of the chipset in display applications. The default switches and jumper positions have been set at the factory. This setup guide assumes the user has already installed and configured the included ALP software. See [Installation](#) for details.

1. Connect an appropriate 12 VDC power supply to barrel jack J12. If 1.8V VDDIO operation is desired, set the 1.8V position at JP10.
2. Connect an applicable cable (not provided, HSD automotive connector configured by default) from the DS90UH928QEVM (RX) board FPD-Link III input (J4) to the FPD-Link III output of a compatible FPD-Link III (TX) board (DS90UB925-Q1EVM or DS90UH927QEVM).
3. From the Video source, connect a flat cable to the TX board (J5) and connect the appropriate cable from the RX board to the panel.
4. Connect the included USB cable from a host computer running the included TI ALP software to the USB port (J17) on the RX board. See [Usage](#) for further information on using the TI ALP tool.
5. (Optional) Connect audio from an I2S audio source to TX board (JP2) pins DA (data), CLK (clock), and WC (word clock) and from RX board pins DA, CLK, and WC to an I2S DAC.
6. (Optional) Connect and configure any required GPIO interfaces. GPIO0 and GPIO1 are dedicated pins.

Jumpers and switches have been configured by TI and do not require any changes for immediate operation of the board. See [Evaluation Hardware Overview](#) and the DS90UH928Q device data sheet for further details.

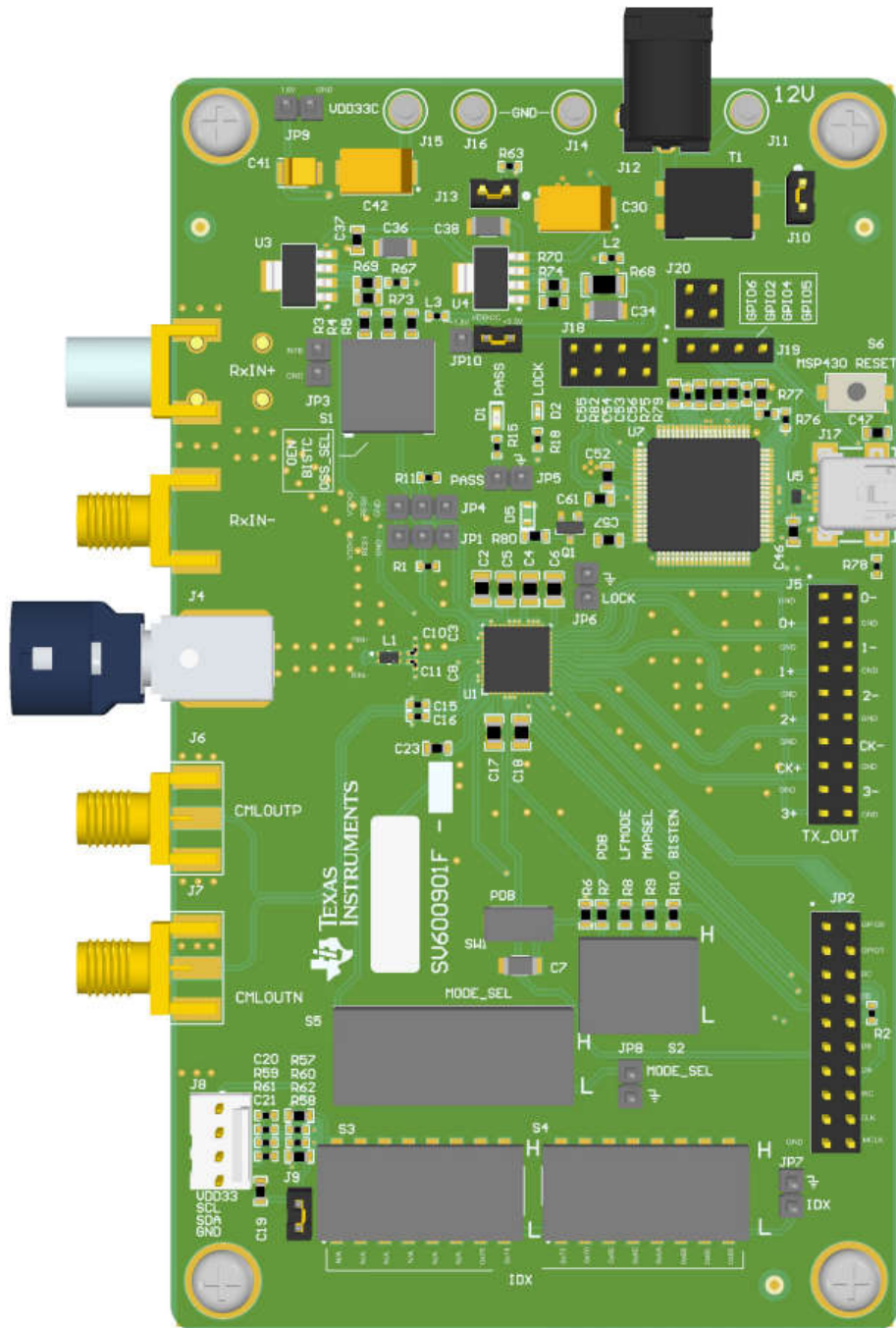


Figure 2-1. DS90UB928-Q1EVM

3 Evaluation Hardware Overview

3.1 Board Overview

The evaluation board includes circuits and interfaces facilitating the different device features of the DS90UH928Q deserializer, including power, video data, FPD-Link III interface, I2S audio, I2C control, connectors, and configuration switches.

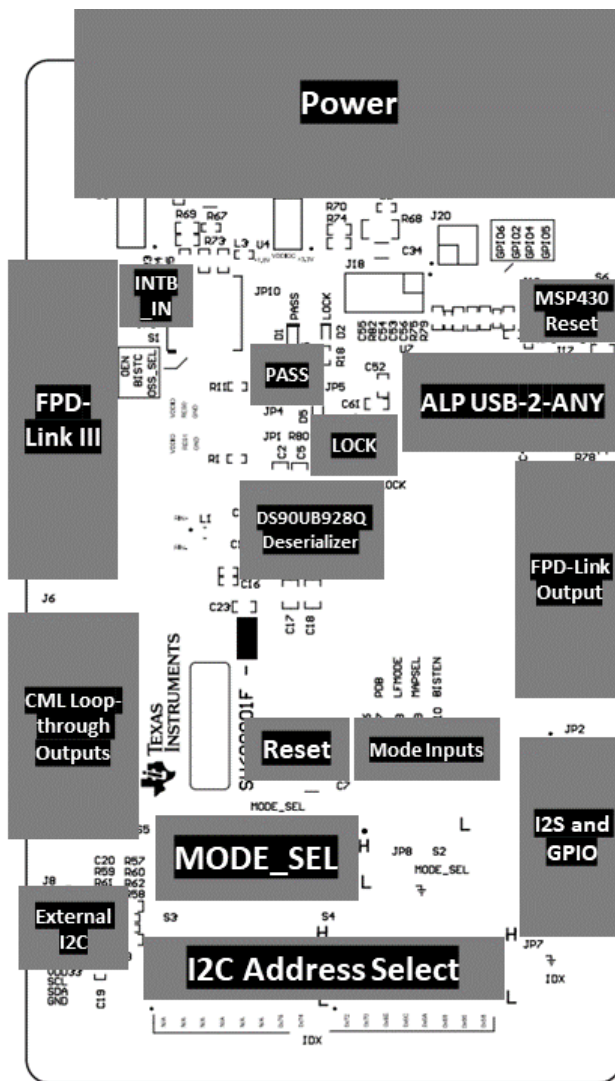


Figure 3-1. DS90UH928-Q1EVM Layout

3.2 Power

There is one option to power the board. +12V DC power can be supplied at the provided barrel connector (J12). If 1.8V VDDIO power supply operation is desired, then select 1.8V VDDIO power from JP10.

3.3 FPD-Link Video Data Output

The FPD-Link video data output accepts a 20-pin IDC cable or similar 0.1 inch spaced connector. Connect the clock and 4 FPD-Link (LVDS) data pairs here. Video data mapping is determined from the MAPSEL switch, located on the mode select switch block (S2).

The required standard 100Ω differential termination is not populated onboard by default, but can be populated at R13, R14, R16, R17, and R19, located under the output connector (J5). Many sink devices (such as displays) have termination closer to the connector, or integrated into the module or board. Check the specific target device or module to verify that proper LVDS termination is used.

3.4 FPD-Link III Interface

The FPD-Link III interface is the receive point for the high-speed (up to 2.975Gbps) forward data channel, as well as the transmit point for the low speed back channel. The default configuration features a Rosenberger HSD-style automotive cable connector (J4). The board also provides two SMA connectors (J1/J2 and J3) to which other cable connectors can be attached. To use the SMA connectors, swap out C10 and C11, and populate them at C3 and C8. See [Section 6](#) for details.

The FPD-Link III signal can be probed from the CML loop-thru interface (J6 and J7) for easier observation of the forward-channel link. See the device data sheet for additional details.

3.5 CML Loop-thru Monitor Interface

The evaluation board provides two SMA connectors (J6 and J7) for monitoring the CML Loop-thru driver (CMLOUTP/CMLOUTN pins). If this feature is enabled (see device data sheet for details), then the recovered and equalized link eye diagram can be monitored from these outputs, allowing easier observation of link signal integrity.

3.6 Controller

The onboard USB-to-I2C controller allows for easy evaluation of the DS90UH928Q I2C interface without the need for a dedicated external tool. The DS90UH928Q interfaces with a host PC using the provided TI Analog LaunchPAD (ALP) software. Connect the provided cable to the USB connector at J17. The I2C bus can also be accessed by an external controller via the external I2C interface at J8. If desired, then the onboard USB-to-I2C connector can be disconnected from the I2C bus by removing resistors R60 and R62 (see the board schematic for details). See [Section 6](#) for details.

3.7 I2C and Device Addressing

A row of switches provided by S3 and S4 sets the IDx I2C address select. Only one I2C address can be selected at a time. Note that addresses 0x58 and 0x66 through 0x76 are available. All others are reserved.

Table 3-1. I²C Unique Address Settings for IDx

NO.	ADDRESS 7'b	ADDRESS 8'b
1	0x2C	0x58
2	0x33	0x66
3	0x34	0x68
4	0x35	0x6A
5	0x36	0x6C
6	0x37	0x6E
7	0x38	0x70
8	0x39	0x72
9	0x3A	0x74
10	0x3B	0x76

3.8 I2S and GPIO Interface

JP3 provides connections to the I2S and GPIO interfaces (JP2). All GPIOs can be configured as inputs or outputs, with GPIO[3:0] (GPIO2 is shared with DC, GPIO3 shared with DD) available for bidirectional transport. IO voltage levels scale with VDDIO.

3.9 Device Address, Reset and Mode Selection Inputs

The Mode Selection Inputs determine the specific mode or state of device operation.

3.9.1 Output State Select (S1)

The output state select switches (S1) set the operating conditions for both normal operation and BIST. See the device data sheet for detailed usage of these pins.

- **OEN**
- **BISTC/INTB_IN**
- **OSS_SEL**

3.9.2 Mode Selection Inputs (S2)

The Mode Input Switches (S2) configure the following DS90UH928Q device pins:

- **PDB** When set LOW, the device enters a low-power mode and all registers are reset. Set HIGH for normal operation.
- **LFMODE** Set HIGH for $5\text{MHz} \leq \text{PCLK} < 15\text{MHz}$. Set LOW for $15\text{MHz} \leq \text{PCLK} \leq 85\text{MHz}$
- **MAPSEL** Set LOW to assign LSBs to TxOUT3±, set HIGH to assign MSBs to TxOUT3±. See device data sheet for details.
- **BISTEN** Set HIGH to enable the Built-In Self-test (BIST) Mode. Set LOW for normal operation.

3.9.3 I2C Address Select (IDx)

10 address switches (S3 and S4) set the deserializer I2C address select voltage input to the IDx pin. Each switch selects a different I2C address, up to 10 unique addresses total. Only one switch can be selected at a time (0x58 default). Note that address 0x58 and 0x66 through 0x76 are available for normal device operation. All others are reserved.

3.9.4 MODE_SEL (S5)

The MODE_SEL switches (S5) configure the analog input value to the device mode selection (MODE_SEL) pin. The provided switches and resistor pads allow for configuration of the MODE_SEL voltage. To use other modes or resistor combinations, replace resistors R111 and R116 and use switch position 1 (see board schematic for details).

- **1** - Sets Mode 1 (LONG_CABLE=L, REPEAT=L, BKWD=L, I2S_B=L).
- **2** - Sets Mode 7 (LONG_CABLE=H, REPEAT=H, BKWD=L, I2S_B=L).
- **3** - Sets Mode 9 (LONG_CABLE=L, REPEAT=L, BKWD=H, I2S_B=L).

3.10 Indicators

The board includes three LEDs to indicate deserializer and board status.

- **D5** Indicates that the onboard USB-to-I2C ALP hardware is powered on.
- **D1/PASS** Indicates PASS status, including link error results during and after BIST. See the device data sheet for additional details on BIST mode operation.
- **D2/LOCK** Indicates LOCK status. The LED remains on if the link is active and the device is locked to the remote serializer.

3.11 Input/Output Connectors

The following jumpers and connectors are provided on the board:

- **J1/J2 and J3 FPD-Link III SMA Inputs (optional)** – These optional inputs can be used to evaluate the FPD-Link III serial link with different cable configurations. To use, remove J4 and populate R3 and R4 with 0Ω resistors.
- **J4 FPD-Link III HSD Automotive Input** – Connect an automotive-grade STP cable with HSD connector here. Remove the connector (J4) if the SMA outputs (J1/J2) are used (see description above).
- **J5 20-pin FPD-Link (I) Output** – Connect to LVDS data and clock here. The board does not provide the required 100Ω terminations as these are normally located closer to, or integrated into, the sink device (display). If desired, then termination resistors can be populated at R5, R6, R7, R8, and R10. See the device data sheet for output electrical characteristics and requirements.
- **J8 4-pin I2C Input/Output** – Connect SDA, SCL, VSS, and VDD33 to external I2C peripherals or controllers here. The EVM board provides the recommended 4.7kΩ pull-up resistors.
- **J17 USB Connector for USB-to-I2C Controller** – Connect USB cable to host PC to use the ALP evaluation software with the EVM board.
- **J12 12V External Power Input** – Connect a +12V, 2.1mm barrel connector here to supply power to the board. Onboard regulators supply the devices with 3.3V VDDIO and 3.3V/1.8V VDDIO supplies.
- **JP2 I2S/GPIO Input/output Header** – Connect to I2S input pins or bidirectional GPIO pins. See the device data sheet for detailed I2S and GPIO usage.
- **JP10 VDDIO Select** – Connect jumper to select VDDIO=VDD33 [2-3] or VDDIO=VDD18 [1-2]



Figure 3-2. VDDIO Select (JP7) Jumper Settings

- **JP5 PASS Monitor** – Probe PASS status here.
- **JP6 LOCK Monitor** – Probe LOCK status here.
- **JP9 AUX Power** – Alternative power connection header. See board schematics for details.
- **JP3 INTB_IN** – General-purpose interrupt. See device data sheet for control register and usage descriptions.
- **JP9 I2C Power Enable** – Place jumper (default) to provide 3.3V power to on-board I2C pull-up resistors.
- **SW1 PDB Reset** – Press to set PDB LOW (device resets and all registers are cleared to default values).
- **S6 ALP Reset** – Resets onboard USB-to-I2C (MSP430) hardware.

4 ALP Software

4.1 Overview

The Analog Launch PAD (ALP) software allows evaluation of the I2C control interface of the DS90UH928Q deserializer. The tool provides a graphical interface for reading and writing the device registers. The tool also features several useful tools for manipulating advanced device-specific features, including internal pattern generation and image enhancement features.

System Requirements:

Operating system: Windows XP, Vista, or greater

USB version: 2.0

4.2 Installation

Download the TI Analog Launch PAD (ALP) software from the TI website, ti.com/tool/ALP. Please also download the separate ALP updater too, the [ALP-PROFILE-UPDATE](#). Make sure the EVM USB port is not connected to the host PC during this time.

Users need to log into a ti.com profile to access the download page, then fill out the questionnaire for export approval before receiving the executable installer.

The following installation instructions are for the Windows Operating System:

Install the ALP Software

Extract the *ALPF_setup_v_x_xx_xxxx.exe* from snlc048, then run the executable.

1. Click *Next*.
2. Select *I accept the agreement*.
3. Click *Next*.
4. Select the location to install the ALP software and click *Next*.
5. Select the location for the Start Menu shortcut and click *Next*.
6. Create a desktop shortcut icon and Quick Launch button (optional). Click *Next*.
7. Click *Install*. The software is extracted and installed to the system.
8. Uncheck *Launch Analog LaunchPAD* and click *Finish*. The ALP software must not be launched until the USB driver is installed.

USB2ANY Driver

The DS90UB928QEVM is recognized from the host as a generic human interface device (HID), so there is no proprietary driver to install onto the PC. Typically after connecting the device to the host PC, users see a pop-up window indicating *Found New Hardware, USB Input Device*. If users do not see this prompt, then refer to the below information.

If the USB2ANY firmware is not installed onto the MSP430 on-board, then the USB2ANY firmware does not register in ALP as detecting the hardware (see troubleshooting for more information). In this case, the firmware must be loaded onto the MSP430 to communicate with the device. Users can find and install the program needed for this under [MSP430USBDEVPACK/5.20.07.01](#), *Python based Firmware Upgrade Example*.

To install the ALP hardware USB driver, connect the USB cable from the host PC to the DS90UH928QEVM USB port (J6):

1. Launch the *Python_Firmware_UpgraderGUI* software.
2. If *ready* is shown in the console box, proceed to step 3. If not, then hold the BSL reset button (S6), remove and re-insert the USB mini into the port. Then select File > Rescan HID Bus...
3. Select File > Open User Firmware...
4. Locate the *USB2ANY_2_7_0_0.txt* file for import, depending on your location of the ALP software. The rest of the path is shown here: Analog LaunchPAD v1.57.0010\Drivers\i2c_controllers\usb2any\Firmware\.
5. After running the program, the console shows *OK* at the end, and the driver is recognized by the PC.
6. Open ALP to confirm whether the USB2ANY populates on the main screen under *Devices*.

The software installation is now complete. The ALP software can now be used with DS90UB928-Q1EVM.

4.3 Usage

Startup

Make sure all the software has been installed and the hardware is powered on and connected to the PC. Execute *Analog LaunchPAD* from the start menu. The default start menu location is *Programs\National Semiconductor Corp\Analog LaunchPAD vx.x.x\Analog LaunchPAD*.

The application comes up in the state shown below. If the application does not, then see [Section 4.4](#). Under the *Devices* tab click on DS90UH928Q to select the device and open up the device profile and the associated tabs.

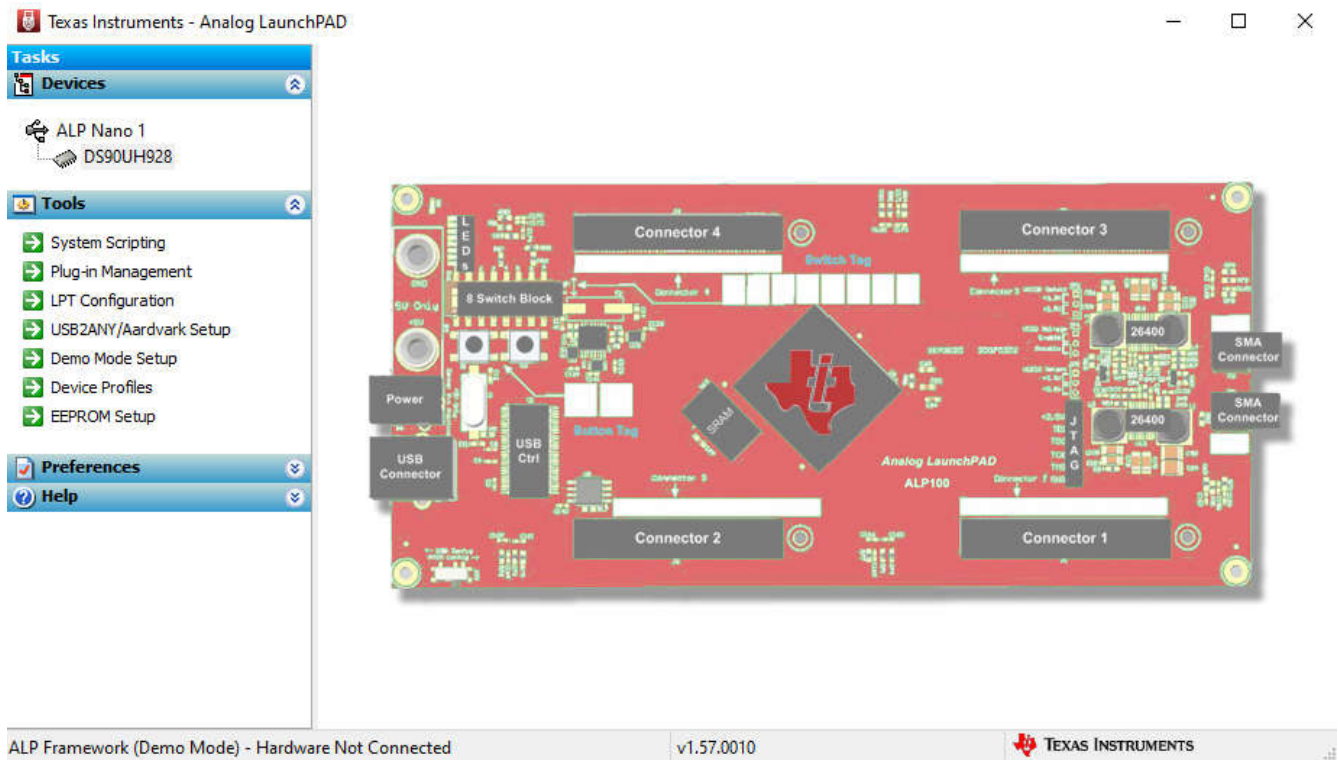


Figure 4-1. ALP Startup Screen

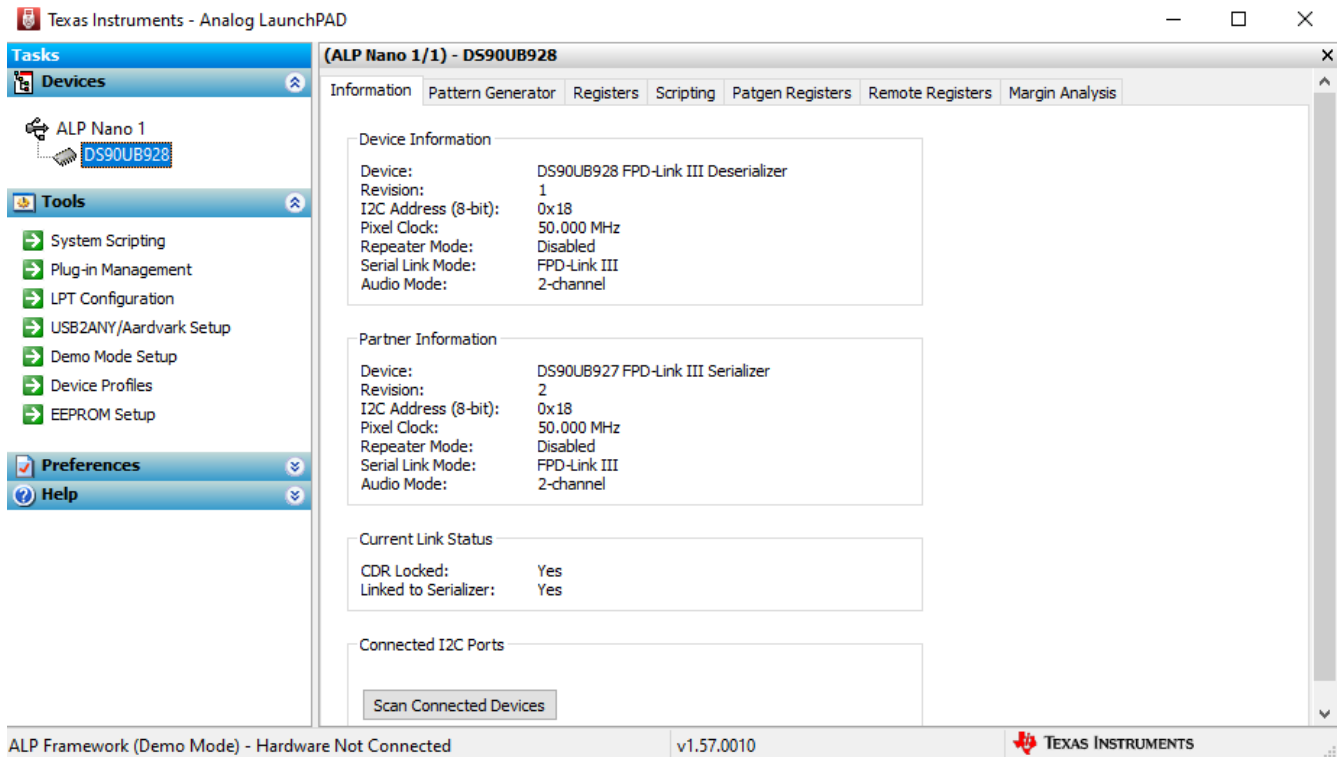


Figure 4-2. Information Tab

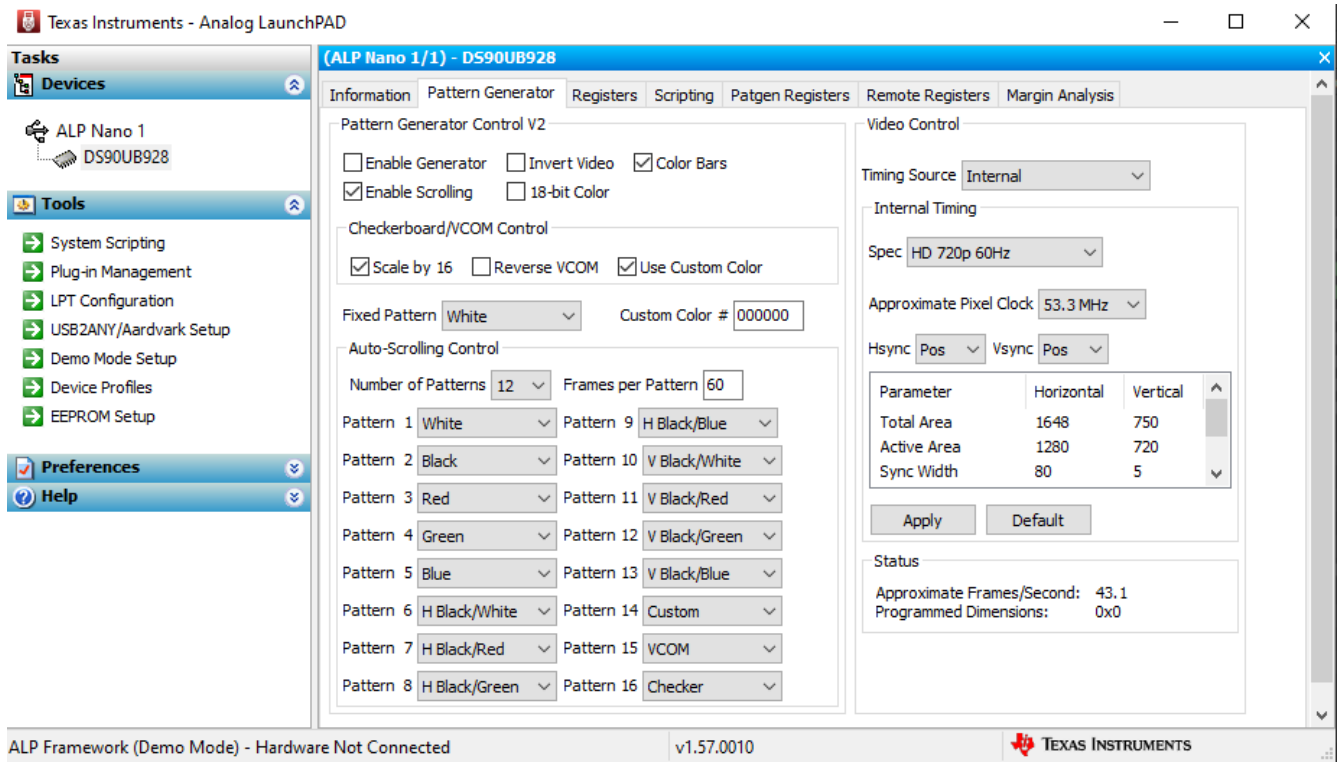


Figure 4-3. Pattern Generator Tab

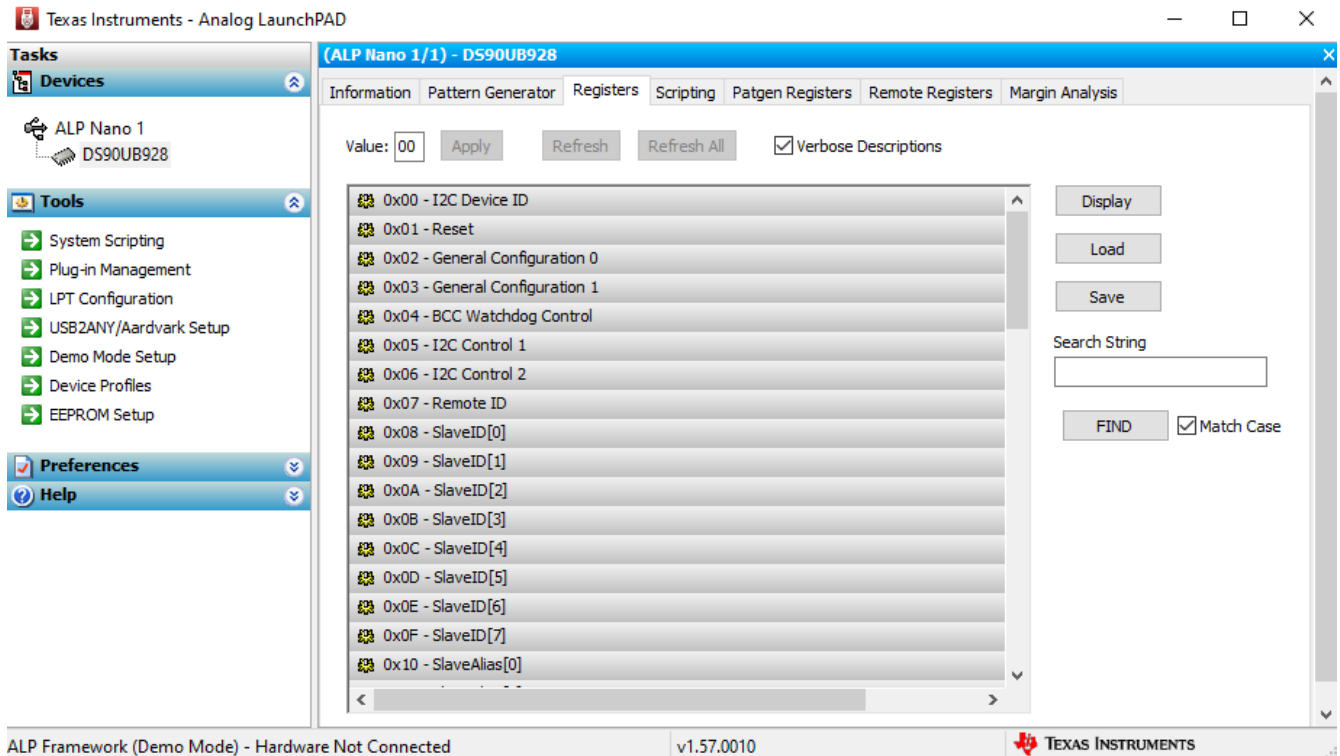


Figure 4-4. Register Tab

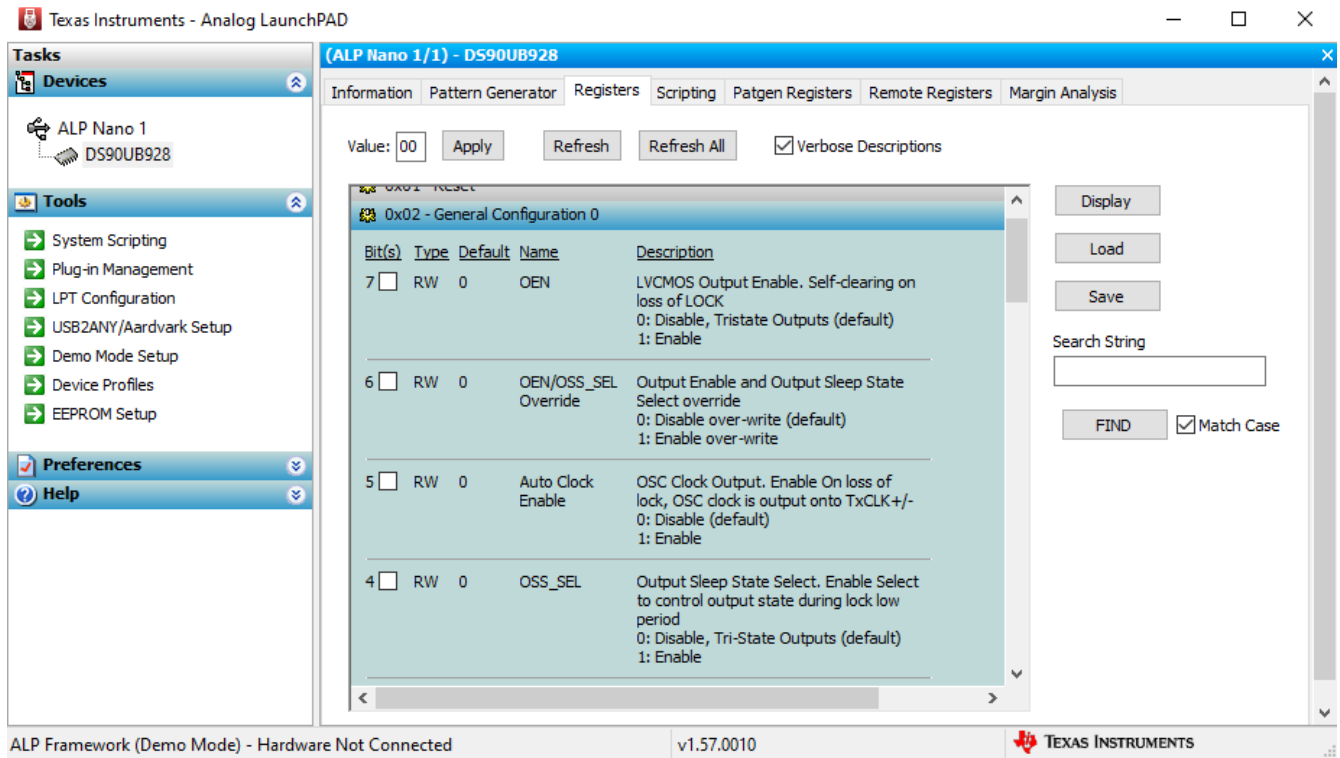


Figure 4-5. Register Tab with expanded register description

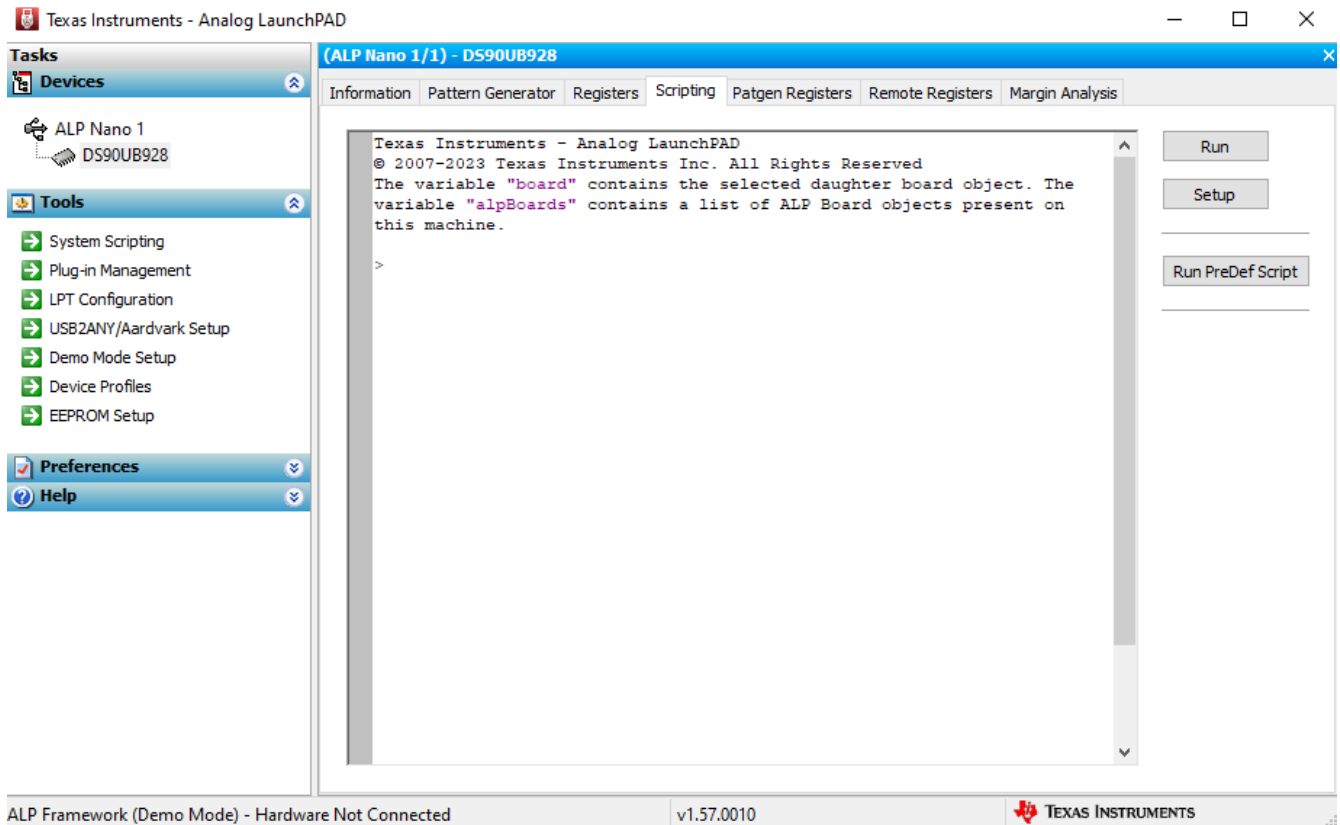


Figure 4-6. Scripting Tab

4.3.1 Information Tab

The information tab gives basic device state information, including local device information, partner device information, and current link status. For both the local device and partner device, the tab gives the following information:

- Device Name
- Device Revision
- I2C address
- Pixel clock range (set by LFMODE)
- Repeater Status (set by MODE_SEL)
- Serial Link Mode (set by MODE_SEL)
- Audio mode (set by configuration registers)

4.3.2 Pattern Generator Tab

The Pattern Generator Tab enables interactive control of the internal pattern generator features. The pane controls timing information and different pattern settings, including a scrolling function. Timing information is configured from the Video Control panel, and supports the following timing/clocking sources:

- External
- Internal
- Internal w/ Ext. Clock

The Internal timing option allows evaluation of the link performance without the need for an external source. The Video Control panel also provides several timing and pixel clock options, including several presets covering common video resolutions. See TI application note AN-2198 for more details.

4.3.3 Registers Tab

The Registers Tab allows for direct reading/writing of individual registers or register bits located on the local device. Each register drop-down shows the name and description of individual bits or groupings of bits. Use the check boxes to set individual bits, and commit the register write by clicking the “Apply” button. Click the “Refresh” or “Refresh All” buttons to read an update of the selected register or all registers respectively.

4.3.4 Scripting Tab

The Scripting Tab allows for basic I2C read/write commands to be sent to the board using ALP's FPD-Link library. Custom scripts can be loaded and run from this panel as well, to configure several registers at once.

4.4 Troubleshooting

If the following window opens after starting the ALP software, double check the hardware setup and that the board USB port is connected to the host PC.

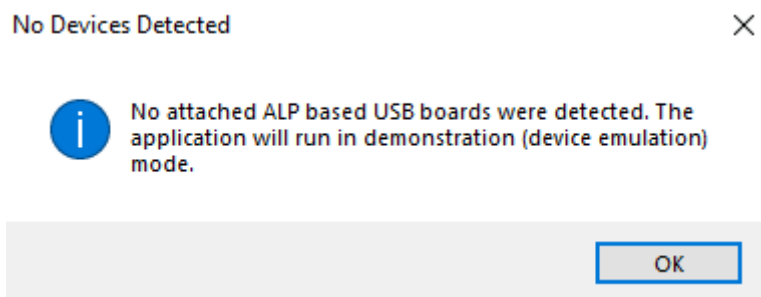


Figure 4-7. No Devices error message

The USB driver is not installed. Check the device manager. There is a device named *NSC ALP Nano Atmel* device under the *Universal Serial Bus Controllers* as shown below.

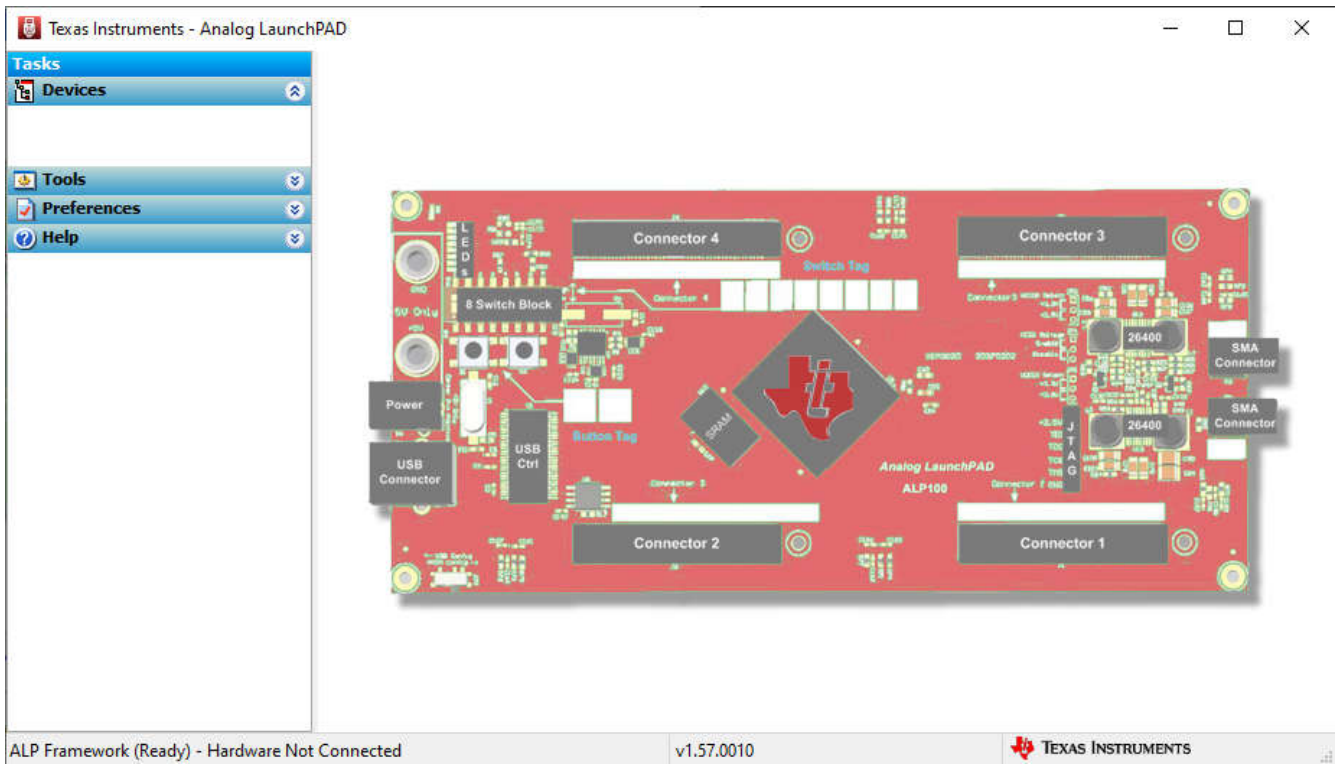


Figure 4-8. Analog LaunchPAD in Demo Mode

Disable the demo mode by selecting the *Preferences* pull down menu and un-checking *Enable Demo Mode*.

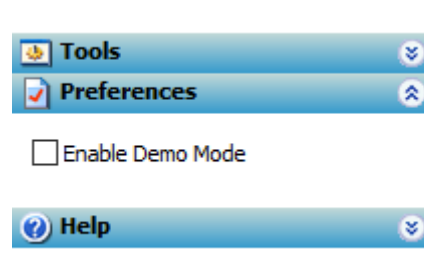


Figure 4-9. Analog LaunchPAD Preferences Menu

After demo mode is disabled, the ALP software polls the ALP hardware. The ALP software updates and displays only DS90UH928Q under the *Devices* drop-down menu.

5 Related Documentation

Additional information can be found in the device product folder at www.ti.com.

- DS90UH928Q data sheet: 5MHz - 85MHz 24-bit Color FPD-Link III to FPD-Link Deserializer with HDCP with Bidirectional Control Channel ([SNLS417](#))
- DS90UH927Q data sheet: 5MHz - 85MHz 24-bit Color FPD-Link III Serializer with Bidirectional Control Channel ([SNLS416](#))
- DS90UH925Q data sheet: 720p 24-bit Color FPD-Link III Serializer with Bidirectional Control Channel ([SNLS407](#))
- TI Application Note: AN-2173 I2C Communication Over FPD-Link III with Bidirectional Control Channel ([SNLA131](#))
- TI Application Note: AN-2198 Exploring the Internal Test Pattern Generator Feature of 720p FPD-Link III Devices ([SNLA132](#))

6 Board Schematic

Consider the discrete component selection for the design carefully. Disregarding the basic design considerations can result in below-optimum performance. The figures below show the schematic overview for the evaluation board.

Board Block Diagram

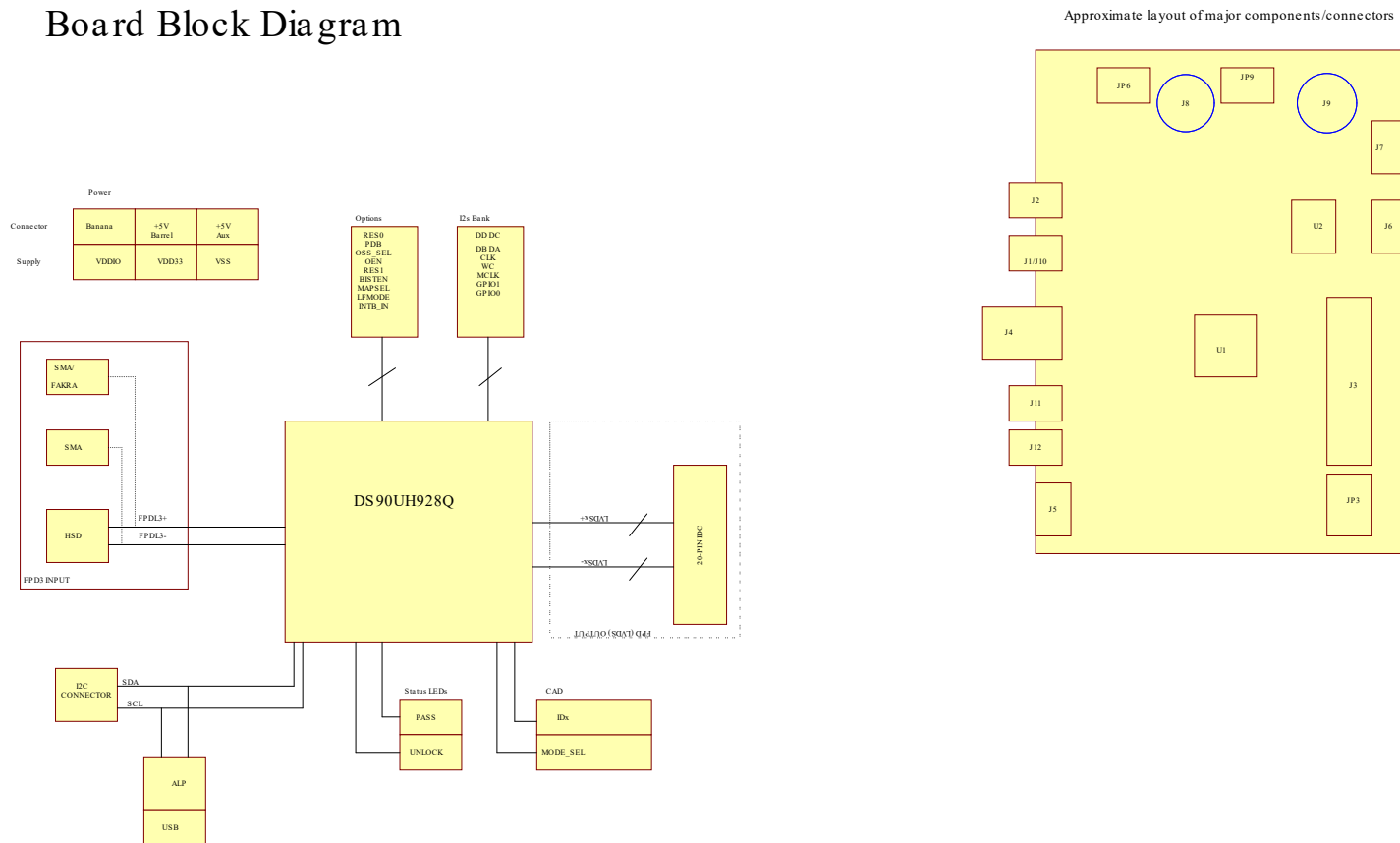


Figure 6-1. System Block Diagram

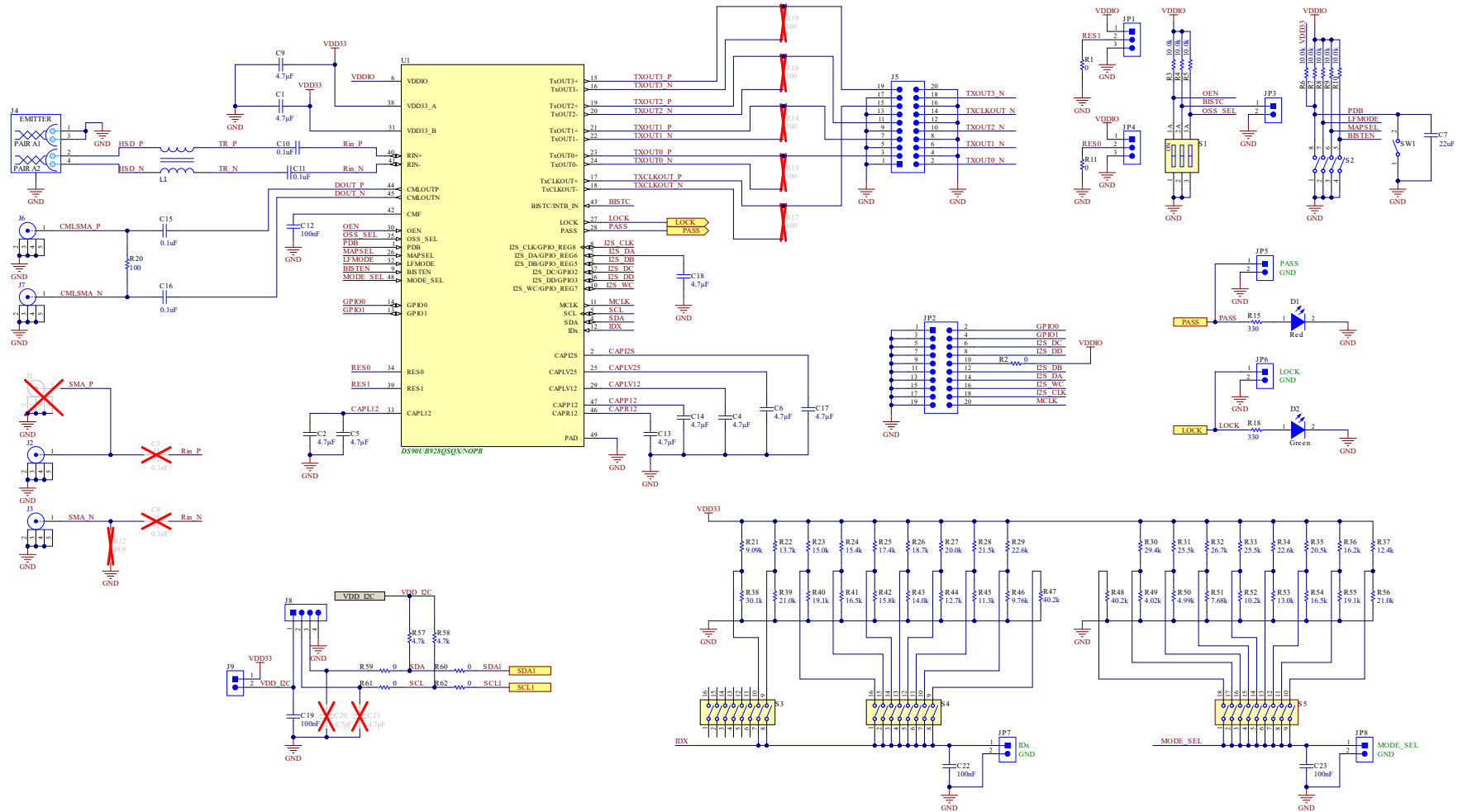


Figure 6-2. DS90UB928-Q1 Device

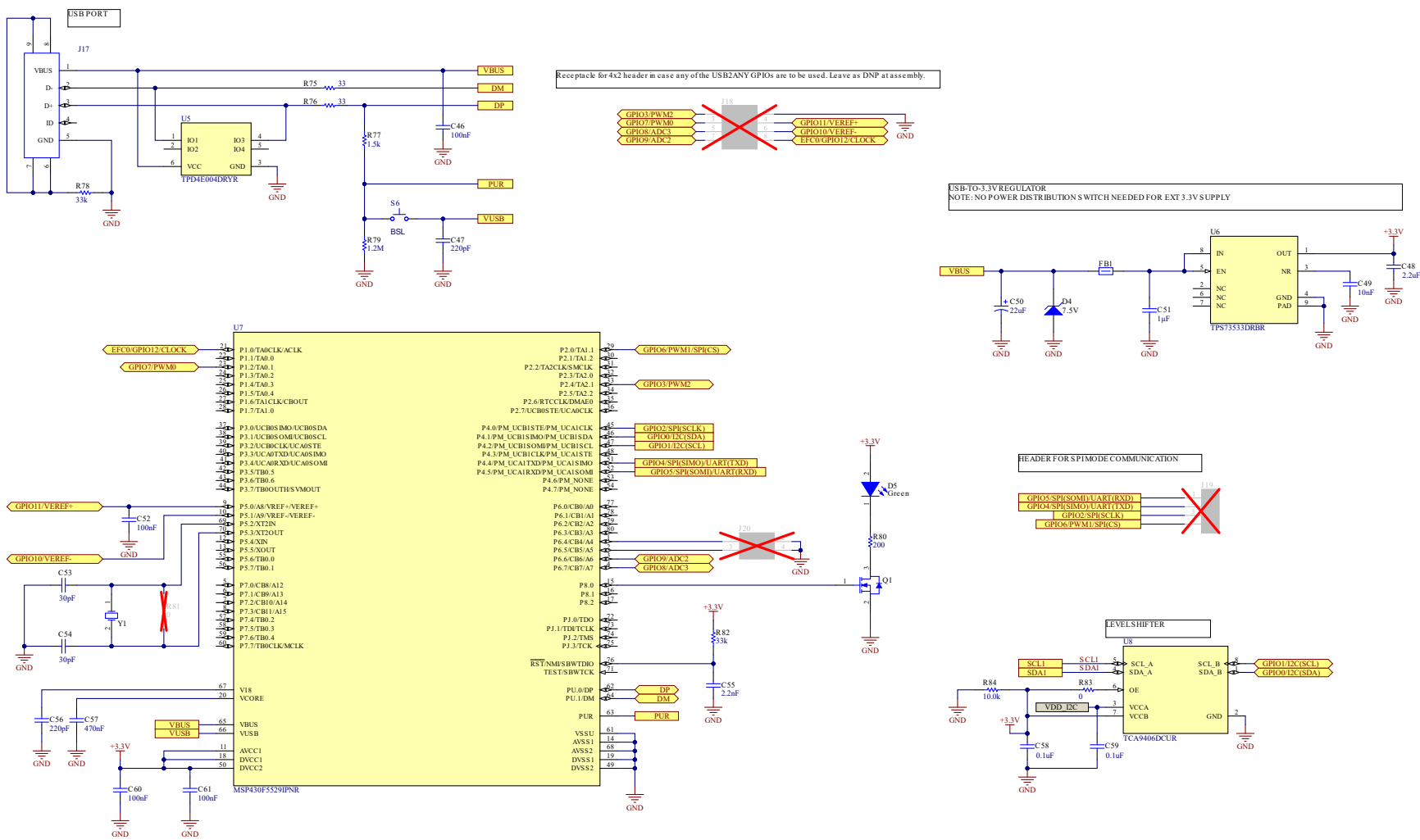


Figure 6-3. USB2ANY

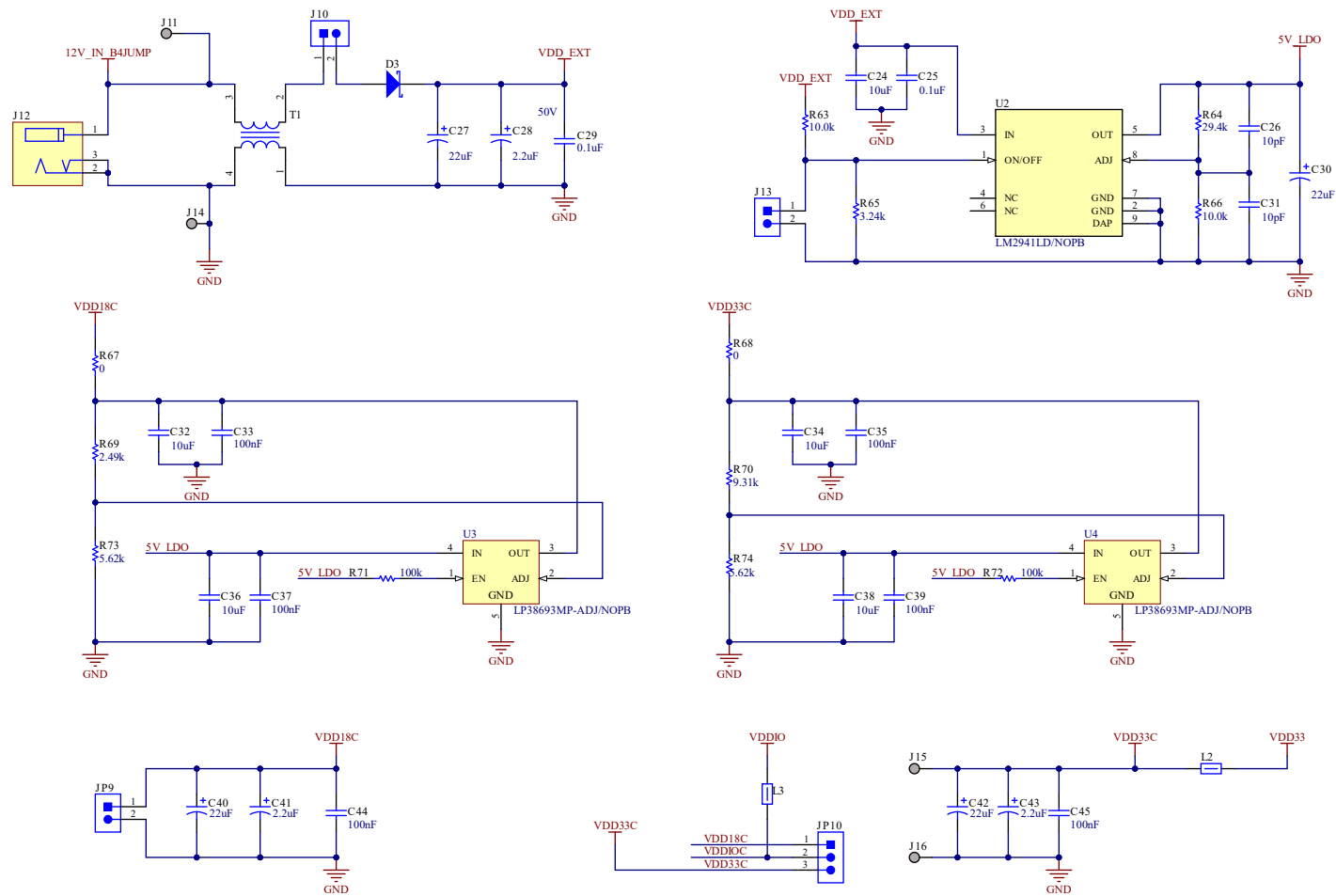
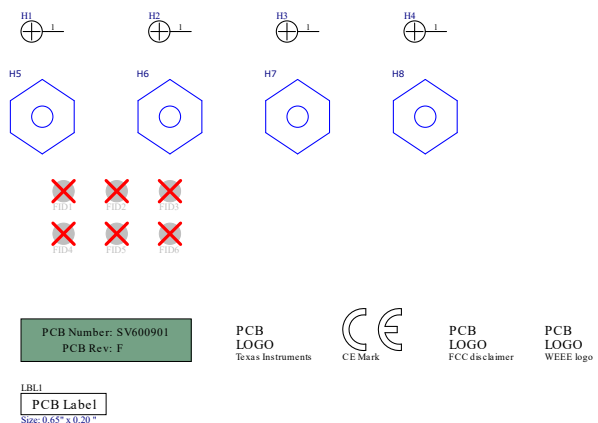


Figure 6-4. Power



Variant	Label Text
001	DS90UB928QEVM
002	DS90UH928QEVM
003	DS90UB924-Q1EVM

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only.

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Default Jumper Placement

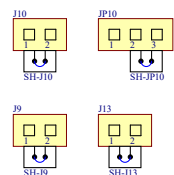


Figure 6-5. Hardware

7 Bill of Materials

Table 7-1. DS90UH928QEVM Bill of Materials

Item	Designator	Part Number	Quantity	Manufacturer	Package Reference	Value
1	C1, C2, C4, C5, C6, C9, C13, C14, C17, C18	GCM21BR71C475KA73L	10	MuRata	0805	4.7uF
2	C7	GCM31CR70J226KE23L	1	MuRata	1206	22uF
3	C10, C11	GRM033C71C104KE14D	2	MuRata	0201	0.1uF
4	C12, C19, C22, C23, C33, C35, C37, C39, C44, C45	GRM188R71H104KA93D	10	MuRata	0603	0.1uF
5	C15, C16	GCM155R71C104KA55D	2	MuRata	0402	0.1uF
6	C24	GRM188R61E106MA73D	1	MuRata	0603	10uF
7	C25, C29	C1005X7R1H104K050BB	2	TDK	0402	0.1uF
8	C26, C31	GRM1555C1H100JA01D	2	MuRata	0402	10pF
9	C27, C30, C50	293D226X0025D2TE3	3	Vishay-Sprague	7343-31	22uF
10	C28	293D225X9025A2TE3	1	Vishay-Sprague	3216-18	2.2uF
11	C32, C34, C36, C38	C3216X7R1C106K160AC	4	TDK	1206_190	10uF
12	C40, C42	F931E226MNC	2	AVX	7343-31	22uF
13	C41, C43	T491B225K020AT	2	Kemet	3528-21	2.2uF
14	C46, C52, C60, C61	0603YC104JAT2A	4	AVX	0603	0.1uF
15	C47, C56	06035A221FAT2A	2	AVX	0603	220pF
16	C48	0805YD225KAT2A	1	AVX	0805	2.2uF
17	C49	C1608X7R1H103K080AA	1	TDK	0603	0.01uF
18	C51	B37941K9105K62	1	TDK	0805	1uF
19	C53, C54	GRM1885C2A300JA01D	2	MuRata	0603	30pF
20	C55	C0603X222K5RACTU	1	Kemet	0603	2200pF
21	C57	GRM188R71A474KA61D	1	MuRata	0603	0.47uF
22	C58, C59	GRM155R71C104KA88D	2	MuRata	0402	0.1uF
23	D1	LTST-C191KRKT	1	Lite-On	LED_0603	Red
24	D2	APHHS1005CGCK	1	Kingbright	0402	Green
25	D3	1N5819HW-7-F	1	Diodes Inc.	SOD-123	40V
26	D4	1SMB5922BT3G	1	ON Semiconductor	SMB	7.5V
27	D5	150060VS75000	1	Würth Elektronik	LED_0603	Green
28	FB1	BK1608HS600-T	1	Taiyo Yuden	0603	60 ohm
29	H1, H2, H3, H4	NY PMS 440 0025 PH	4	B&F Fastener Supply	Screw	
30	H5, H6, H7, H8	1902D	4	Keystone Electronics	HEX_STANDOFF_#4-40	

Table 7-1. DS90UH928QEVM Bill of Materials (continued)

Item	Designator	Part Number	Quantity	Manufacturer	Package Reference	Value
31	J2, J3, J6, J7	142-0701-851	4	Cinch Connectivity	SMA End Launch	
32	J4	D4S20D-40ML5-Z	1	Rosenberger	HSD connector, Waterblue	
33	J5, JP2	TSW-110-07-G-D	2	Samtec	10x2 Header	
34	J8	0022112042	1	Molex	Header 4x1 keyed	
35	J9, JP3, JP5, JP6, JP7, JP8, JP9	TSW-102-07-T-S	7	Samtec	Header, 2.54mm, 2x1, TH	
36	J10, J13	5-146261-1	2	TE Connectivity	Header, 2x1, 100mil	
37	J11, J14, J15, J16	1502-2	4	Keystone	Keystone1502-2	
38	J12	PJ-102A	1	CUI Inc.	POWER JACK, 14.4x11x9mm	
39	J17	1734035-2	1	TE Connectivity	USB Mini Type B	
40	JP1, JP4, JP10	TSW-103-07-T-S	3	Samtec	Header, 2.54mm, 3x1, TH	
41	L1	ACM2012H-900-2P-T03	1	TDK	SMT_CMC_2MM0_1MM2	
42	L2, L3	BLM15AX102SN1D	2	MuRata	0402	1000 ohm
43	LBL1	THT-14-423-10	1	Brady	PCB Label 0.650 x 0.200 inch	
44	Q1	BSS138	1	Fairchild Semiconductor	SOT-23	50V
45	R1, R2, R11, R59, R60, R61, R62	MCR01MZPJ000	7	Rohm	0402	0
46	R3, R4, R5, R6, R7, R8, R9, R10	ERJ-3EKF1002V	8	Panasonic	0603	10.0k
47	R15, R18	ERJ-2RKF3300X	2	Panasonic	0402	330
48	R20	ERJ-2RKF1000X	1	Panasonic	0402	100
49	R21	CRCW04029K09FKED	1	Vishay-Dale	0402	9.09k
50	R22	CRCW040213K7FKED	1	Vishay-Dale	0402	13.7k
51	R23	CRCW040215K0FKED	1	Vishay-Dale	0402	15.0k
52	R24	CRCW040215K4FKED	1	Vishay-Dale	0402	15.4k
53	R25	CRCW040217K4FKED	1	Vishay-Dale	0402	17.4k
54	R26	CRCW040218K7FKED	1	Vishay-Dale	0402	18.7k
55	R27	CRCW040220K0FKED	1	Vishay-Dale	0402	20.0k
56	R28	CRCW040221K5FKED	1	Vishay-Dale	0402	21.5k
57	R29, R34	CRCW040222K6FKED	2	Vishay-Dale	0402	22.6k
58	R30, R64	CRCW040229K4FKED	2	Vishay-Dale	0402	29.4k
59	R31, R33	CRCW040225K5FKED	2	Vishay-Dale	0402	25.5k
60	R32	CRCW040226K7FKED	1	Vishay-Dale	0402	26.7k
61	R35	CRCW040220K5FKED	1	Vishay-Dale	0402	20.5k
62	R36	CRCW040216K2FKED	1	Vishay-Dale	0402	16.2k

Table 7-1. DS90UH928QEVM Bill of Materials (continued)

Item	Designator	Part Number	Quantity	Manufacturer	Package Reference	Value
63	R37	CRCW040212K4FKED	1	Vishay-Dale	0402	12.4k
64	R38	CRCW040230K1FKED	1	Vishay-Dale	0402	30.1k
65	R39, R56	CRCW040221K0FKED	2	Vishay-Dale	0402	21.0k
66	R40, R55	CRCW040219K1FKED	2	Vishay-Dale	0402	19.1k
67	R41, R54	CRCW040216K5FKED	2	Vishay-Dale	0402	16.5k
68	R42	CRCW040215K8FKED	1	Vishay-Dale	0402	15.8k
69	R43	CRCW040214K0FKED	1	Vishay-Dale	0402	14.0k
70	R44	CRCW040212K7FKED	1	Vishay-Dale	0402	12.7k
71	R45	CRCW040211K3FKED	1	Vishay-Dale	0402	11.3k
72	R46	CRCW04029K76FKED	1	Vishay-Dale	0402	9.76k
73	R47, R48	ERJ-2RKF4022X	2	Panasonic	0402	40.2k
74	R49	CRCW04024K02FKED	1	Vishay-Dale	0402	4.02k
75	R50	CRCW04024K99FKED	1	Vishay-Dale	0402	4.99k
76	R51	CRCW04027K68FKED	1	Vishay-Dale	0402	7.68k
77	R52	CRCW040210K2FKED	1	Vishay-Dale	0402	10.2k
78	R53	CRCW040213K0FKED	1	Vishay-Dale	0402	13.0k
79	R57, R58	ERJ-3GEYJ472V	2	Panasonic	0603	4.7k
80	R63, R66, R84	CRCW040210K0FKED	3	Vishay-Dale	0402	10.0k
81	R65	CRCW04023K24FKED	1	Vishay-Dale	0402	3.24k
82	R67, R83	CRCW04020000Z0ED	2	Vishay-Dale	0402	0
83	R68	CRCW12060000Z0EA	1	Vishay-Dale	1206	0
84	R69	CRCW06032K49FKEA	1	Vishay-Dale	0603	2.49k
85	R70	CRCW06039K31FKEA	1	Vishay-Dale	0603	9.31k
86	R71, R72	ERJ-2GEJ104X	2	Panasonic	0402	100k
87	R73, R74	CRCW06035K62FKEA	2	Vishay-Dale	0603	5.62k
88	R75, R76	CRCW040233R0JNED	2	Vishay-Dale	0402	33
89	R77	CRCW04021K50JNED	1	Vishay-Dale	0402	1.5k
90	R78, R82	CRCW040233K0JNED	2	Vishay-Dale	0402	33k
91	R79	CRCW06031M20JNEA	1	Vishay-Dale	0603	1.2Meg
92	R80	CRCW0603200RFKEA	1	Vishay-Dale	0603	200
93	S1	78B03T	1	Grayhill	9.7x9.65mm	
94	S2	78B04ST	1	Grayhill	DIP Switch, 4 Pos	
95	S3, S4	219-8MST	2	CTS Electrocomponents	Switch, 8Pos, 21.8x3.8x6.7 mm	
96	S5	208-9	1	CTS Electrocomponents	25.04x9.78mm	

Table 7-1. DS90UH928QEVM Bill of Materials (continued)

Item	Designator	Part Number	Quantity	Manufacturer	Package Reference	Value
97	S6	KSR221GLFS	1	C&K Components	KSR	
98	SH-J9, SH-J10, SH-J13, SH-JP10	SNT-100-BK-G	4	Samtec	Shunt	1x2
99	SW1	ADTSM31NV	1	APEM	6x3.51mm	
100	T1	ACM9070-701-2PL-TL01	1	TDK	9x7mm	
101	U1	DS90UB928QSQX/NOPB	1	Texas Instruments	RHS0048A	
102	U2	LM2941LD/NOPB	1	Texas Instruments	NGN0008A	
103	U3, U4	LP38693MP-ADJ/NOPB	2	Texas Instruments	NDC0005A	
104	U5	TPD4E004DRYR	1	Texas Instruments	DRY0006A	
105	U6	TPS73533DRBR	1	Texas Instruments	DRB0008A	
106	U7	MSP430F5529IPNR	1	Texas Instruments	PN0080A	
107	U8	TCA9406DCUR	1	Texas Instruments	DCU0008A	
108	Y1	ABM3-24.000MHZ-D2Y-T	1	Abracon Corporation	ABM3	

8 Board Layout and Layers

The following mechanical drawings (not to scale) illustrate the physical layout and stack-up of the 4-layer DS90UH928QEVM evaluation board:

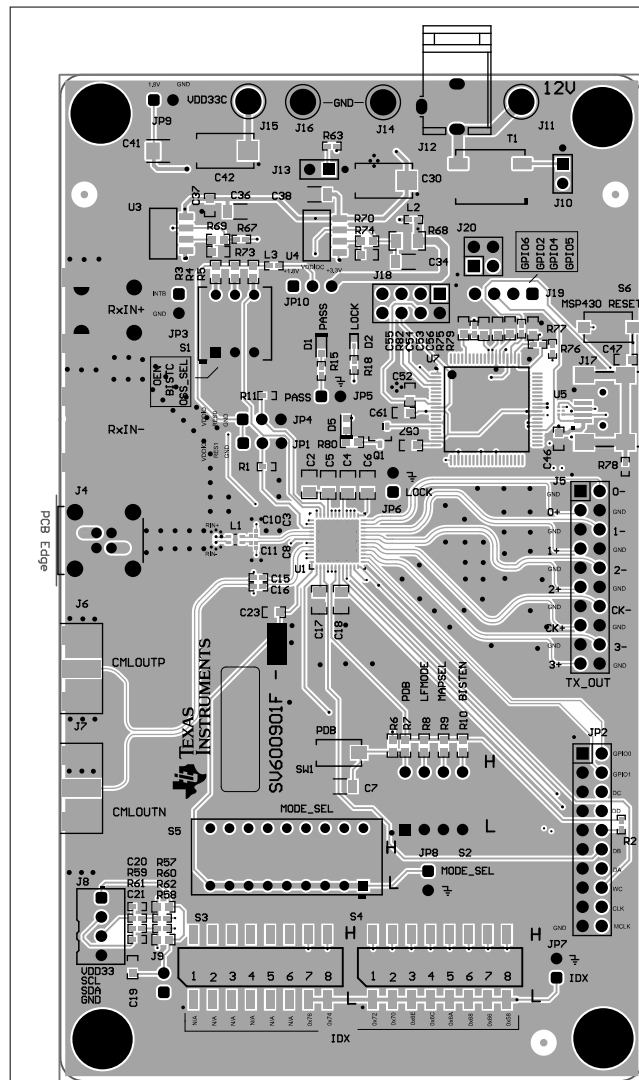


Figure 8-1. Top Silkscreen

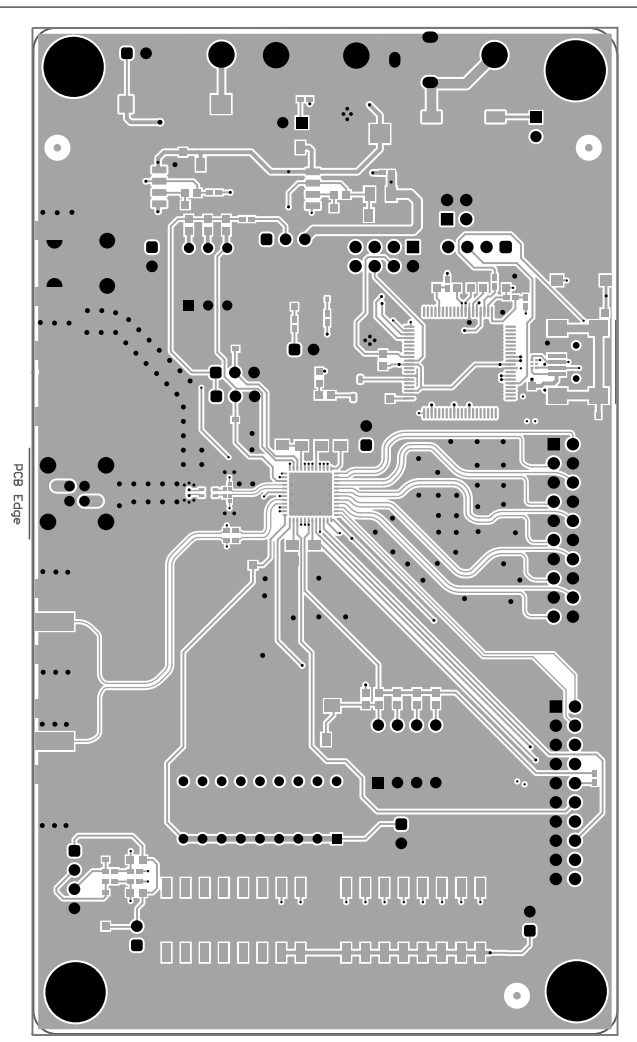


Figure 8-2. Top Layer

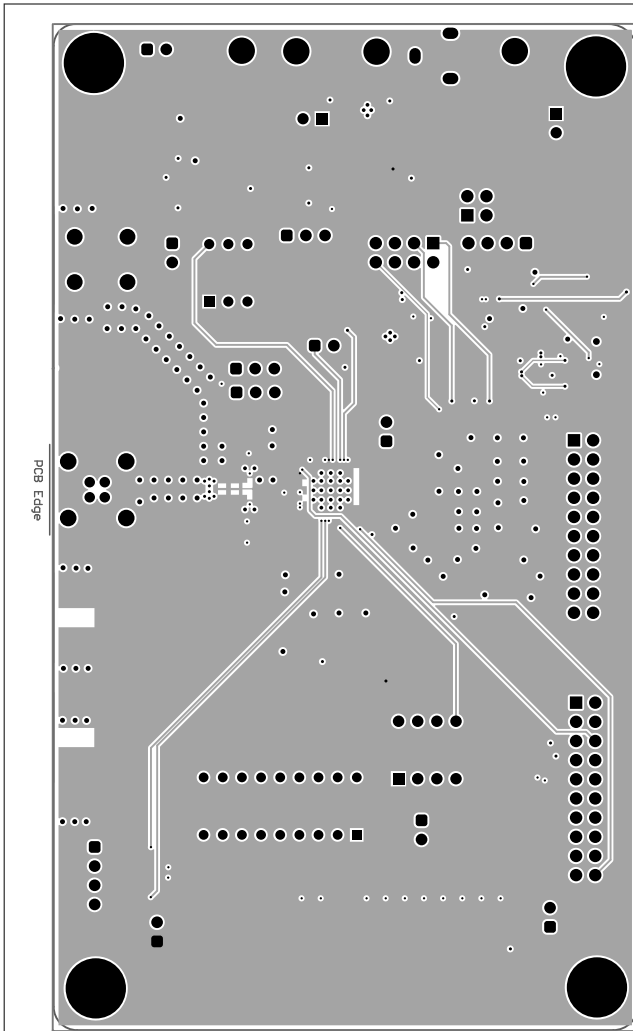


Figure 8-3. Internal Layer 1: Signals

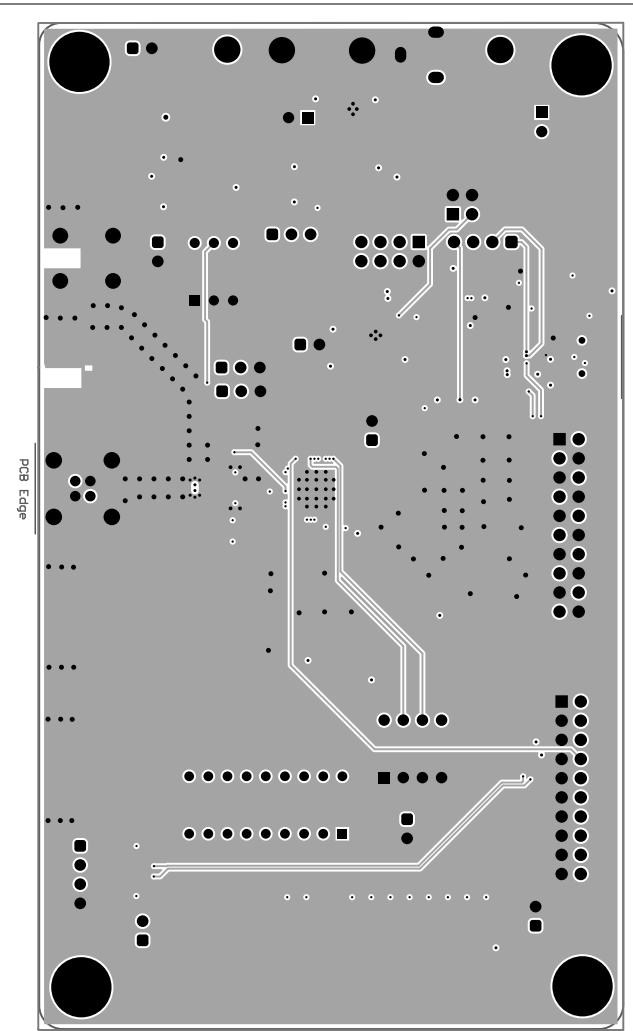


Figure 8-4. Internal Layer 2: Signals 2

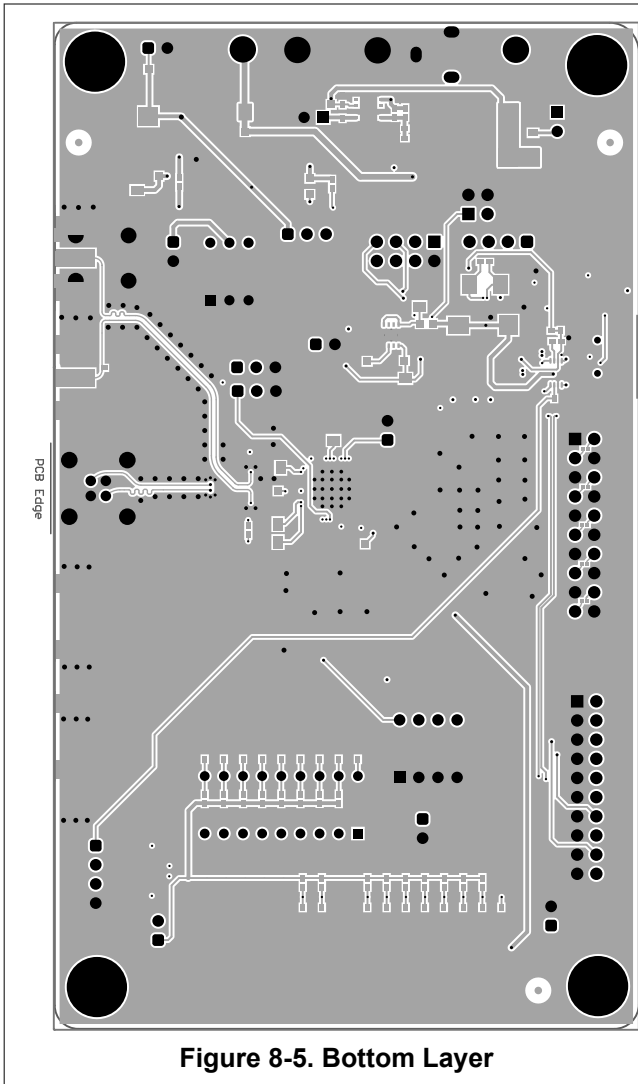


Figure 8-5. Bottom Layer

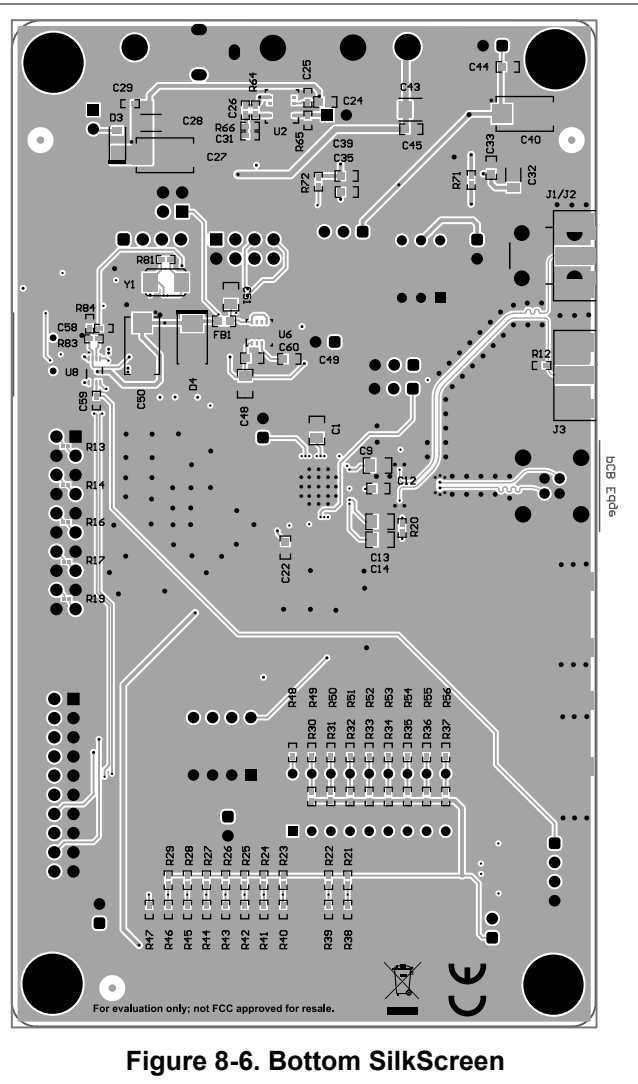


Figure 8-6. Bottom SilkScreen

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2013) to Revision A (June 2024)

Page

- Updated document throughout to reflect hardware redesign..... 2

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
 - 1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software
 - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
2. *Limited Warranty and Related Remedies/Disclaimers:*
 - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
 - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.
 - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGRADATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 Regulatory Notices:

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html>

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。技術適合証明を受けていないものご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。日本テキサス・イ

ンスツルメンツ株式会社

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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。 <https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html>

3.4 European Union

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

-
4. *EVM Use Restrictions and Warnings:*
 - 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
 - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
 - 4.3 *Safety-Related Warnings and Restrictions:*
 - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
 - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
 - 4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.
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