

DS100BR111EVK User's Guide SMA Evaluation Kit

User's Guide



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DS100BR111EVK User's Guide

SMA Evaluation Kit

The DS100BR111EVK – SMA evaluation kit provides a complete high band-width platform to evaluate the signal integrity and signal conditioning features of the Texas Instruments signal conditioning products – with Equalization and De-emphasis.

SMA edge launch connectors are used as the input and the output connections for this evaluation board. Commercially available adaptor boards can be purchased to facilitate connection to cables or backplane interconnects.

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1 Features

- Two Channel Repeater up to 10.3 Gbps Rate
 - DS100BR111: 1x Bidirectional Lane
- Low 65mW/channel Power Consumption, with Option to Power Down Unused Channels
- Advanced Signal Conditioning Features
 - 4 Stage Equalization
 - Transmit De-Emphasis
 - Transmit VOD Control
 - < 0.3 UI of Residual DJ at 10 Gbps
- Fully Programmable via Pin Selection or SMBus Interface
- Selectable Single Supply Operation
- >4 kV HBM ESD Rating
- 3.3 V LVCMOS Input Tolerant for SMBus Interface
- Flow-Thru Pinout Package: 24-Pin LLP (4 mm x 4 mm)
- Industrial –40 to 85°C Operating Temperature Range

2 Applications

- High-Speed Active Copper Cable Modules and FR4 Backplanes in Communication Systems
- 10GE, FC, SAS, SATA 3/6 Gbps (with OOB detection), Infiniband, CPRI, RXAUI, and many others

3 Demo Kit Contents

- End User License Agreement
- DS100BR111EVK User Guide Rev.1.2
- DS100BR111EVK Board

4 Ordering Information

Table 1. DS100BR111AEVK Ordering Information

DEVICE	QUANTITY
DS100BR111SQ/NOPB	2000
DS100BR111SQE/NOPB	250
SMA Evaluation Kit: DS100BR111EVK/NOPB	

5 Evaluation Board

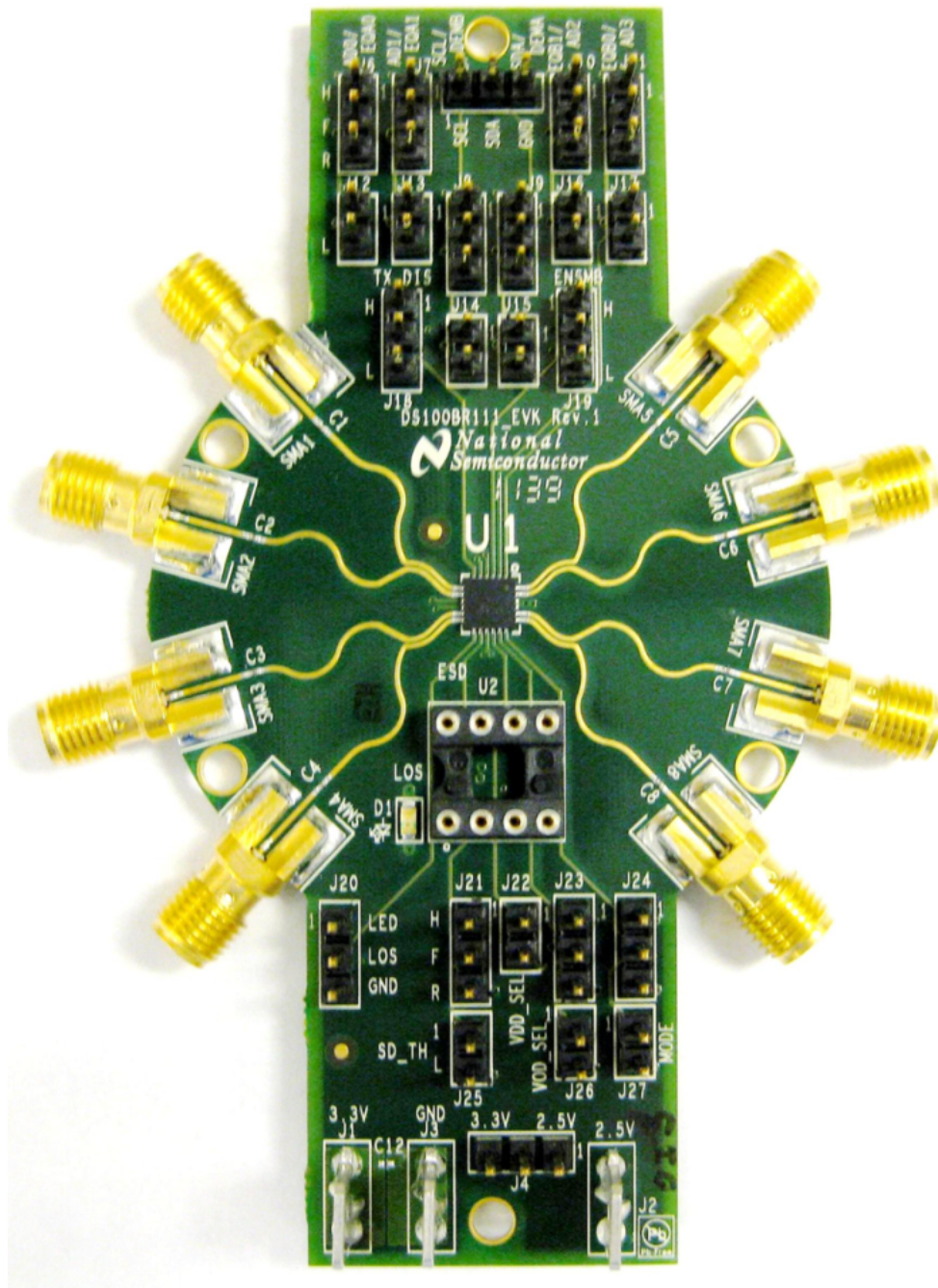


Figure 1. DS100BR111EVK Evaluation Board

6 Setup

The DS100BR111EVK – SMA evaluation kit can be used in three different modes:

1. **Pin Control** (provides access to selected signal integrity settings)
2. **SMBus Mode** (full access to signal integrity and control settings)
3. **EEPROM Mode** (full access to signal integrity and control settings)

The EEPROM mode is a convenient method of programming one or more DS100BRxxx devices on system power-up when a SMBus master (microcontroller or similar) is unavailable in the design.

6.1 DS100BR111 Pin Control

Uses the external control pins on the DS100BR111 to configure the signal integrity and control settings of the device. In this mode only a subset of the equalization and de-emphasis levels are available. Due to the limited number of control pins, a limited bandwidth 4-level input scheme has been implemented across the control pin interface. This allows for improved EQ, DE, and VOD control with fewer physical pins.

The 4 levels are defined as:

1. **Low:** 1 K Ω to GND
2. **Resistor:** 20 K Ω to GND
3. **Float:** No External Connection
4. **High:** 1 K Ω to VDD

The EVK interfaces to this 4-level IO using the setup below. Only one shunt connection is required to access any of the 4 levels. This methodology minimizes the risk of improper connections that could damage the board or board power supply.

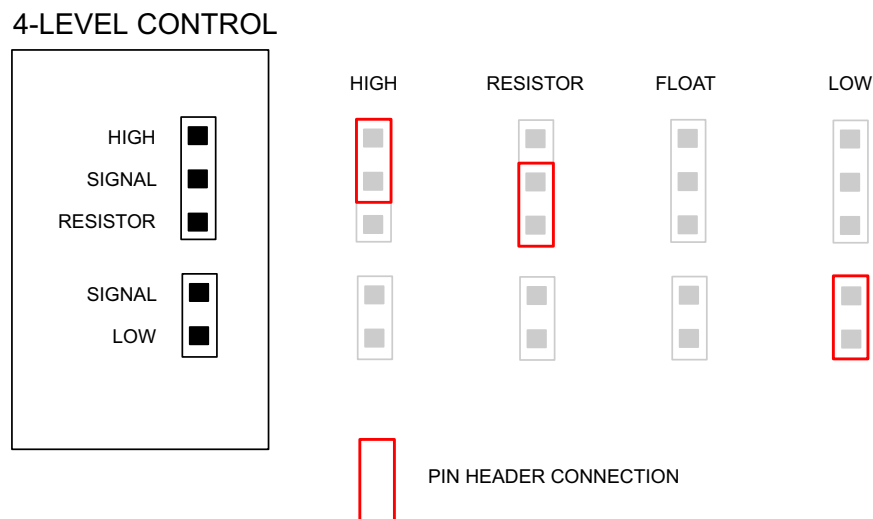


Figure 2. 4-Level IO Control on EVK

The DS100BR111 EVKs are shipped ready to use in pin control configuration. As delivered, the EVK will have the following installed jumpers.

1. J4 – 3.3 V operation: Use the J1 and J3 connectors to supply 3.3 V power to the EVK.
2. J18 – TX-DIS = LOW: Device is enabled.
3. J19 – ENSMB = LOW: PIN CONTROL configuration mode.
4. J20 – LED – LOS: The LOS output is connected to the onboard LED. The LED will glow green in the presence of a valid signal on CH A input.
5. J22 – VDD_SEL = LOW: Use DS100BR111A internal regulator to convert 3.3 V supply to proper internal supply level of 2.5 V. Note: The 2.5 V level may be observed on the device VDD pins.
6. VOD_SEL = Float: Default output amplitude settings for CH A and CH B.

6.2 SMBus Mode

The SMBus can also be used to control the DS100BR111 devices. This method has the advantage of independent control and finer signal conditioning granularity.

Table 2. Typical DS100BR111 Register Writes

Register Address	Function	Description
Register 0x0F	CHA EQ	Write EQ setting à 1B'h
Register 0x11	CHA DEM	Write DE setting for bits [2:0] = 000'b
Register 0x23	CHA VOD	Write VOD setting for bits [4:2] = 101'b
Register 0x06	CRC DIS	Write bit [3] = 1'b send register updates directly to channel without any CRC check.

6.3 EEPROM Mode

A serial EEPROM may also be used to configure one or more DS100BR111 devices. This configuration mode is accessed by setting the ENSMB 4-level input to FLOAT. For additional information please see the device datasheet.

7 Expected Results

This evaluation board has been designed to evaluate the cable and/or FR4 signal conditioning performance of the DS100BR111. Adding additional cables or adaptor boards into the signal path will have some impact on the optimal settings, but keeping the adaptor boards small and using short high-quality SMA cables will minimize this effect.

7.1 Cable Performance

When used in a full active cable application, it is generally expected that the DS100BR111 driving the cable will use a VOD setting of 1000 mV or greater and no output De-Emphasis (DE). The DS100BR111 receiving the signal will utilize a Continuous Time Linear Equalizer (CTLE) to recover the attenuated signal and redrive it into the local system.

SETUP1: PRBS7 Generator → BR111 (A) → 10m 30AWG cable → DS100BR111 (B) → Scope

DS100BR111A (A) Transmit Settings

1. Output Voltage Amplitude = 1000 mV or greater
2. De-Emphasis = 0 dB
3. EQ = 00 (Bypass)

DS100BR111A (B) Receive Settings

1. Output Voltage Amplitude = 700 mV or greater
2. De-Emphasis = 0 dB
3. EQ = 2F'h (Default)

Additional documentation and device performance is available in the device datasheet.

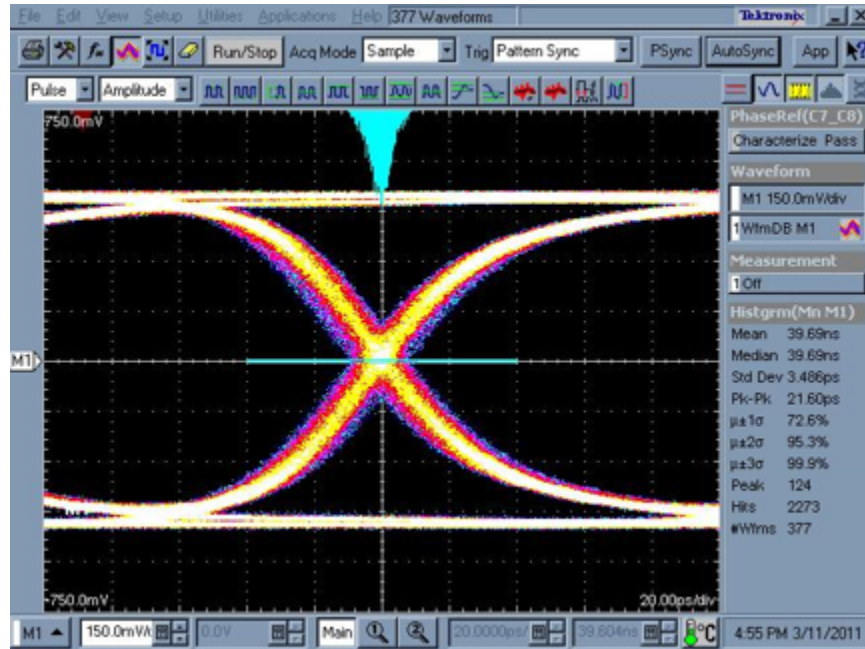


Figure 3. 6 Gbps Eye Diagram at SCOPE in SETUP1

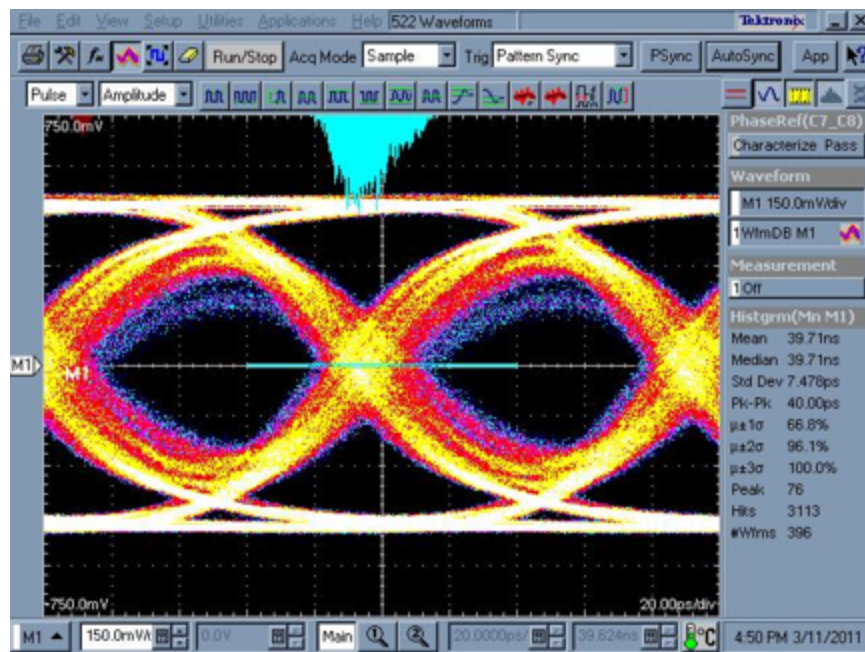
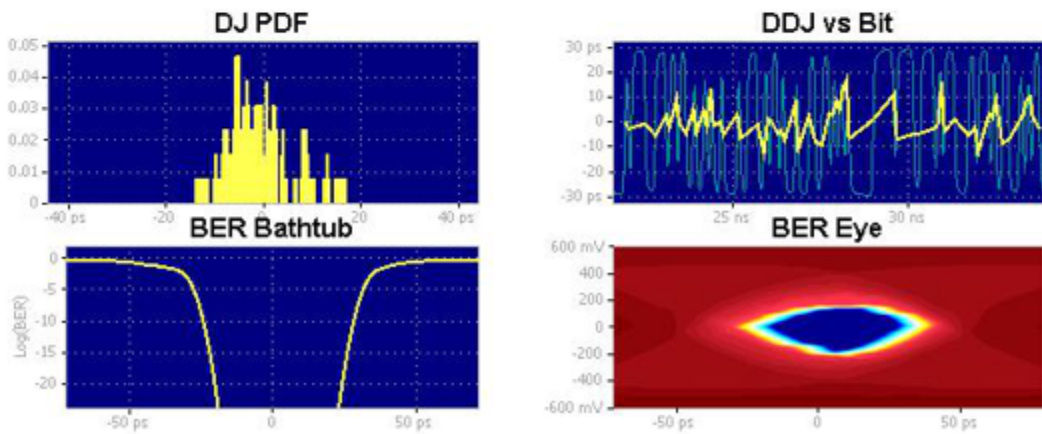


Figure 4. 10.3125 Gbps Eye Diagram at SCOPE in SETUP1

Data Source: MATH1	Data Rate: 10.3125 Gbps	Filter: None	
SSC: Off	Pattern: 127 bits	Channel: None	
Phase Reference: 10.3125 GHz	Sample Count: 52.70 k	Equalizer: None	
Jitter (Decision Threshold: 2.87 mV)		Noise (Sampling Phase: 0 UI)	
Random Jitter		Random Noise	
RJ (RMS)	= 1.28 ps	RN (RMS)	= 2.17 mV
RJ(h) (RMS)	= 1.27 ps	RN(v) (RMS)	= 2.16 mV
RJ(v) (RMS)	= 177.69 fs	RN(h) (RMS)	= 279.32 μ V
Deterministic Jitter		Deterministic Noise	
DJ	= 30.26 ps	DN	= 424.41 mV
DDJ	= 28.10 ps	DDN	= 414.39 mV
DCD	= 466.71 fs	DDN(level 1)	= 340.70 mV
DDPWS	= 23.65 ps	DDN(level 0)	= 283.59 mV
PJ	= 821.85 fs	PN	= 9.97 mV
PJ(h)	= 0 s	PN(v)	= 9.97 mV
PJ(v)	= 821.85 fs	PN(h)	= 0 V
Total Jitter @ BER		Total Noise @ BER	
TJ (1E-12)	= 47.18 ps	TN (1E-12)	= 457.60 mV
Eye Opening (1E-12)	= 49.79 ps	Eye Opening (1E-12)	= 332.20 mV
		Eye Amplitude	= 789.80 mV
Dual Dirac		SSC Modulation	
RJ(d-d)	= 1.50 ps	Magnitude	= 0 ppm
DJ(d-d)	= 25.62 ps	Frequency	= 0 Hz



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Figure 5. Jitter Analysis: Breakdown into Dj, Rj, and Tj for 10.3125 Gbps Case

7.2 FR4 Performance

The output de-emphasis of the DS100BR111 allows for flexible placement options on the receive system board. Even at 10.3125 Gbps, a clean eye can be achieved nearly 20" away without resorting to expensive board materials or special board stackups.

SETUP2: PRBS7 Generator → BR111 (A) → 15" FR4 (4 mil trace width) → Scope

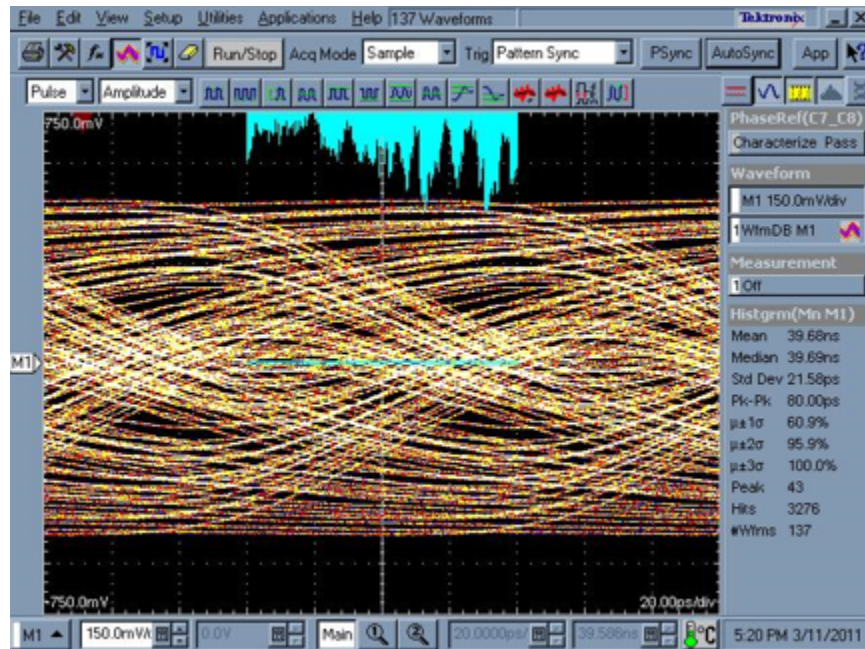


Figure 6. 10.3125 Gbps Eye Diagram at SCOPE in SETUP2 (DE Setting = 000)

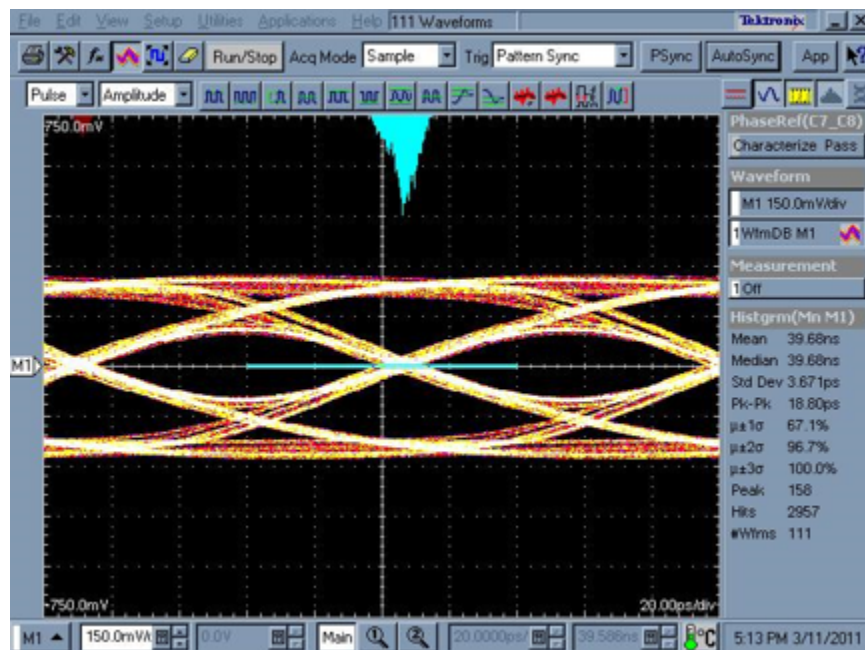


Figure 7. 10.3125 Gbps Eye Diagram at SCOPE in SETUP2 (DE Setting = 110)

8 Schematic

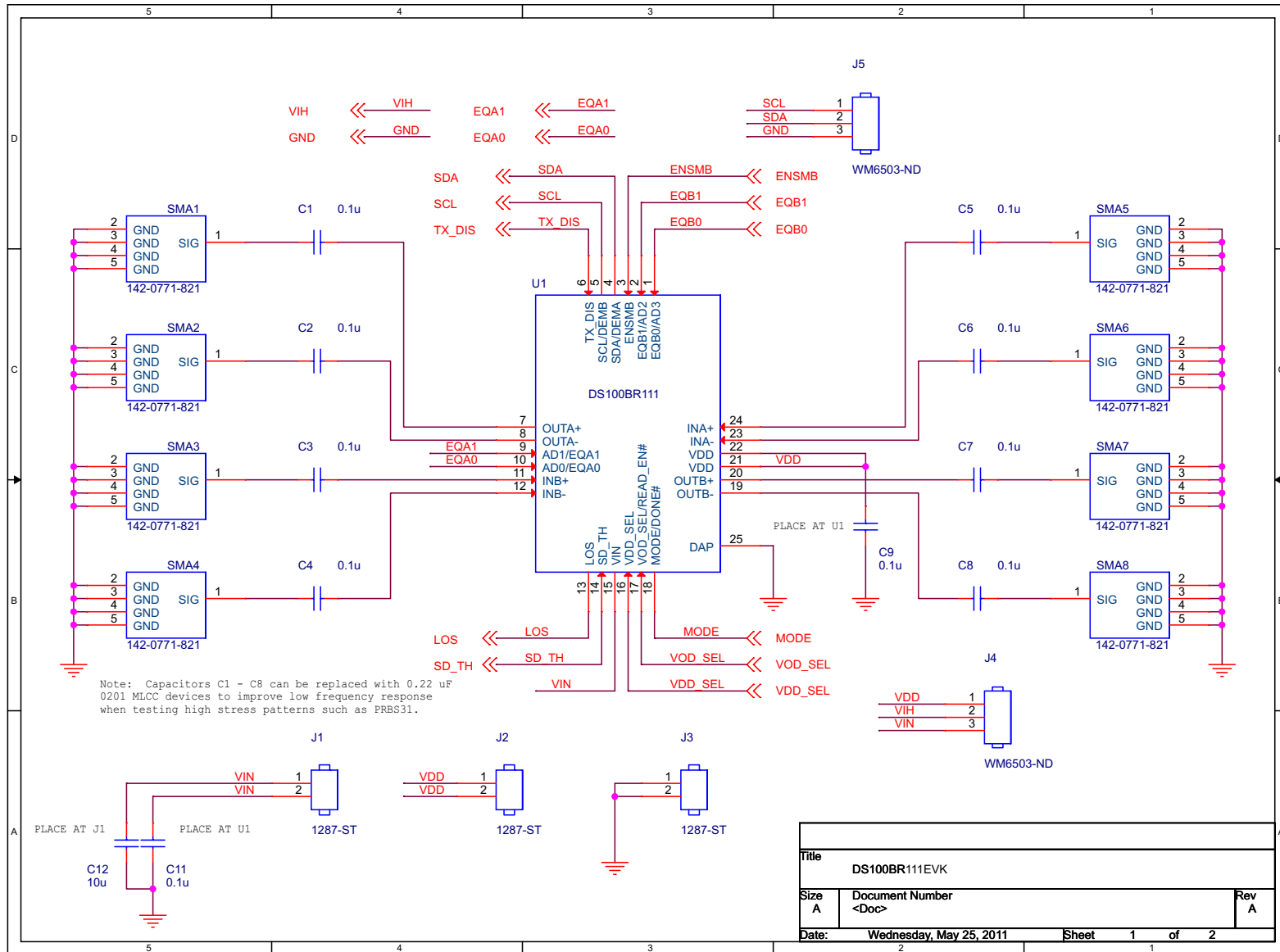


Figure 8. DS100BR111AEVK Schematic

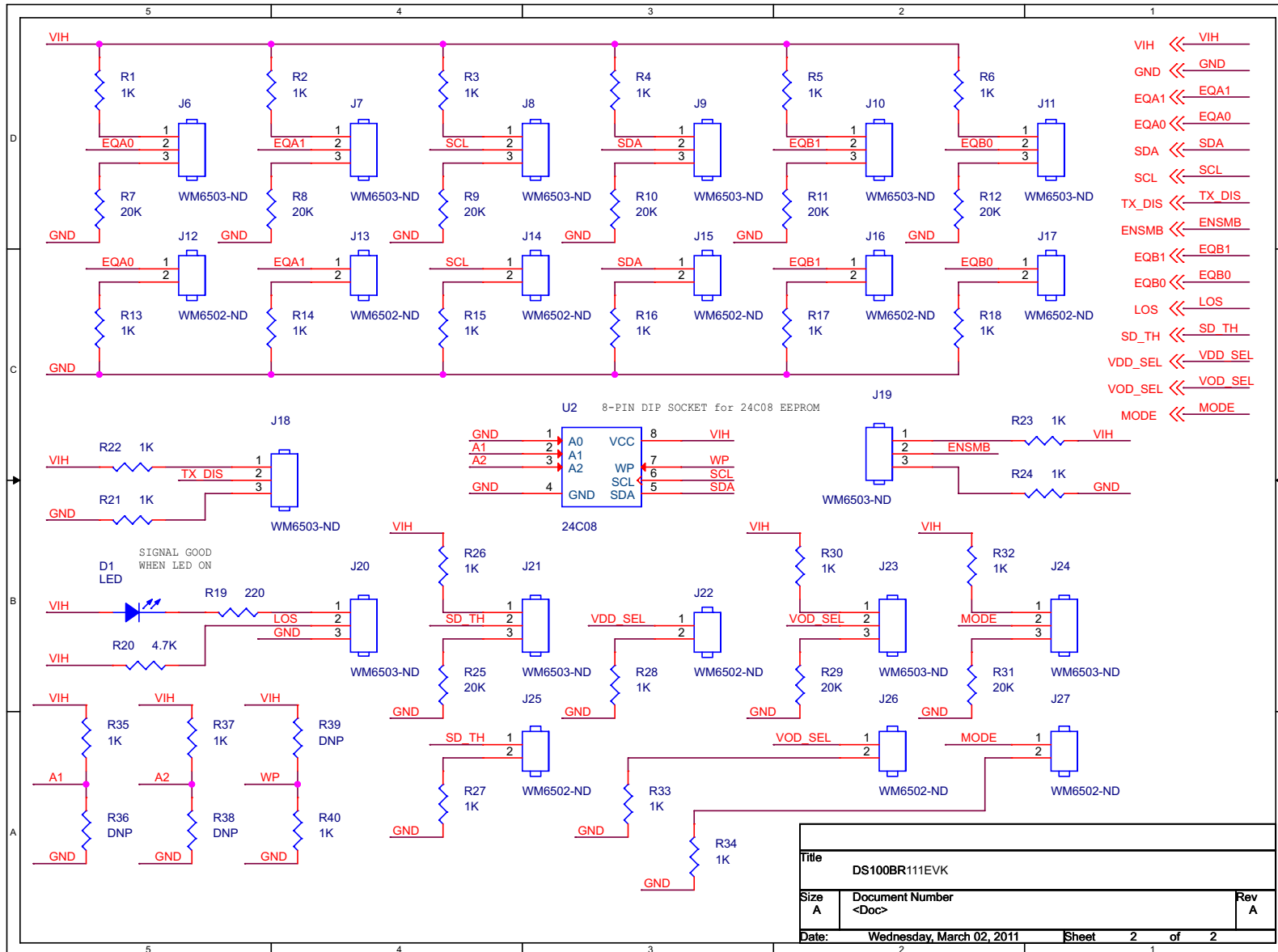


Figure 9. DS100BR111AEVK Schematic

9 Bill of Materials

Item	Quantity	Reference	Digikey PN	Manufacture PN	Descriptions
1	10	C1,C2,C3,C4,C5, C6,C7, C8,C9,C11	445-1796-1-ND	C0603X5R0J104K	CAP CERAMIC .1UF 6.3 V X5R 0201
2	1	C12	511-1502-1-ND	TCTAL1C226M8R	CAP TANT 22UF 16 V 20% SMD 1206
3	1	D1	160-1409-1-ND	LTST-C139KGKT	LED GREEN 0603 SMD
4	10	SMA1,SMA2,SMA3, SMA4, SMA5,SMA6, SMA7,SMA8, SMA9, SMA10,SMA11,SMA1 2	J807-ND	142-0771-821	CONN JACK SMA 50 Ω PC MOUNT
5	14	J4,J5,J6,J7, J8,J9,J10, J11,J18,J19, J20,J21,J23, J24	WM6503-ND	22-28-4033	CONN HEADER 3POS .100 VERT GOLD
6	10	J12,J13,J14, J15,J16,J17, J22,J25,J26,J27	WM6502-ND	22-28-4023	CONN HEADER 2POS .100 VERT GOLD
7	26	R1,R2,R3,R4, R5,R6,R13, R14, R15,R16,R17,R18, R21, R22,R23,R24, R26,R27,R28, R30, R32,R33,R34,R35, R37, R40	RHM1.0KJCT-ND	MCR01MZPJ102	RES 1.0K Ω 1/16W 5% 0402 SMD
8	9	R7,R8,R9, R10,R11,R12, R25, R29,R31	RHM20.0KLCT-ND	MCR01MZPF2002	RES 20.0K Ω 1/16W 1% 0402 SMD
9	1	R19	RHM220JCT-ND	MCR01MZPJ221	RES 220 Ω 1/16W 5% 0402 SMD
10	1	R20	RHM4.7KJCT-ND	MCR01MZPJ472	RES 4.7K Ω 1/16W 5% 0402 SMD
11	1	R41,R42	RHM0.0JCT-ND	MCR01MZPJ472	RES 0.0 Ω 1/16W 5% 0402 SMD
12	1	U1	NA	NSC	DS100BR111SQ/NOPB (24LLP - 4x4mm)
13	1	U2	ED90197-ND	115-43-308-41- 001000	IC SOCKET 8PIN DIP
14	3	R36,R38,R39	DNP	DNP	DNP

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

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This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

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2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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