*Application Report*
*SNOA467A–April 2006–Revised July 2006*

# *AN-1447 Improving PSRR and CMRR in Fully Differential Amplifiers*

## ABSTRACT

Power Supply Rejection Ratio (PSRR) and Common Mode Rejection Ratio (CMRR) are the two key specifications when it comes to characterizing and designing differential amplifiers. Although these amplifiers are designed to give best PSRR and CMRR performance, a careless application design and a poor selection of external components can significantly affect these specifications and degrade the overall performance. In this application note, we will look at some of the effects that external components have on PSRR and CMRR: mismatched external gain-setting resistors, the role of the bypass capacitor on PSRR, and some layout techniques that improve CMRR and PSRR.

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### Contents

### List of Figures

# 1 Introduction

Power Supply Rejection Ratio (PSRR) and Common Mode Rejection Ratio (CMRR) are the two key specifications when it comes to characterizing and designing differential amplifiers. Although these amplifiers are designed to give best PSRR and CMRR performance, a careless application design and a poor selection of external components can significantly affect these specifications and degrade the overall performance. In this application note, we will look at some of the effects that external components have on PSRR and CMRR: mismatched external gain-setting resistors, the role of the bypass capacitor on PSRR, and some layout techniques that improve CMRR and PSRR.

In Figure 1, a typical fully differential amplifier block diagram is shown with external gain resistors and an optional bias generator bypass capacitor. DC outputs at Vo1 and Vo2 are biased to half-$V_{DD}$ by internal bias circuitry. AC signals at Vo1 and Vo2 are 180° out of phase with respect to each other, creating a Bridge-Tied-Load (BTL) configuration. These amplifiers run with minimal component count, reducing layout time and system cost. Care must be taken to achieve the best possible performance from these amplifiers.

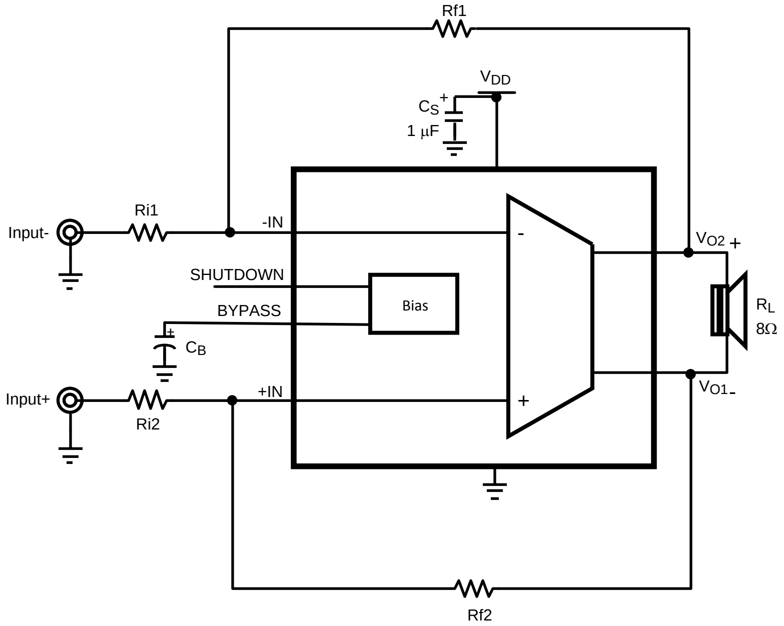

**Figure 1. Fully Differential Amplifier Block Diagram**

# 2 Application Information

## 2.1 MEASURING POWER SUPPLY REJECTION RATIO (PSRR)

The type of PSRR we are interested in here is an AC specification measuring the ability of the amplifier to reject AC-ripple voltage on the power supply bus, as opposed to a DC specification where we measure the change in output voltage for a change in supply voltage. Basically, ripple PSRR is the ratio of the differential output voltage to the supply ripple voltage expressed in dB as shown in Equation 1.

$$\text{PSRR} = 20\text{Log}\,\frac{V_{\text{out (ac)}}}{V_{\text{Ripple}}} \tag{1}$$

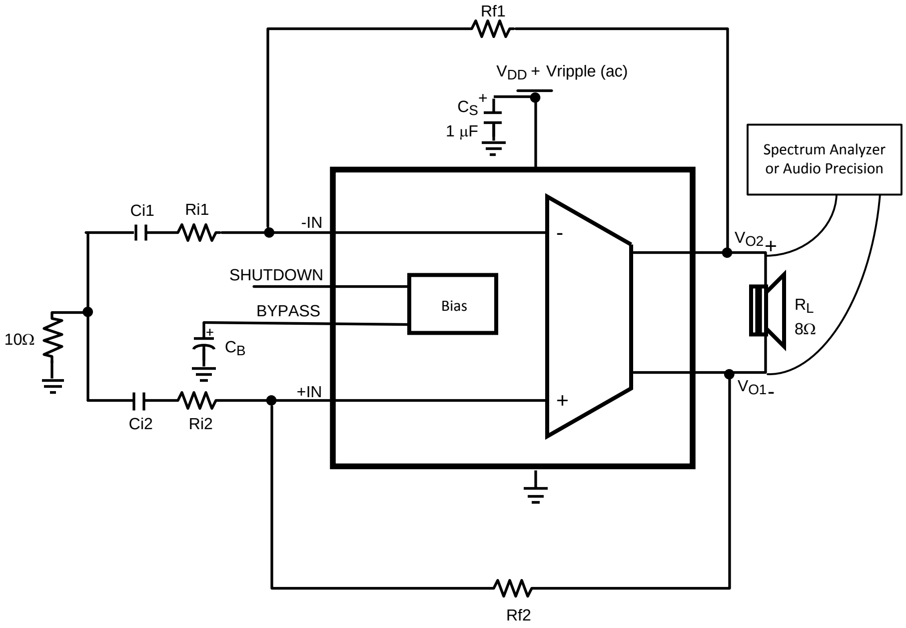

Figure 2. PSRR Measurement Test Circuit

A test circuit for measuring PSRR is shown in Figure 2. The amplifier's AC inputs are terminated to GND with a low value resistor—typically 10Ω. The value of the input capacitors Ci1 and Ci2 should be matched as closely as possible. Any mismatch can compromise PSRR performance at low frequencies. An alternate solution is the elimination of input coupling capacitors terminating the inputs directly to GND. A low-level AC voltage, in the range of 100mVpp to 500mVpp is combined with $V_{DD}$. This AC plus DC signal is applied to the amplifier's $V_{DD}$ pin. Any residual AC signal at the ripple frequency present across the BTL outputs is a function of the amplifier's PSRR. The magnitude of this residual signal is measured with an FFT (using a spectrum analyzer or Audio Precision instrument). Using Equation 1 gives the PSRR value in dB.

## 2.2 MEASURING COMMON MODE REJECTION RATIO (CMRR)

Common Mode Rejection Ratio is an ability of the differential amplifier to reject common mode input signal and is expressed in dB as shown in Equation 2.

$$\text{CMRR} = 20\text{Log}\frac{V_{\text{out (ac)}}}{V_{\text{cmi (ac)}}} \tag{2}$$

A test circuit for measuring CMRR is shown is Figure 3. The amplifier's AC inputs are connected to a common-mode AC input. Output can be measured by using a high precision AC Volt Meter or Audio Precision instrument. Equation 2 gives the CMRR measurement in dB. For differential input amplifiers with external gain-settings resistors, CMRR measurement is highly dependent on external resistors as well as board layout. This will be fully discussed in the next section. As a side note, a lot of newer audio measuring instruments such as Audio Precision can perform the CMRR test (and a lot of other audio parameters as well) automatically.

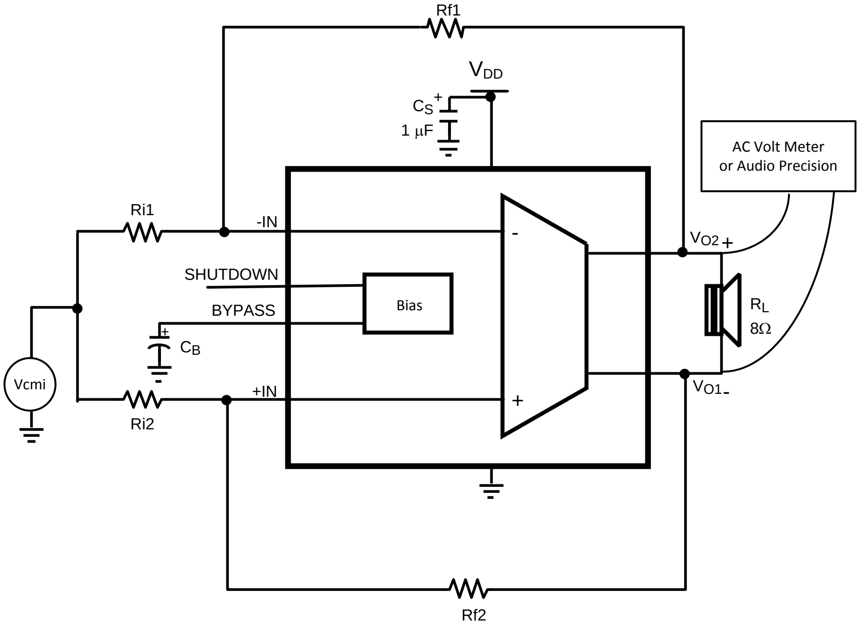

Figure 3. CMRR Measurement Test Circuit

## 2.3 EFFECTS OF EXTERNAL GAIN RESISTORS

It is extremely important to match the input resistors to each other as well as the feedback resistors to each other for best CMRR performance. When the inputs of the fully differential amplifier are DC-coupled, resistor matching differences generate net DC currents across the load because of the balanced nature of the differential amplifiers.

Internally these amplifiers consist of two circuits: a differential amplifier and a common-mode feedback amplifier that adjusts the output voltages so that the nominal DC output bias remains $V_{DD}/2$. Assuming that the amplifier' has two equal “halves.” Equation 3 can be obtained by the simple analysis of the differential amplifier in Figure 1 with Vcmi = 0V. Each half uses an input and feedback resistor (Ri and Rf) and contributes to each side of the equation. This equation shows an output offset DC voltage that can result because of resistor mismatching either between feedback resistors (Rf1 and Rf2) or input resistors (Ri1 and Ri2).

$$Vo2 - Vo1 = \frac{V_{DD}}{2}\left[\left(\frac{Ri2 + Rf2}{Ri1 + Rf1}\right)\left(\frac{Ri1}{Ri2}\right) - 1\right] \tag{3}$$

Ideally, when Ri1 = Ri2 and Rf1 = Rf2, we get perfectly matched and balanced input and feedback resistors pairs and no offset voltage. But if, for example, we assume:

Ri1 = Ri2 = R

Rf1 = 0.8R and Rf2 = 1.2R, with 20% tolerance in the feedback resistors.

We will get an offset voltage of about 0.45 Volts and load current of about 46mA assuming an 8Ω load connected across the output. Now that’s quite a big DC offset voltage! As a result, this reduces the battery life and could affect the speaker performance significantly because of extra DC current flowing through the voice coil. Common Mode Rejection Ratio is a parameter that can be gravely affected by mismatched gain resistors. A graph of Common Mode Rejection Ratio vs. feedback resistor mismatch is shown in Figure 4. As can be seen in the graph, a feedback resistor mismatch of 0.4 reduces the CMMR approximately 23dB from the ideal condition perfectly matched resistor.

PSRR is also affected by the gain resistors mismatch, but with a small capacitor on the bypass pin this effect is reduced extensively and yields practically no effect at all on the power supply rejection. The effects of bypass capacitor will be fully discussed in the next section. Thus, for all practical purpose, resistors of 1% tolerance or even better should be used for optimal performance and best common mode rejection ratio.

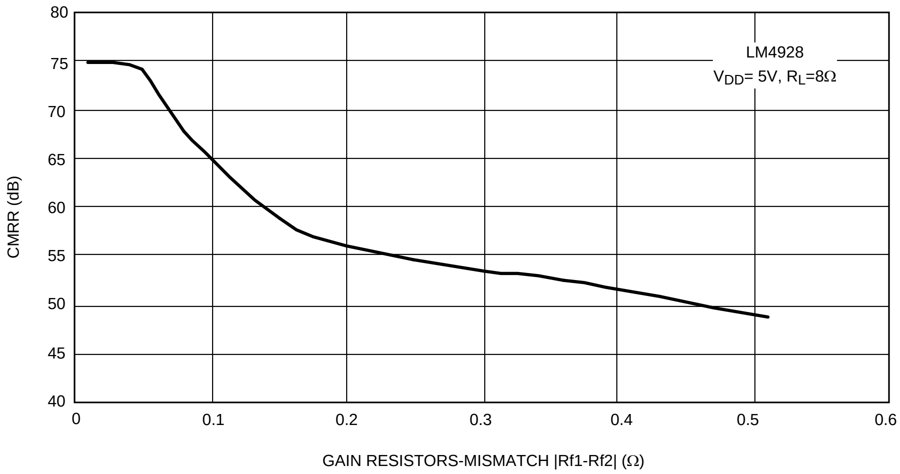

Figure 4. CMRR vs Feedback Resistor Mismatch

## 2.4 EFFECTS OF BYPASS CAPACITOR

Fully differential amplifiers offer an “optional” bypass capacitor ($C_B$) and allow a designer to use these amplifiers with minimal component count. Before eliminating the optional bypass capacitor to reduce component count, one should understand how that might affect the overall performance of the amplifier. Internally, a common mode amplifier adjusts the two outputs to a quiescent DC voltage equal to halve-$V_{DD}$. Any supply fluctuations cause both outputs to move in phase. This ideally creates a net change of $0V_{DC}$ differentially across the outputs. Thus, a bypass capacitor is not really required and can be considered optional. But in the real world, these amplifiers are not perfect. Furthermore, mismatch in the external resistors can result in unbalanced amplifier operation. PSRR is the most important parameter that would be affected significantly by eliminating the bypass capacitor.

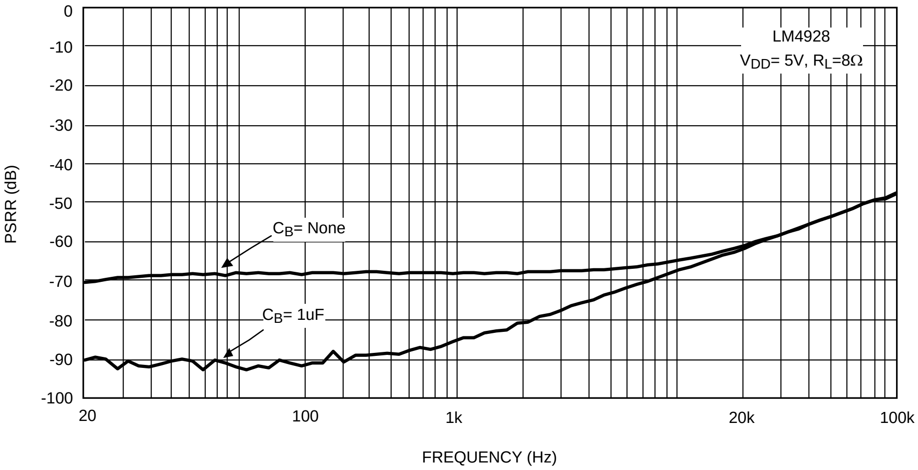

**Figure 5. PSRR vs Ripple Frequency**

Differential input amplifiers are considered excellent low noise and high PSRR amplifiers when compared to similar single-ended amplifiers. As shown in Figure 5 at low ripple frequencies, the PSRR is close to 70dB, even without a bypass capacitor. However, using a bypass capacitor in range of 0.1 uF to 1 uF offers a significant 20dB PSRR improvement. Depending upon the application, PSRR of 70dB might be considered good and more than adequate for most applications. However, in cell-phone market where an excellent PSRR is desired, particularly at lower frequencies, adding a bypass capacitor certainly will improve the lower frequencies power supply rejection. Furthermore, the amplifier will be less sensitive to slight gain resistor value mismatch.

## 2.5 LAYOUT CONSIDERATIONS

Printed circuit board layout is generally considered to be very application specific. Nevertheless, it is possible to observe some guidelines that optimize the overall performance of the amplifier. Fully differential amplifiers come in different packages.

Please contact the National Semiconductor Corp. website for package-specific applications information before attempting to start any new layout. Another important factor to consider is star ground vs. ground plane. This is very application and package specific. Either configuration is used when combined with the following general suggestions:

a) Make use of symmetrical placement of components (i.e. feedback resistors and input resistors).

b) If not using ground planes, $V_{DD}$ and GND traces should be as wide as possible.

c) If a heat-sink plane is desired for exposed-DAP packages, it should be appropriately sized. Refer to the power derating graphs in the corresponding datasheet.

d) The distance between the chip and any possible antenna source should be as far as possible.

e) If possible, make the output traces short and equal in length and away from the any antenna source.

f) If using a star ground, all the GNDs such as bypass capacitor GND, supply capacitor GNDs, and any other system ground should be directly connected to a single point on the board, possibly at the board's point of entry for the power supply GND.

## 3 Revision Table

| Rev | Date | Description |
|---|---|---|
| 1.0 | 04/20/06 | Initial release. |
| 1.1 | 07/24/06 | Simple text edits, then re-released the App Notes into the WEB. |

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