Application Report
SNOA504B–September 2007–Revised April 2013

AN-1716 Driving the ADC14DS105 High-Speed A/D Converter for High Performance

ABSTRACT

This application report discusses design implementation and focuses on how to provide input signals and clock to the ADC14DS105 by reading data from its serial interface. Also, the unique output drive details are reviewed.

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1 Introduction

The ADC14DS105 is a dual 14-bit 105 MHz converter with serial LVDS outputs. It has an input bandwidth of 1 GHz and a low power of 1W total. The ADC14DS105 is useful in many applications. Its dual channels are handy for I and Q channel processing, useful in the design of communication systems and basestations.

2 Input Signal Conditioning

Achieving 14-bit performance requires applying an input with good phase and amplitude matching to the differential pins of the analog input. Converters with switched cap inputs can be challenging, but this challenge can be overcome by using a good high frequency transformer or buffer amplifier such as the LMH6552.

Switched cap inputs loads are part of the sample-and-hold amplifier present in most high-speed Analog-to-Digital Converters (ADCs). Omitting on-board buffer amplifiers provides wide bandwidth without the power drain of a wide band amplifier. Unfortunately it presents a dynamic load to the devices driving the converter. This might be more commonly known as a “ping and ring.” When the ADC is driven by a transformer, the input capacitance makes a resonant circuit with its driving transformer. When the capacitor closes or opens, the change will result in a ring on both inputs. These rings must not be filtered, and most important is for them to settle before the next conversion. The most important quality of a driving transformer is gain and phase balance across secondary windings.

A typical transformer drive configuration is shown in Figure 1. Using this configuration, the ADC14DS105 will provide an SNR of 73 to 75 dBFS and an SFDR of 85 to 90 dBFS at input frequencies up to 100 MHz. For higher input frequencies other configurations are required, see the device-specific data sheet.

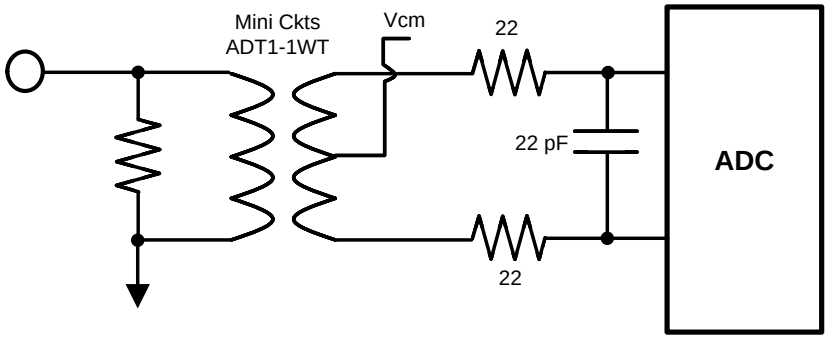

Figure 1. Transformer Drive Circuit

An LMH6552 may also be used to drive the converter. It provides isolation between the converters switched cap input in the signal source. Additionally, noise and anti aliasing filters may be easily constructed between the converter and the ADC14DS105.

Figure 2 illustrates a 4.3 MHz 2nd order Low-Pass (LP) filter between the LMH6552 and the ADC14DS105.

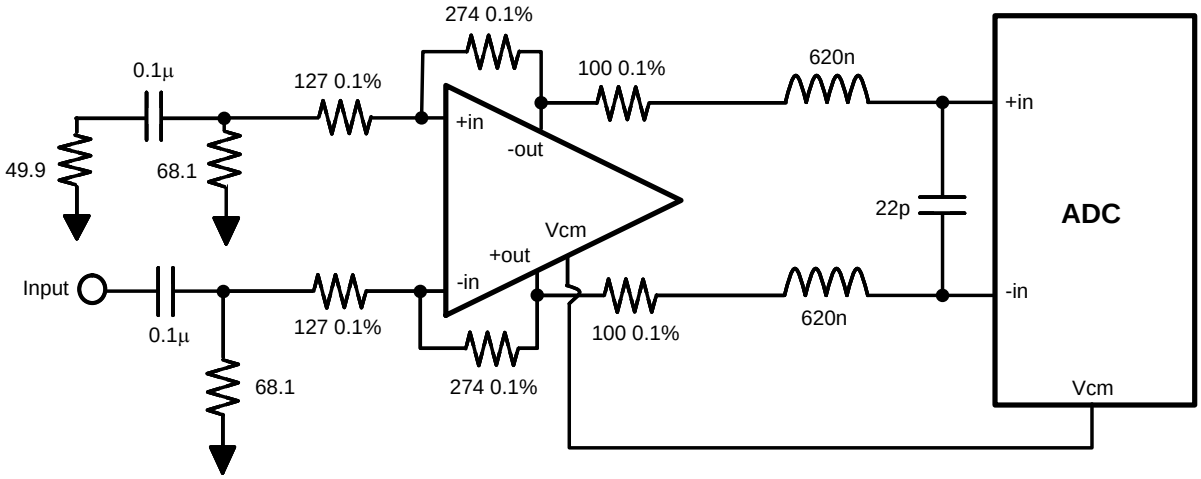

Figure 2. LMH6552 Driving a Circuit With 2nd Order Low Pass Filter

3 Clock Signal

There is a direct connection between clock jitter and SNR. The clock jitter path of the ADC14DS105 is less than 100 fs. Low jitter clock sources are required to preserve the superb jitter and SNR of the ADC14DS105. The SNR will be limited if an inferior source is used to generate the clock. Higher analog input frequencies require lower jitter clock sources. For specific data timing details, see the *ADC14DS105 Dual 14-Bit, 105 MSPS A/D Converter With Serial LVDS Outputs Data Sheet* (SNAS380).

The Pletronics 7745 or the Vectron VCC1 are used as clock sources on the ADC14DS105 eval board. Although their clock jitter is specified at 3 ps, we have found it to be less than 200 fs when used to encode the ADC. With a 240 MHz input, this yields an SNR of 71 dBFS. These clock sources give the best jitter when powered by 5V (appropriate buffers must be used to drive the ADC).

4 Output Interface

The ADC14DS105 is designed with an LDVS serial output format. Its output is shown in Figure 3. The serial differential LVDS outputs offer many design advantages over CMOS, including, lower pin count, higher noise immunity and lower radiated emissions.

There is a data cell with each clock edge, see the device-specific data sheet. To provide a complete 14-bit output word at a 105 MHz data rate, the output rate would have to be 14 * 105 MHz or 1.47 GHz. SerDes FPGAs give rise to bit error rates when capturing an ADC's output. Therefore, this high switching speed can be a challenge for digital capture.

To address this dilemma, The LVDS output of the ADC14DS105 is available in single lane or dual lane format. At lower frequencies, the data might be acquired through the single lane. At higher sample rates the dual lanes are used. The single or dual lane mode is selectable by exercising pin-48 of the converter.

In the dual lane mode, the data rate is divided by 2 and interleaved between the dual output ports. In our product evaluations, conversion clock rates up 65 MHz are used in the single lane mode. At conversion rates above 65 MHz the dual lanes are used. The "switchover point" between dual and single lane modes depends of the abilities of the digital data receiver (FPGA, etc).

Serial data clock and data frame are provided for ease of capturing data. A word alignment function is available on pin 47. It will shift the phase relationship between the serial clock and data. This is useful when timing race conditions appear in the data receive paths. The frame output provides a boundary for the data word.

The amplitude of the LVDS differential signals may be controlled by adjusting the programming resistor attached to pin-29 of the ADC.

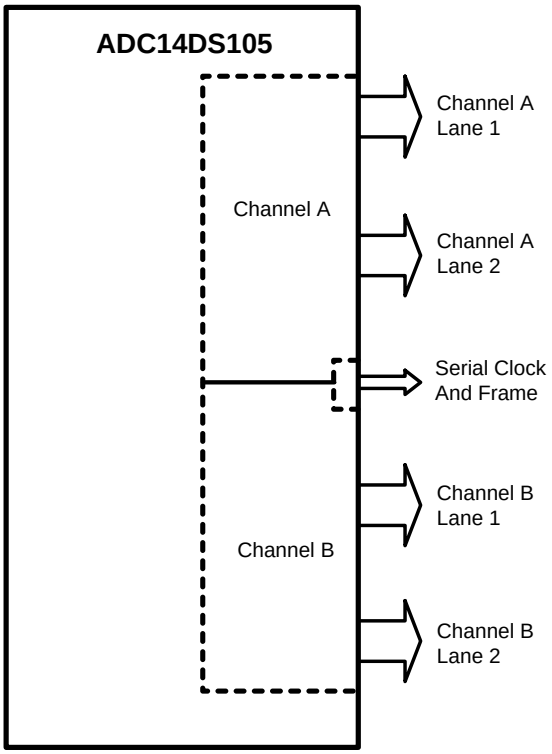

Figure 3. Output Ports

5 Additional Controls

A power-down function is available for individual channels on pins 57 and 20. Exercising this function on both channels will reduce power consumption to very low levels.

The OF/DCS pin of the converter (19) controls clock and data format functions. Through this function the clock duty cycle stabilizer may be controlled. This pin also determines the data output format (offset binary or 2's compliment.)

6 Summary

The ADC14DS105 is an easy-to-use high-bandwidth, low-power ADC. It provides design flexibility and performance enhancements that include high bandwidth with a low power solution.

7 References

ADC14DS105 Dual 14-Bit, 105 MSPS A/D Converter With Serial LVDS Outputs Data Sheet (SNAS380)

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