TP-14

TP-14 Low Voltage Techniques (Addendum to AN 211)

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Low Voltage Techniques*

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Abstract. *A micropower operational amplifier is described that will operate from a total supply voltage of 1.1V. The complementary Class-B output can swing within 10 mV of the supplies or deliver ±20 mA with 0.4V saturation. Common-mode range includes V⁻, facilitating single-supply operation. Otherwise, DC performance compares favorably with that of the LM108. An adjustable-output voltage reference is also presented that uses a new technique to eliminate the bow usually found in the temperature characteristics of the band-gap reference. Minimum supply is 1V, and typical drift is 0.002%/°C.*

introduction

The intrinsic operating voltage limit of bipolar ICs is only 100–200 mV greater than the emitter-base voltage of the transistors. To date, this limit has been pushed only with digital circuitry and relatively simple linear devices. This paper will deal with techniques for fabricating such devices as operational amplifiers, comparators, regulators and voltage references that work from a voltage as low as that supplied by a single nickel-cadmium cell.

Field-effect transistors have been considered for low-voltage applications because their operating voltage can theoretically be made less than that of bipolar transistors. Although their transconductance equals that of bipolar devices at very-low currents, it is considerably less even at moderate current densities. This limits FETs to such functions as input stages where the operating current is relatively low and well controlled.

A combined op amp, voltage reference and reference amplifier was chosen as a design example. A functional diagram is given in *Figure 1*. This configuration will serve to demonstrate that the usefulness of low-voltage operation goes beyond battery-powered equipment. It can be used in a floating mode, independent of fixed supplies. This is illustrated both by the floating voltage regulator in *Figure 2*, where the IC operates from the drive voltage to the pass transistors, and the remote comparator in *Figure 3*, where the IC functions as a 2-terminal device, driving TTL logic directly. A wide range of similar applications have been developed and are discussed elsewhere.[1]

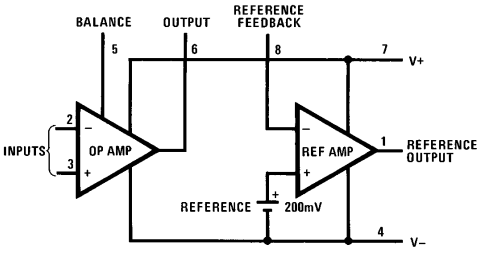

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Figure 1. Functional diagram of the design example

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†This work was performed under contract to National Semiconductor Corporation, Santa Clara, California.

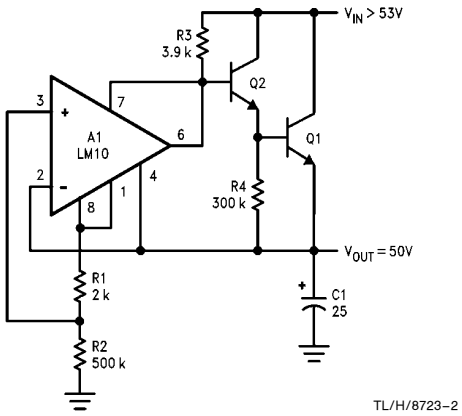

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Figure 2. High voltage regulator with bootstrapped control amplifier

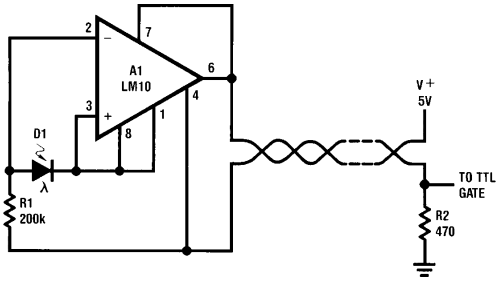

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Figure 3. Light level detector driving TTL directly over 2-wire line

Some small advantage might be gained by limiting operation to low voltages. This is overshadowed by the benefits of making a general-purpose IC. Therefore, it was decided to use standard processing with maximum operating voltages limited only by the BV_{CEO} of the transistors (50V–60V).

Ion-implanted resistors were incorporated to obtain the necessary high values for micropower operation. They also have the advantage that, with proper design, the speed/power tradeoffs can be determined at the final stages of processing by varying the implant dose. However, the advisability of doing this on a production basis has yet to be established.

operational amplifier design

A simplified schematic of the op amp is given in *Figure 4*. Lateral PNP transistors are used on the input because this is the easiest way to secure operation at common-mode voltages equal to the negative supply voltage. Processing that yields typical PNP current gains greater than 100 at low

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currents has been in production for nearly 10 years. These lateral transistors also have relatively constant current gain over temperature, giving lower bias-current drift than NPNs.

Protective resistors have been included in the input leads so that current does not become excessive when the inputs are forced below the negative supplies, forward biasing the base tubs.

Offset nulling is accomplished by connecting the balance terminal to a variable voltage derived from the reference output. Both the input-stage current and the reference are tightly regulated over temperature, and the resistance of the adjustment potentiometer can be made very much lower than the resistance looking back into the balance pin. Therefore, offset nulling can produce a minimum-drift condition.

Proceeding through the circuit, the input stage is buffered by vertical PNP followers, Q3 and Q4. This differential signal is converted to single ended by Q5 and Q6 and fed to the base of the second-stage amplifier Q7.

This configuration is not inherently balanced in that the emitter-base voltage of the vertical PNPs is required to match that of the NPNs. As will be seen, the final circuit does include circuitry to correct for the expected variations.

From the collector of Q7, the signal splits, driving separate halves of the complementary Class-B output stage. The NPN output transistor, Q25, is driven through Q13 and Q14. This complementary emitter follower arrangement provides the necessary current gain without requiring the extra bias voltage of a Darlington connection. This is essential in realizing minimum-voltage operation.

Base drive for the NPN output transistor is initially supplied by Q12, but a boost circuit has been added to increase the available drive as a function of load current. This is accomplished with Q24 in conjunction with a current inverter. The inclusion of R23 prevents gross over boosting.

The boost amounts to controlled positive feedback. It does tend to reduce dead zone and linearize gain. Excess boost current is absorbed by Q14, which presents a low enough drive impedance so that the voltage transfer function from its base does not exhibit a negative-gain characteristic. Considerable experience with this and similar boost circuits shows that they do not unfavorably alter frequency response, at least below a few megahertz.

Drive for the PNP half of the output is somewhat more complicated. Again, a compound buffer, Q15 and Q16, is used, although to maintain circuit balance rather than for current gain. The signal proceeds through two inverters, Q17 and Q19, to obtain the correct phase relationship and DC level shift, before it is fed to the PNP output transistor, Q28.

This path has three common-emitter stages; and, potentially, much higher gain than the NPN side. The gain is equalized, however, by the shunting action of Q18-R19 and Q21-R22 as well as negative feedback through Q23.

When the output PNP saturates, Q20 serves to limit its base overdrive with a feedback path to the base of Q17. This is also important to the floating-mode operation of *Figures 2* and *3* in that it disables the PNP drive circuitry when the op amp output is connected to V^+.

The complete schematic of the operational amplifier in *Figure 5* shows the remaining design features. The lower collector on Q1 is outside the normal collector. Its current is quite low until the positive common-mode limit is exceeded, saturating the normal collector of Q1. The auxiliary collector picks up the re-injected current in saturation, which is routed through Q4 to the collector of Q3. When, for example, the amplifier is connected as a follower, this prevents false outputs when the common-mode limit is exceeded. In normal operation, the low-level leakage from the auxiliary collector is evenly divided between the input-stage collectors because the voltage drop across R4 is small.

An extra emitter on Q2 working with Q18 performs a similar function when the negative common-mode limit is exceeded on the inverting input, insuring that the output will be in positive saturation. The non-inverting input is also arranged to give a proper output when the input is driven below V^-.

As mentioned earlier, the optimum collector current of Q13 will depend on the V_{BE} difference between NPN and PNP transistors (Q9-Q10 and Q7-Q13). This is compensated by generating a similar difference current with Q21 and Q22 then processing it with Q19, Q17 and Q15 to generate the required complement in the collector circuit of Q13.

The output stage has been designed to deliver a minimum output current of ± 20 mA with a typical saturation voltage of ± 0.4V. Conventional current limiting cannot be used without significantly increasing the saturation voltage. Since the current gain of lateral PNPs falls off severely at high current and high temperature, it is only necessary to limit the driver current. This is done with R42 and R43, with Q44 insuring that supply current does not become excessive if the BV_{CEO} of Q45 is exceeded on supply transients.

Current limit for the NPN side is done with Q51, Q53 and associated circuitry. In addition, Q49 and Q52 have been added to limit the over boost, should it become larger than can be handled by Q35.

The maximum operating voltage and output current of this device are high enough that current limiting cannot be expected to prevent excessive die temperature, especially with worst-case conditions. Therefore, thermal overload protection has been provided. Die temperature is sensed with Q25, and Q26 introduces hysteresis into the limiting characteristic. The cut out temperature is designed to be 165°C, with operation resuming when the die cools to 155°C. The NPN and PNP halves are shut off by Q27 and Q29, respectively.

Output stage quiescent current is determined by the voltage across R16 and various device geometries. The current is stabilized for varying supply voltage by connecting Q33 in cascode with Q30 and by the addition of Q31 and Q32, which tend to compensate for the collector voltage sensitivity of emitter-base voltage.

At temperatures approaching thermal limit, Q40 must operate beyond the threshold of saturation. The addition of Q39, which is actually a lateral PNP collector ring surrounding the base of Q40, produces a voltage drop across R34 to compensate for the drop across R35 caused by excess base current.

frequency compensation

With feedback amplifiers, the ability to frequency compensate a particular design is generally the bottom line in determining its usefulness. Considering the number of stages involved and the fact that the drive paths for the PNP and NPN output transistors are entirely different, one might rightly conclude that frequency compensation would be difficult.

As much of the frequency compensation network as can be explained in a straightforward manner is shown in the simplified schematic of *Figure 4*. Overall compensation is provided by a MOS capacitor, C2, between the output and the collector of an input transistor. Within this loop, a diffused capacitor, C1, rolls off the gain of Q7, breaking back out where $X_{C1} = R6$.

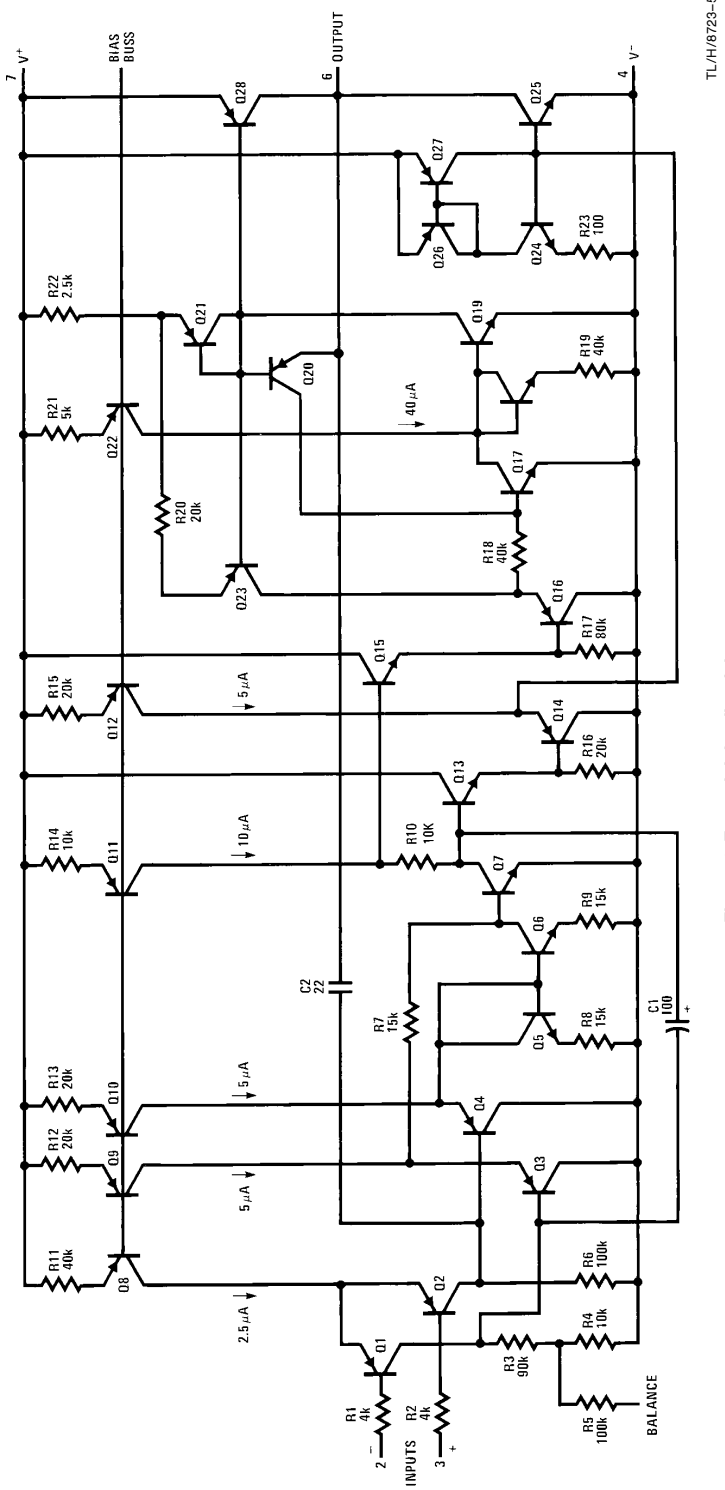

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Figure 4. Essential details of the op amp

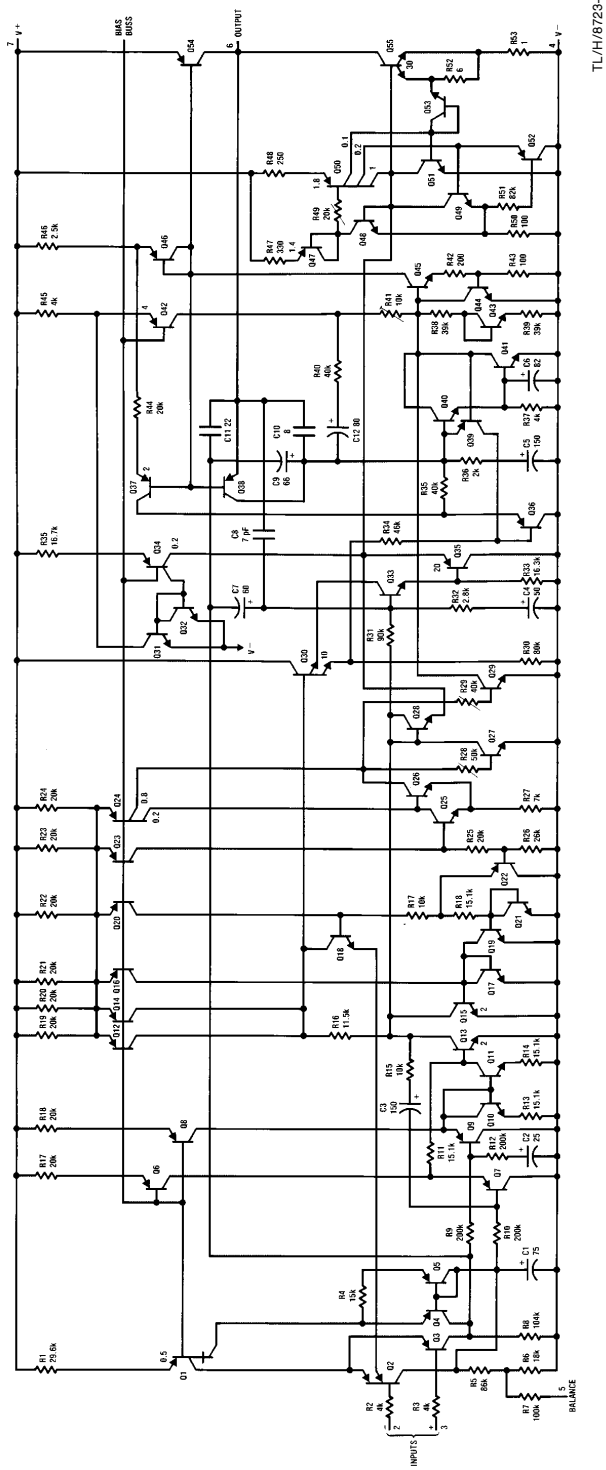

Figure 5. Complete op amp schematic

Referring again to the complete schematic, it can be seen that things are not really that simiple. The function of the feed-forward capacitors, C7 and C9, seems obvious. But remaining compensation components were added as a result of breadboard tests which checked the circuit over temperature with full range of load currents and operating voltages, while varying the resistive and reactive components of load impedance.

A detailed theoretical analysis of the compensation seems overly complicated, considering the number of minor feedback loops involved. This conclusion is supported by the fact that impedance levels in portions of the circuit vary considerably with load current and so does the effect of the frequency-shaping circuits.

Results show the circuit to be stable. For one, no significant differences were found between the breadboard and the IC. This is not overly surprising considering the frequencies involved. Further, varying the sheet resistance of the implant resistors over a 5:1 range showed only that higher resistors made slower amplifiers. Varying NPN current gain over a 4:1 range had little effect on AC characteristics.

Figure 6 is a plot of the open-loop frequency-phase plot of the amplifier. It can be seen that the response does not exactly follow a 6 dB/octave curve. In voltage follower applications, the excess phase shift will cause about 3 dB peaking around 35 kHz. This is of little consequence in that the circuit is not intended for operation above the audio range. What is important is that there are no stability problems for capacitive loads in excess of 1000 pF over the entire operating range of the device. This is illustrated by the plot in *Figure 7*.

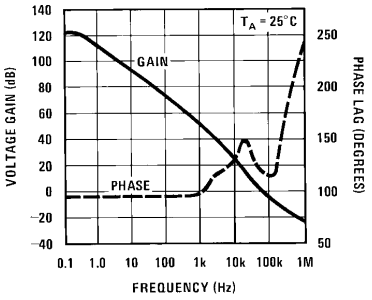

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Figure 6. Open loop frequency response of the op amp

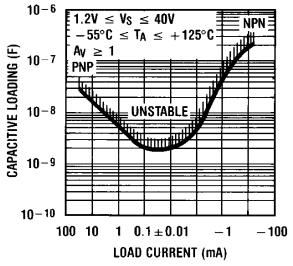

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Figure 7. Plot of capacitive loading required to produce excessive transient ringing in the op amp

A tally of the compensation capacitance for the entire circuit gives a total value of 1000 pF. Nearly all of this is diffused emitter-isolation capacitance (~1 pF/mil^2), and most is diffused into the isolation walls, requiring no extra die area. The reverse bias on diffused capacitors is less than a diode drop, minimizing the effect of soft junctions. This is but one of the advantages of a design where most of the circuit sees only low voltage.

reference and internal regulators

The reference and the internal biasing circuitry are shown in *Figure 8*. The design of the band gap reference[2] (using Q71 and Q72) is unconventional in its configuration and because it compensates for the second-order nonlinearities in the emitter-base voltage as well as those introduced by the temperture drift of the resistors. Thus, the uncompensatable bow in the thermal characteristics of standard devices can be minimized and better temperature stability obtained.

Ignoring the voltage drop across R61 for the moment, the reference voltage developed at the emitter of Q71 is equal to the voltage drop across R62 plus the difference in the emitter-base voltages of Q71 and Q72. The former component is proportional to the emitter-base voltage of Q72 and has a negative temperature coefficient while the latter has a positive temperature coefficient. First order temperature compensation can be obtained by adding these voltages in the proper proportions.

The collector current of Q72 is essentially the output current of the top collector on Q68 less the current through the R62-R64-R66 divider. If the current-source current (Q68) is invariant with temperature and the divider current varies as emitter-base voltage, the collector current of Q72 can be made proportional to absolute temperature. This done, the value of R61 can be set so that the voltage on the collector of Q72 does not change appreciably for small changes in current-source current.

Drift-curvature correction is obtained by maintaining the collector current of Q71 nearly constant while that of Q72 varies directly as temperature. This makes the reference output rise at a rate increasing with temperature. Resistor drift and emitter-base voltage non-linearities have the opposite effect. Near-exact cancellation can be obtained with the proper tap on R64/R66.

The reference amplifier is pretty much a conventional design using a PNP pair (Q66-Q69) for the input, with a NPN current inverter (Q67-Q70) supplying gain and converting to single ended operation. Additional gain is supplied by Q64, and its output is buffered by Q62 and Q56. Frequency rolloff is provided with C12 and R60, with a lead established by feed-forward through C13 and R59.

The quiescent level of the Class-A output stage is set by Q57. The output current is primarily limited by the current gain of Q56. Current limiting is added with Q58, Q61 and R54 to control the short circuit current for supply voltages above BV_{CEO}. This was considered necessary because the thermal limiting does not operate on the reference amplifier.

A clamp, Q59, has been added to insure that the emitter-base junction of Q56 does not break over if the reference output is shorted to V^+.

Precise regulation of the op amp input stage current is required to minimize drift when the recommended offset balancing scheme is used. It also turns out to be of considerable value in normalizing overall operation over the 40:1 range of supply voltage specified for the device.

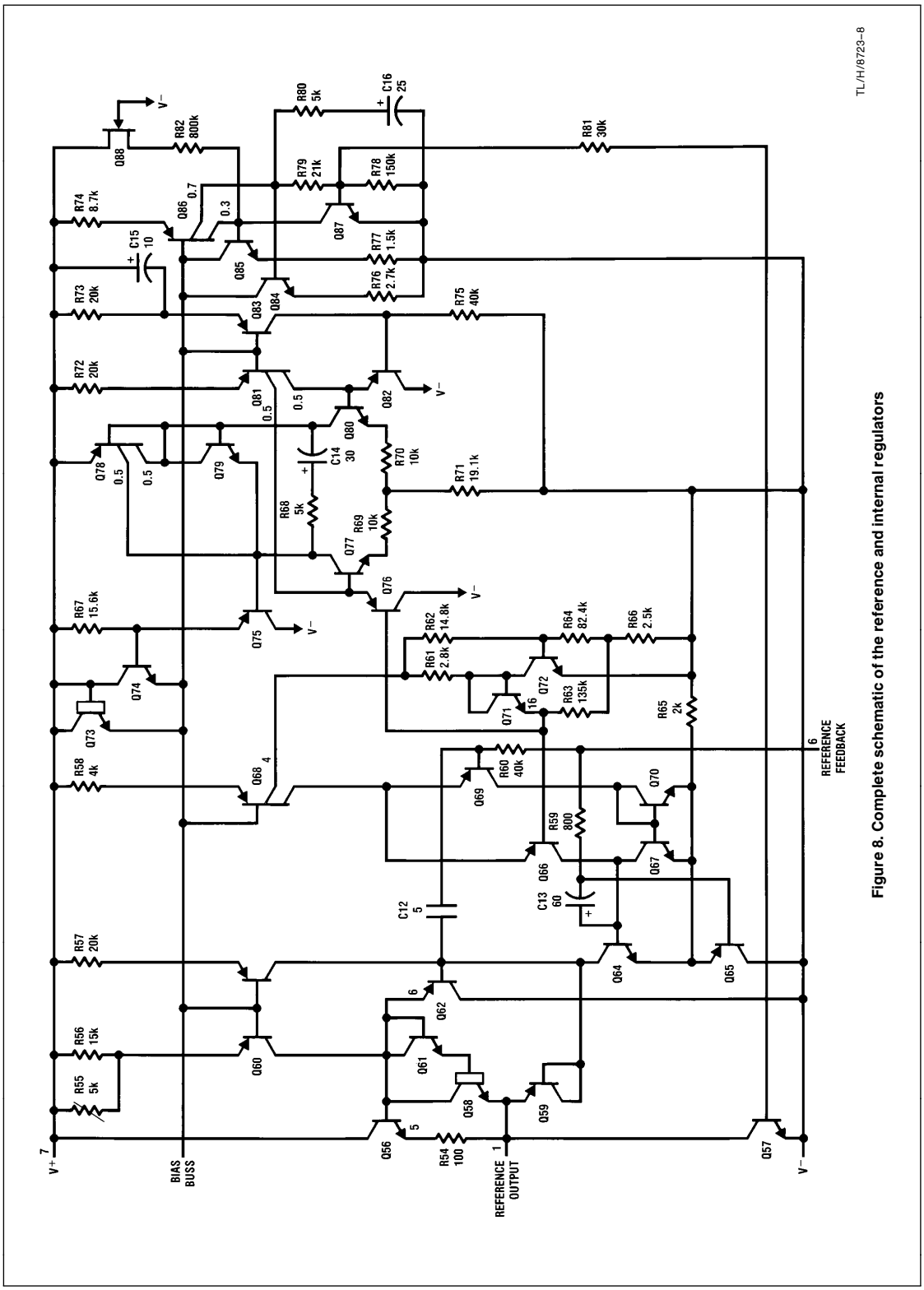

Figure 8. Complete schematic of the reference and internal regulators

Regulation is obtained with another feedback amplifier that maintains the output current of one of the current sources (Q83) at a level where the voltage drop across R75 is equal to the basic reference voltage. The differential input stage (Q77-Q80) is buffered by vertical PNPs (Q76-Q82) more for DC level shift than increased current gain. Q78 serves as a current inverter, delivering a single-ended output to a compound buffer (Q74-Q75) that drives the bias bus. The only unusual feature is Q73. It is a transistor formed using the isolation diffusion as the base. This makes the intrinsic emitter-base voltage more than 100 mV higher than a standard NPN. With this high emitter-base voltage, it can be used as a clamp on the bias bus, limiting peak current-source current under transient conditions.

A high sensitivity start-up circuit is used that will activate on leakage currents alone (Q85-Q86). However, worst-case analysis of any start up based on leakage currents, especially at low temperatures and low voltages, becomes an exercise in the unknown.

To avoid these obscure problems, a collector FET and implant resistor (Q88-R82) have been added to insure reliable operation. Once the circuit is going, Q87 disconnects the start-up circuitry, leaving Q84 to supply current to the bias bus.

performance

The characteristics of the op amp are outlined in Table I. The standard specifications compare favorably with the best of the bipolar ICs available today. The output-voltage swing, output-saturation voltage, output current, common-mode range and supply-voltage range are indeed unusual. These are indicated by the measurement conditions of relevant parameters.

Table I. Typical performance of the operation amplifier at 25°C

Parameter	Conditions	Value
Input Offset Voltage		0.3 mV
Offset Voltage Drift	$-55°C \le T_A \le +125°C$	2 μV/°C
Input Offset Current		0.25 nA
Offset Current Drift	$-55°C \le T_A \le +125°C$	2 pA/°C
Input Bias Current		10 nA
Bias Current Drift	$-55°C \le T_A \le +125°C$	60 pA/°C
Common-Mode Rejection	$V^- \le V_{CM} \le V^+ - 0.85V$	102 dB
Supply-Voltage Rejection	$1.2V \le V_S \le 40V$	96 dB
Unloaded Voltage Gain	$V_S = \pm 20V$, $V_O = \pm 19.97V$, $I_O = 0$	400V/mV
Loaded Voltage Gain	$V_S = \pm 20V$, $V_O = \pm 19.6V$, $R_L = 980\Omega$	130V/mV
Unity-Gain Bandwidth	$1.2V \le V_S \le 40V$	0.2 MHz
Slew Rate	$1.2V \le V_S \le 40V$	0.15V/μs

The typical specifications of the reference are given in Table II. Again it is clear that performance has not been sacrificed to realize low-voltage operation.

Table II. Typical Peformance of the Reference at 25°C

Parameter	Conditions	Value
Line Regulation	$1.2\ V \le V_S \le 40V$	0.001 %/V
Load Regulation	$0 \le I_O \le 1$ mA	0.01%
Feedback Sense Voltage		200 mV
Temperature Drift	$-55°C \le T_A \le +125°C$	0.002%/°C
Feedback Bias Current		20 nA
Amplifier Gain	$0.2V \le V_O \le 75V$	75 V/mV
Total Supply Current	$1.2V \le V_S \le 40V$	270 μA

Minimum operating voltage for the op amp depends on load current and allowable gain error as indicated in *Figure 9*. The typical saturation voltage of the output stage is shown in *Figure 10*. The voltage required to power the reference is plotted in *Figure 11*.

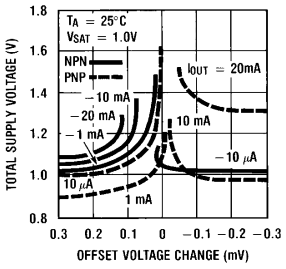

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Figure 9. Plot defining minimum supply voltage for the op amp at various load currents

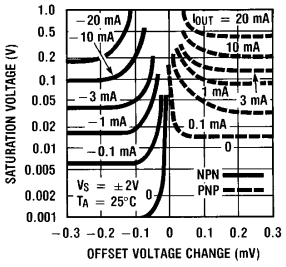

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Figure 10. Saturation characteristics of the op amp

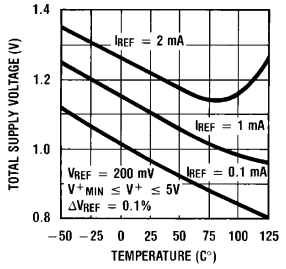

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Figure 11. Minimum supply voltage of the reference as a function of temperature

The total supply current for the complete IC is typically 270 μA. This is impressive only considering the performance and complexity of the circuit. This current might be reduced by a factor of 4, at the expense of speed, by raising the sheet resistance of the implanted resistors.

general

Except for the inclusion of implanted resistors, processing is essentially the same as that developed in 1968 for the LM101A. The high sheet resistivities obtained with implanted resistors strongly recommend them for micropower devices, especially at high levels of complexity. But implanted resistors have a lower breakdown voltage than their diffused counterparts (40V vs 100V). This is caused by the reduced radius of curvature at the junction edges. With higher sheet resistivities, a significant voltage coefficient of resistivity will be observed (resulting in a carrier depletion of about 10^{12} cm^{-2} at the BV_{CEO} of the NPN transistors). These factors recommended that caution be used when operating implant resistors at higher voltages or that they be operated at low voltages where possible. In the circuit under discussion, none of the implant-resistor junctions see the full supply voltage.

A consequence of this low voltage design is that most of the low-level circuitry is operating at junction biases of little more than a diode drop. At this voltage, junctions are not greatly affected by minor defects. Further, in this circuit, most areas that see full supply voltage can tolerate several microamperes of leakage before operation is affected in the least. This can be expected to increase both reliability and manufacturing yield. The overall yield will also be improved because there is a substantial market for devices that will work only at low voltages.

The complete IC is built on a 97 x 105 mil die, shown in *Figure 12*. This is definitely large for an op amp, even when combined with a reference. But with 3-inch wafers and modern processing, die size is not the prime determinant of selling price, as long as reasonable yields are maintained. This is evidenced by the low cost of regulators having equal die area and encapsulated in more expensive power packages.

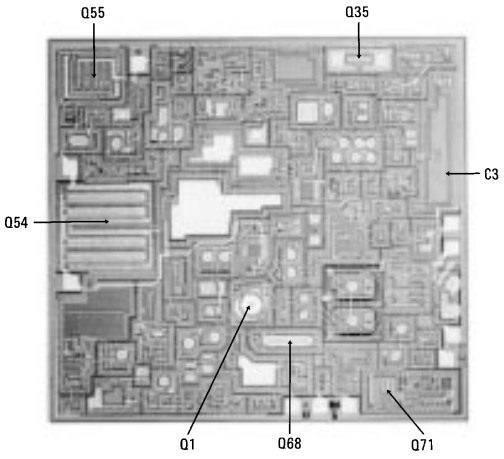

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Figure 12. Photomicrograph of the IC

As can be seen from *Figure 12*, the input-stage current-source, Q1, has been made with about 3 times the base width of the other current-source transistors. This serves both to give it the same emitter-base voltage at roughly half the current density and to make it less sensitive to changes in collector-base voltage. The latter contributes directly to improved common-mode rejection.

To save space, several lateral PNP current-sources have been built with a combination of linear emitter and emitter on a radius. Q68 in *Figure 12* is an example of this. The current density at circular emitters is higher than linear emitters for a given bias voltage. This must be accounted for in design.

As mentioned earlier, operating biases in several places are determined by the difference in the emitter-base voltage between NPN and PNP transistors. Hence, a knowledge of these differences is essential to avoid production problems.

Since the output transistors of the op amp can dissipate considerable power, thermal gradients are potentially a problem. The effects of this dissipation have been measured and the results plotted in *Figure 13*. It is evident that the thermal gradients are well in hand even with 400 mW dissipation. The thermal gradient feed-through into the reference is also plotted in *Figure 14*. Clearly it will be insignificant at the power levels encountered in practical designs. Thermal gradient isolation is primarily the result of careful layout, since many points within the circuit are sensitive. The difficulties are, of course, mitigated by the large die size.

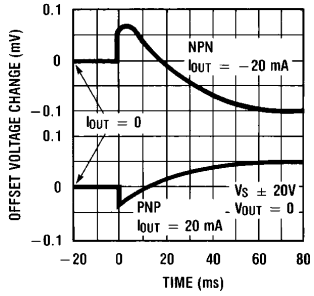

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Figure 13. Effect of a pulsed load on the offset voltage of the op amp showing electrical change and that caused by thermal gradients

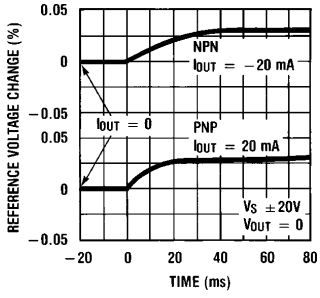

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Figure 14. Cross-coupling from the op amp to the reference caused by thermal gradients

applications

There are many obvious uses for precision functions such as op amps, voltage comparators and voltage references that are capable of operating at low voltages with a small power drain. These include a variety of portable instruments, remote telemetry and even implanted medical devices.

With this battery powered equipment, there is a decided advantage in reducing operating voltage to that of a single cell. The power source will be more simple, less costly and have a higher energy content for a given size and weight. In many respects, current requirements for a given application do not decrease linearly with available supply voltage, giving an even greater advantage to single-cell operation. The resulting increase in the capacity of the power source coupled with the low drain of the electronics could eliminate the need for ON/OFF switches in certain applications.

The control circuits described earlier (*Figures 2* and *3*) that operate from residual voltages independent of fixed supplies suggest an entirely new range of equipment-design possibilities, even with line-operated power supplies. In general, the usefulness of this approach suffers greatly if minimum operating voltage is much above a volt. Low idling current is also an important consideration.

It is difficult to evaluate the impact of these new approaches mainly because they seem to represent a step change in how things can be done at the equipment-design level. But considering that low-voltage operation can be realized with no sacrifice in performance, it would seem that there are few restraints on investigating the new methods.

As a practical matter, the IC described here can also be used in a variety of ordinary applications providing significant performance advantages when compared to existing ICs. Because of this they might be expected to become an ''industry standard''. This is important considering the volume-related economies that strongly influence pricing in the semiconductor business. The general availability of the part can be expected to have a strong influence on the investigation of the new design methods advocated here and elsewhere.[1]

conclusions

It has been shown here that high-performance linear circuits can be designed to operate with little more than a volt of supply voltage. This precludes many standard design methods that require more than two diode drops of bias. Notable among these is the Darlington connection. Alternate techniques can result in a significant increase in complexity. However, this is not a serious problem with modern manufacturing methods, providing that reasonable yield can be maintained.

Although the 270 μA power drain of the example used is not overly impressive in the realm of micropower, it should be remembered that it is a fairly complex function designed for $-55°C$ to $+125°C$ operation and capable of delivering more than 20 mA of output current. A more specialized device could be built with less than a tenth the drain, especially if the maximum operating temperature could be restricted to 85°C. At elevated temperatures and low currents, the emitter-base voltage of a transistor approaches the saturation offset voltage, creating circuit problems.

In general, feedback amplifiers with more complicated signal paths become more difficult to frequency compensate. The benefits to be gained (i.e., saturating outputs and extended common-mode range) are probably justified only in low-voltage circuits. The isolation-wall capacitors introduced here ease the compensation problem some. A typical integrated circuit (LM108) has over 1000 pF of this capacitance available with no area penalty. Nonetheless, stabilizing some designs requires perseverance.

acknowledgement

Special thanks are due to Mineo Yamatake and Bob Dobkin at National Semiconductor Corporation for invaluable assistance in frequency compensating the op amp and other contributions to the final design.

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2. R. J. Widlar, ''New Developments in IC Voltage Regulators'', *IEEE J. of Solid-State Circuits,* Vol. SC-6, No. 1, pp. 2–7, February 1971.

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