LM2593HV

Reducing Converter Stresses

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Reducing Converter Stresses

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Introduction

When designing or testing DC-DC converters with a wide input voltage range, we are invariably concerned with how the stresses in the power supply may change with respect to input/line variations. For example, when conducting stress testing or design validation, one needs to fix an input voltage for the test. But it isn't obvious whether a given stress is going to be the highest at the maximum or at the minimum of the input voltage range. Or worse, somewhere in the middle of the input voltage range!?

Further, designers used to working with one major topology may be quite surprised when they shift attention to another topology, because the rules of the game do in fact change suddenly. In fact the answer to what input voltage represents the 'worst' condition for a given stress, does have a lot to do with the topology at hand. So for example, the peak switch current is higher at low input voltages for the Boost and the Buck-Boost, but quite the opposite for the Buck, for which the worst case is at high input voltages. Further, during the design process too, similar puzzling questions can arise. For example, should the inductor be designed at the highest input or the lowest input voltage of the range? For a Buck it didn't seem to matter too much at what input voltage we design the inductor, but if one applies the same nonchalance to a Boost or a Buck-Boost, there may be no power supply to put through any further testing.

Among the stresses we have obviously ignored are the voltage stresses, as for them it is clear that the worst condition is going to be at the maximum input voltage. Besides, designers can easily figure out the required voltage ratings of the devices used, in any given topology. The same applies to load conditions. It is understood that maximum load is the worst condition, and that is what we need to design for and test. But the important point is even while delivering this constant maximum load, the internal currents of the power supply do change their shape, peak values, RMS and Average values considerably in response to changes in input voltage. The purpose of this article is to figure out how some of these vary and to thereby fix a 'worst case' design or test condition for each of them.

Parameters	Buck	Boost	Buck-Boost
Duty Cycle	$\frac{V_O + V_D}{V_{IN} - V_{SW} + V_D}$	$\frac{V_O - V_{IN} + V_D}{V_O - V_{SW} + V_D}$	$\frac{V_O + V_D}{V_{IN} + V_O - V_{SW} + V_D}$
$V_{IN\ 50}$ *(V)*	$(2 \bullet V_O) + V_{SW} + V_D$ $\approx 2 \bullet V_O$	$\frac{1}{2} \bullet [V_O + V_{SW} + V_D]$ $\approx V_O/2$	$V_O + V_{SW} + V_D$ $\approx V_O$
Output Voltage, V_O *(V)*	$V_{IN} \bullet D - V_{SW} \bullet D - V_D \bullet (1-D)$	$\frac{V_{IN} - V_{SW} \bullet D - V_D \bullet (1-D)}{1-D}$	$\frac{V_{IN} \bullet D - V_{SW} \bullet D - V_D \bullet (1-D)}{1-D}$
Et *(Vμsec)*	$\frac{V_O + V_D}{f} \bullet (1-D) \bullet 10^6$	$\frac{V_O - V_{SW} + V_D}{f} \bullet D \bullet (1-D) \bullet 10^6$	$\frac{V_O + V_D}{f} \bullet (1-D) \bullet 10^6$
L *(μH)*	$\frac{V_O + V_D}{I_O \bullet r \bullet f} \bullet (1-D) \bullet 10^6$	$\frac{V_O - V_{SW} + V_D}{I_O \bullet r \bullet f} \bullet D \bullet (1-D)^2 \bullet 10^6$	$\frac{V_O + V_D}{I_O \bullet r \bullet f} \bullet (1-D)^2 \bullet 10^6$
'r'	$\frac{V_O + V_D}{I_O \bullet L \bullet f} \bullet (1-D) \bullet 10^6$	$\frac{V_O - V_{SW} + V_D}{I_O \bullet L \bullet f} \bullet D \bullet (1-D)^2 \bullet 10^6$	$\frac{V_O + V_D}{I_O \bullet L \bullet f} \bullet (1-D)^2 \bullet 10^6$
ΔI *(A)*	$\frac{V_O + V_D}{L \bullet f} \bullet (1-D) \bullet 10^6$	$\frac{V_O - V_{SW} + V_D}{L \bullet f} \bullet D \bullet (1-D) \bullet 10^6$	$\frac{V_O + V_D}{L \bullet f} \bullet (1-D) \bullet 10^6$
RMS Current in Input Cap *(A)*	$I_O \bullet \sqrt{D \bullet \left[1 - D + \frac{r^2}{12}\right]}$	$\frac{I_O}{1-D} \bullet \frac{r}{\sqrt{12}}$	$\frac{I_O}{1-D} \bullet \sqrt{D \bullet \left[1 - D + \frac{r^2}{12}\right]}$
I_{pp} in Input Capacitor *(A)*	$I_O \bullet \left[1 + \frac{r}{2}\right]$	$\frac{I_O \bullet r}{1-D}$	$\frac{I_O}{1-D} \bullet \left[1 + \frac{r}{2}\right]$
RMS Current in Output Cap *(A)*	$I_O \bullet \frac{r}{\sqrt{12}}$	$I_O \bullet \sqrt{\frac{D + \frac{r^2}{12}}{1-D}}$	$I_O \bullet \sqrt{\frac{D + \frac{r^2}{12}}{1-D}}$
I_{pp} in Output Capacitor *(A)*	$I_O \bullet r$	$\frac{I_O}{1-D} \bullet \left[1 + \frac{r}{2}\right]$	$\frac{I_O}{1-D} \bullet \left[1 + \frac{r}{2}\right]$
Energy Handling Capability *(μJoules)*	$\frac{I_O \bullet Et}{8} \bullet \left[r \bullet \left(\frac{2}{r} + 1\right)^2\right]$	$\frac{I_O \bullet Et}{8 \bullet (1-D)} \bullet \left[r \bullet \left(\frac{2}{r} + 1\right)^2\right]$	$\frac{I_O \bullet Et}{8 \bullet (1-D)} \bullet \left[r \bullet \left(\frac{2}{r} + 1\right)^2\right]$
RMS Current in Inductor *(A)*	$I_O \bullet \sqrt{1 + \frac{r^2}{12}}$	$\frac{I_O}{1-D} \bullet \sqrt{1 + \frac{r^2}{12}}$	$\frac{I_O}{1-D} \bullet \sqrt{1 + \frac{r^2}{12}}$
Average Current in Inductor *(A)*	I_O	$\frac{I_O}{1-D}$	$\frac{I_O}{1-D}$
Peak Current Switch/Diode/ Inductor *(A)*	$I_O \bullet \left[1 + \frac{r}{2}\right]$	$\frac{I_O}{1-D} \bullet \left[1 + \frac{r}{2}\right]$	$\frac{I_O}{1-D} \bullet \left[1 + \frac{r}{2}\right]$

$r = \Delta I / I_{DC}$, Et in Vμsecs, L in μH, f in Hz, All voltages and currents are magnitudes

Table 1a: Design Table with Stresses expressed in terms of Duty Cycle 'D'

A comprehensive table of design information (**Table 1a** in this part and **Table 1b** in the next part of the article to follow) is provided for all the three main topologies: the Buck, the Buck-Boost and the Boost. We are considering a power supply of any of these topologies, operating at constant (maximum) load, with a fixed output voltage, whose input voltage is varied. We predict the response of a given parameter to the resulting variation in duty cycle, and

thereby figure out the worst case input test or design condition. These conclusions will be summarized in Part 2 of this article which follows. The equations are essentially cast in terms of the output voltage (V_O), max load ('I_O') and Duty Cycle ('D'), and inductor current ripple ratio ('r'). The input voltage 'V_{IN}' is not included directly in the stress formulae, as 'D' is intended to reflect the input voltage variation. The most important fact to keep in mind in this article when relating D to V_{IN} is that for all topologies, low D corresponds to high V_{IN} and a high D to low V_{IN} (since output voltage is considered fixed). It will also be noticed that the design table includes the drops across the Switch ('V_{SW}') and diode ('V_D') for all the topologies. It was figured that since these 'drops' have become increasingly important with the present day situation of ever-decreasing input/output voltage rails, it doesn't make sense anymore to approximate them to zero as is often done in related literature. So the table, being a fairly complete and accurate reference source of useful design information, was also used to make some important design related conclusions along the way.

In Part 1 of this article we will present the equations for inductor and capacitors. In Part 2 we will take up the semiconductors, and also plot out the functions referred to in both articles and summarize them in an easy lookup table.

Inductor Current Waveforms

An inductor current waveform consists of an AC/ramp component 'ΔI', and a DC/average component 'I_{DC}', the latter being the geometric center of the ramp. For the Buck, the average inductor current is the load current, but for the Boost and the Buck-Boost, the average diode current is the load current. So as from **Table 1a**, it can be shown that

$I_{DC} = I_O = \text{constant}$ BUCK

$I_{DC} = \frac{I_O}{1-D} \propto \frac{1}{1-D}$ BOOST/BUCK-BOOST

So it is clear that the average Inductor current becomes very high if D approaches 1 for the Boost and the Buck-Boost. This corresponds to the lowest input voltage 'V_{IN_MIN}' for these topologies, and the inductor design must be conducted at this voltage. But for the Buck there is hardly any relationship of inductor design to input voltage since the average current depends only on the load (which is considered fixed in our analysis). So for a Buck regulator, as a first pass selection, we often simply pick an inductor with a current rating equal to the load.

The AC component of the inductor current, 'I_{AC}', or 'ΔI' cannot be fully ignored even for a Buck. This parameter is important, firstly, because alongwith I_{DC}, it determines the peak value of the inductor current. This peak value needs to be known so as to accurately evaluate the energy handling requirement of the inductor (defined as $½*L*I^2_{PEAK}$). If we do not size the inductor accordingly, the core may saturate. But more importantly, for all topologies, this AC component is completely responsible for the core loss (which does not depend on I_{DC}, so long as the inductor is not saturating).

Now, for all the topologies, there is an applied voltage 'V_{ON}' applied across the inductor when the switch is ON. This causes a certain AC ramp component 'ΔI' across the inductor from the basic equation $V_{ON}=L*\Delta I/(D/f)$ or $\Delta I=V_{ON}*D/(L*f)$, where f is the frequency. As the input voltage falls, VON also decreases, but D increases. So what happens to ΔI?

The term ΔI is provided in **Table 1a**. We see that

$\Delta I \propto (1-D)$ BUCK/BUCK-BOOST

$\Delta I \propto D \bullet (1-D)$ BOOST

Plotting these functions out we will see that

$\Delta I \Rightarrow$ maximum at highest input voltage for Buck/Buck-Boost

$\Delta I \Rightarrow$ maximum at V_{IN_50} (or closest voltage) for Boost

where V_{IN_50} is the input voltage at which D=50% for the topology under consideration. The equation for V_{IN_50} is also provided in **Table 1a**. If the input voltage range does not include V_{IN_50}, we must choose either V_{IN_MIN} or V_{IN_MAX}, whichever happens to be closer to V_{IN_50}.

We also define a useful parameter called the current ripple ratio 'r' which is the ratio of the AC to the DC value of the inductor current, with the converter delivering maximum load. So

$$r = \frac{\Delta I}{I_{DC}} = \frac{\Delta I}{I_O} \quad \text{BUCK}$$

$$r = \frac{\Delta I}{I_{DC}} = \frac{\Delta I}{I_O} \bullet (1-D) \quad \text{BOOST/BUCK-BOOST}$$

This parameter 'r' is important as it determines among other things, the inductance 'L', and the physical size of most of the power components. It can be shown that the size of the inductor is reduced by increasing 'r'. However an 'r' of 0.3-0.4 represents the most optimum choice for any topology. Allowing greater current ripple than this does not appreciably reduce the size of the inductor, but increases the size of the input/output capacitors. Now, having designed the inductor for a given value of 'r' at the appropriate input voltage end, as discussed earlier, as we vary the input voltage over the expected range, 'r' changes accordingly. The equations in **Table 1a** are cast essentially in terms of 'r' and D, as these are the two main parameters that vary with input voltage. The variation of 'r' with D is also provided, thus making D the only actual variable in our analysis . The value of the required inductance (based on a chosen 'r') can be found in **Table 1a**, and the physical size of this inductor can be also calculated from the required energy handling capability as listed.

Inductor Energy

The 'Energy Handling Capability' is $e=½* L*I^2_{PEAK}$. This parameter literally 'sizes' up the inductor for a given application. Note that the size is not determined just by inductance, since almost any inductance can be theoretically achieved on any core, simply by winding the appropriate number of turns on it. The complete equations for 'e' are provided in **Table 1a**. For our analysis here, we first make an approximation for the rather complicated term involving 'r'. Assuming 'r' to be small this term becomes

$$r \bullet \left[\frac{2}{r}+1\right]^2 \approx r \bullet \left[\frac{2}{r}\right]^2 \propto \frac{1}{r}$$

From **Table 1a**, for small 'r', we can see that the Energy handling Capability goes as

$$e \propto \frac{Et}{r} \propto \frac{(1-D)}{(1-D)} = 1 \quad \text{BUCK}$$

$$e \propto \frac{Et}{(1-D) \bullet r} \propto \frac{D \bullet (1-D)}{D \bullet (1-D)^3} \propto \frac{1}{(1-D)^2} \quad \text{BOOST}$$

$$e \propto \frac{Et}{(1-D) \bullet r} \propto \frac{(1-D)}{(1-D)^3} \propto \frac{1}{(1-D)^2} \quad \text{BUCK-BOOST}$$

Plotting these functions out we will see that

$_e \Rightarrow$ constant/maximum at highest input voltage for Buck
$_e \Rightarrow$ maximum at lowest input voltage for Boost/Buck-Boost

Note that for both the Boost and the Buck-Boost, the required energy handling capability increases dramatically as duty cycle approaches 0.6. This is known to designers of front-end PFC stages. Such stages are typically of Boost topology, providing an internal 400VDC rail from a worldwide AC input. It is seen that the size of the required inductor goes up sharply as the minimum input voltage falls, and so the inductor design should be carried out at the minimum input voltage. As for the Buck, some designers use the maximum input voltage, some the minimum, and some simply use the nominal input voltage. It really does not matter too much, provided 'r' is, and remains, small as we assumed. In reality, 'r' does increase as input voltage increases (thereby causing a slight increase in peak value), so it is preferable to design the inductor of a buck regulator for the highest input voltage.

Inductor Avg/RMS Currents

If 'r' is small, the average and RMS values of the inductor current are the same, 'I_L'. The copper loss in the inductor is I_L^2*R, where 'R' is the winding resistance. The copper loss is usually very large compared to the core loss (which depends on ΔI, as discussed earlier), and largely determines the temperature rise of the inductor.

From **Table 1a**, for small 'r', we can see that the RMS/Avg current goes as

$I_L \propto constant$ BUCK

$I_L \propto \frac{1}{(1-D)}$ BOOST/BUCK-BOOST

We can see that for the Boost and Buck-Boost, if D is large, I_L increases. Therefore when evaluating copper loss or temperature rise of the inductor for these, we need to use the minimum input voltage. For the Buck, since 'r' does increase with increasing input voltage, the RMS value of the inductor current is also higher, and so we should use the maximum input voltage.

$I_L \Rightarrow$ constant/maximum at highest input voltage for Buck
$I_L \Rightarrow$ maximum at lowest input voltage for Boost/Buck-Boost

Input Capacitor Currents

A key parameter is the RMS current ,'I_{IN}', through the input electrolytic capacitor. It determines the basic/minimum selection criterion since the capacitor must be rated at least for the worst case RMS current that may pass through it. A capacitor operated with an RMS current higher than its rated value, is not guaranteed to have any specific life by most manufacturers. Life expectancy vs. temperature curves/equations as provided, are then not considered to be valid.

From **Table 1a**, for small 'r', we can see that this goes as

$I_{IN} \propto \sqrt{D \bullet (1-D)}$ BUCK

$I_{IN} \propto \frac{r}{1-D} \propto \frac{D \bullet (1-D)^2}{1-D} = D \bullet (1-D)$ BOOST

$I_{IN} \propto \frac{1}{(1-D)} \bullet \sqrt{D \bullet (1-D)} = \sqrt{\frac{D}{1-D}}$ BUCK-BOOST

Plotting these functions out we will see that

$I_{IN} \Rightarrow$ maximum at V_{IN_50} (or closest voltage) for Buck/Boost

$I_{IN} \Rightarrow$ maximum at lowest input voltage for Buck-Boost

So the temperature of the output capacitor must also be evaluated at the above input voltages. If the input voltage range does not include V_{IN_50}, we must choose either V_{IN_MIN} or V_{IN_MAX}, whichever happens to be closer to V_{IN_50}.

We are also concerned with the peak to peak current, I_{PP_IN} through the input capacitor as this determines the input voltage ripple $DV_{IN}=I_{PP\_IN}*ESR_{IN}$, where ESR_{IN} is the Equivalent Series Resistance of the input capacitor. This input ripple is a major component of the EMI spectrum at the input of the power supply.

From **Table 1a**, for small 'r', we can see that this goes as

$I_{PP\_IN} \propto \text{constant}$ BUCK

$I_{PP\_IN} \propto \frac{r}{1-D} \propto \frac{(1-D)^2}{1-D} = (1-D)$ BOOST

$I_{PP\_IN} \propto \frac{1}{1-D}$ BUCK-BOOST

Plotting these functions out we will see that

$I_{PP\_IN} \Rightarrow$ constant/maximum at highest input voltage for Buck

$I_{PP\_IN} \Rightarrow$ maximum at highest input voltage for Boost

$I_{PP\_IN} \Rightarrow$ maximum at lowest input voltage for Buck-Boost

For a Buck stage, the input voltage ripple is almost a constant with respect to input voltage variations, provided 'r' is very small. However since 'r' does increase somewhat at high input voltages, it is preferable to evaluate this parameter at the highest input voltage.

Output Capacitor Currents

The Output Capacitor also needs to be at least big enough to handle the worst case RMS current through it, 'I_{OUT}'.

From **Table 1a**, for small 'r', we can see that this goes as

$I_{OUT} \propto r \propto (1-D)$ BUCK

$I_{OUT} \propto \sqrt{\frac{D}{1-D}}$ BOOST/BUCK-BOOST

Plotting these functions out we will see that

$I_{OUT} \Rightarrow$ maximum at highest input voltage for Buck

$I_{OUT} \Rightarrow$ maximum at lowest input voltage for Boost/Buck-Boost

So the temperature of the output capacitor must also be evaluated at the above input voltages.

We are also concerned with the peak to peak current, I_{PP_OUT} through the output capacitor as this determines the

output voltage ripple $DV_{OUT}=I_{PP\_OUT}*ESR_{OUT}$, where ESR_{OUT} is the Equivalent Series Resistance of the output capacitor. This output ripple is a major component of the noise spectrum at the output of the power supply.

From **Table 1a**, for small 'r', we can see that this goes as

$I_{PP\_OUT} \propto r \propto (1-D)$ BUCK

$I_{PP\_OUT} \propto \frac{1}{1-D}$ BOOST/BUCK-BOOST

Plotting these functions out we will see that

$I_{PP\_OUT} \Rightarrow$ maximum at highest input voltage for Buck

$I_{PP\_OUT} \Rightarrow$ maximum at lowest input voltage for Boost/Buck-Boost

Switch RMS/Avg Current

For a MOSFET Switch we need to calculate the conduction loss as given by $I^2_{RMS}*rds$. The crossover losses are lowest at the minimum input voltage. But since they are usually a small fraction of the conduction losses, and are thus ignored here. The I_{RMS} of the switch varies in the following manner

Parameters	Buck	Boost	Buck-Boost
Duty Cycle	$\frac{V_O+V_D}{V_{IN}-V_{SW}+V_D}$	$\frac{V_O-V_{IN}+V_D}{V_O-V_{SW}+V_D}$	$\frac{V_O+V_D}{V_{IN}+V_O-V_{SW}+V_D}$
Output Voltage, V_O *(V)*	$V_{IN}\bullet D-V_{SW}\bullet D-V_D\bullet(1-D)$	$\frac{V_{IN}-V_{SW}\bullet D-V_D\bullet(1-D)}{1-D}$	$\frac{V_{IN}\bullet D-V_{SW}\bullet D-V_D\bullet(1-D)}{1-D}$
'r'	$\frac{V_O+V_D}{I_O\bullet L\bullet f}\bullet(1-D)\bullet 10^6$	$\frac{V_O-V_{SW}+V_D}{I_O\bullet L\bullet f}\bullet D\bullet(1-D)^2\bullet 10^6$	$\frac{V_O+V_D}{I_O\bullet L\bullet f}\bullet(1-D)^2\bullet 10^6$
RMS Current in Switch *(A)*	$I_O\bullet\sqrt{D\bullet\left[1+\frac{r^2}{12}\right]}$	$\frac{I_O}{1-D}\bullet\sqrt{D\bullet\left[1+\frac{r^2}{12}\right]}$	$\frac{I_O}{1-D}\bullet\sqrt{D\bullet\left[1+\frac{r^2}{12}\right]}$
Peak Current Switch/Diode/ Inductor *(A)*	$I_O\bullet\left[1+\frac{r}{2}\right]$	$\frac{I_O}{1-D}\bullet\left[1+\frac{r}{2}\right]$	$\frac{I_O}{1-D}\bullet\left[1+\frac{r}{2}\right]$
Average Current in Switch *(A)*	$I_O\bullet D$	$I_O\bullet\frac{D}{1-D}$	$I_O\bullet\frac{D}{1-D}$
Average Current in Diode *(A)*	$I_O\bullet(1-D)$	I_O	I_O

$r=\Delta I/I_{DC}$, L in µH, f in Hz, All voltages and currents are magnitudes

Table 1b: Design Table with Stresses expressed in terms of Duty Cycle 'D'

From **Table 1b**, for small 'r', we can see that this goes as

$I_{RMS} \propto \sqrt{D}$ BUCK

$I_{RMS} \propto \frac{\sqrt{D}}{1-D}$ BOOST/BUCK-BOOST

Plotting these functions out we will see that

$I_{RMS} \Rightarrow$ **maximum at lowest input voltage for Buck/Boost/Buck-Boost**

It should however be noted that for a Buck, the dissipation in the Switch at low input voltages goes up only slightly, but for the remaining topologies, this dissipation is expected to go up steeply at low input voltages, leading to a large drop in efficiency. In **Table 1b**, the average switch current is also provided, for calculation of dissipation in bipolar switches. It can be shown that the above conclusions for RMS are also valid for the average value of the switch current (which is required to calculate the conduction loss for a bipolar switch).

Talking about efficiency leads to the other main component of loss in a power supply, the diode loss. We will now see how this varies, and what it implies for the effect of input variations on the efficiency of the power supply.

Average Diode Current/Efficiency

For a diode we need to calculate the forward loss as given by $I_{AVG}*V_D$, where 'V_D' is the drop across the diode when it conducts. For the Boost and the Buck-Boost, the average diode current is the load current, so it is not going to change with duty cycle. But for the Buck it does vary.

From **Table 1b**, we can see that this goes as

$I_{AVG} \propto (1-D)$ **BUCK**

$I_{AVG} \propto constant$ **BOOST/BUCK-BOOST**

Plotting these out in **Figure 1**, we can see that

$I_{AVG} \Rightarrow$ **maximum at highest input voltage for Buck**
$I_{AVG} \Rightarrow$ **constant for Boost/Buck-Boost**

We saw that the dissipation in the switch of a Buck remains almost constant as input voltage increases, but now we see that the diode dissipation increases as we do so. So we expect the efficiency of a Buck regulator to fall at high input voltages on account of increased diode dissipation (assuming the drop across switch is less than the drop across the diode). For the Boost and Buck-Boost, the diode dissipation does not change as input voltage falls, but the switch dissipation increases dramatically. So we expect the efficiency of a Boost or a Buck-Boost to fall at low input voltages on account of increased switch dissipation (unless crossover losses are very large, in which case the reverse is occasionally found to be true).

Parameters	Buck	Boost	Buck-Boost
ΔI (I_{AC} in Inductor)	$V_{IN\ MAX}$ 12	$V_{IN\ 50}$ 11	$V_{IN\ MAX}$ 12
Core Loss	$V_{IN\ MAX}$	$V_{IN\ 50}$	$V_{IN\ MAX}$
Inductor Energy/ Core Saturation	$V_{IN\ MAX}$/ V_{IN} 8	$V_{IN\ MIN}$ 1	$V_{IN\ MIN}$ 1
Average Current in Inductor	V_{IN} 8	$V_{IN\ MIN}$ 3	$V_{IN\ MIN}$ 3
RMS Current in Inductor	$V_{IN\ MAX}$/ V_{IN} 8	$V_{IN\ MIN}$ 3	$V_{IN\ MIN}$ 3
Copper Loss/Temperature of Inductor	$V_{IN\ MAX}$/ V_{IN}	$V_{IN\ MIN}$	$V_{IN\ MIN}$
RMS Current in Input Capacitor	$V_{IN\ 50}$ 10	$V_{IN\ 50}$ 11	$V_{IN\ MIN}$ 6
Input Voltage Ripple	$V_{IN\ MAX}$/V_{IN} 8	$V_{IN\ MAX}$ 12	$V_{IN\ MIN}$ 3
RMS Current in Output Capacitor	$V_{IN\ MAX}$ 12	$V_{IN\ MIN}$ 6	$V_{IN\ MIN}$ 6
Output Voltage Ripple	$V_{IN\ MAX}$ 12	$V_{IN\ MIN}$ 3	$V_{IN\ MIN}$ 3
RMS Current in Switch	$V_{IN\ MIN}$ 7	$V_{IN\ MIN}$ 2	$V_{IN\ MIN}$ 2
Average Current in Switch	$V_{IN\ MIN}$	$V_{IN\ MIN}$	$V_{IN\ MIN}$
Peak Current in Switch/Diode/Inductor	$V_{IN\ MAX}$ 9	$V_{IN\ MIN}$ 4	$V_{IN\ MIN}$ 5
Average Current in Diode	$V_{IN\ MAX}$ 12	V_{IN} 8	V_{IN} 8
Temperature of Diode	$V_{IN\ MAX}$ 12	V_{IN} 8	V_{IN} 8
Worst case Efficiency	$V_{IN\ MAX}$	$V_{IN\ MIN}$	$V_{IN\ MIN}$

Numbers in the columns refer to corresponding numbered curves in Figure 1
V_{IN} means any input voltage is appropriate
V_{IN_50} is input voltage at which D=0.5

Table 2: The worst input voltage condition for design/test of a given parameter

For diode temperatures, we need to test a Buck regulator at the highest input voltage. For the other topologies, it does not matter. This is shown as 'V_{IN}' in **Table 2**, implying any input voltage.

Peak Switch Current

This parameter is important because every controller has a current limit for the switch, and if the calculated peak exceeds the lowest value possible of the switch current limit, anywhere in the input voltage range, the required output power cannot be delivered. The peak current in a Buck is just a little higher than the load current, and so for example, the LM2593HV 'Step Down (Buck) regulator' IC from National Semiconductor, which is designed for '2A load', has a minimum set value of 2.3A for the switch current limit. Yet, as seen in **Figure 2**, and from the datasheet of this device, this Buck IC can be operated as a 'positive to negative' regulator, which is actually a standard Buck-Boost topology. In this mode, the peak current values are much higher, as can be seen from **Table 1b**, and in fact depend not only on load, but on the duty cycle/input voltage too. We now try to see how the peak current values vary for all the topologies, with changes in input voltage.

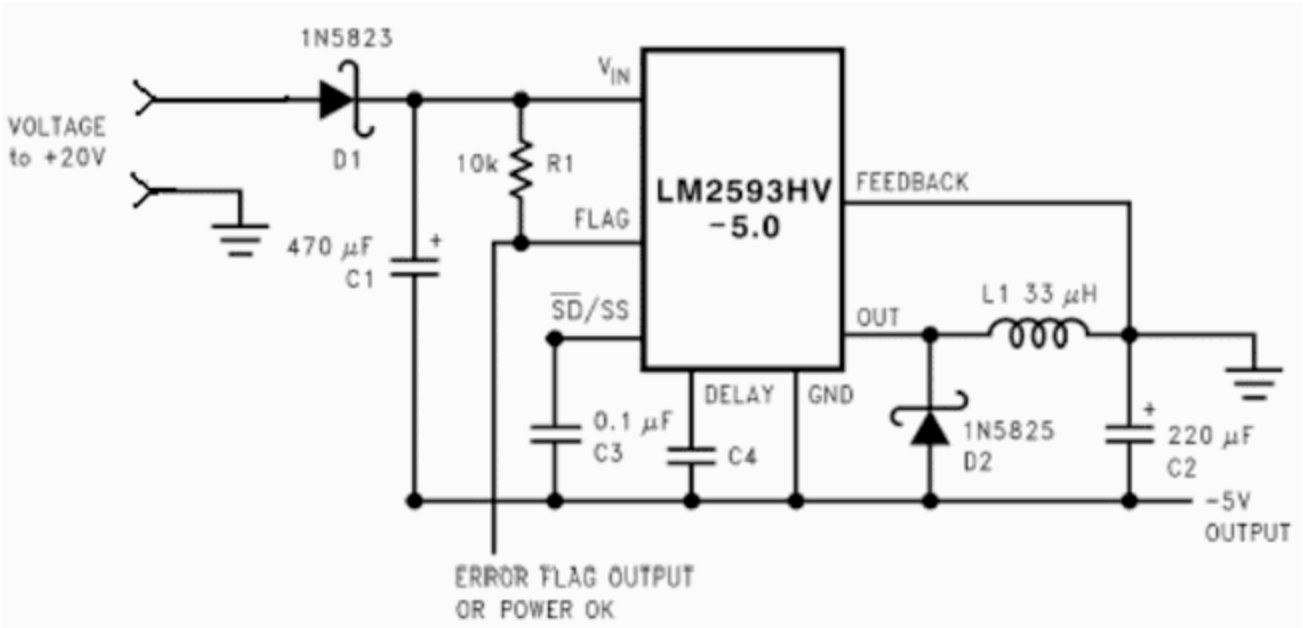


Figure 2: Buck Regulator IC used in a Buck-Boost Application

From **Table 1b**, for small 'r', we can see that the peak current goes as

$$I_{PEAK} \propto \left[1+\frac{r}{2}\right] \propto \left[2+(1-D)\right] = (3-D)$$ BUCK

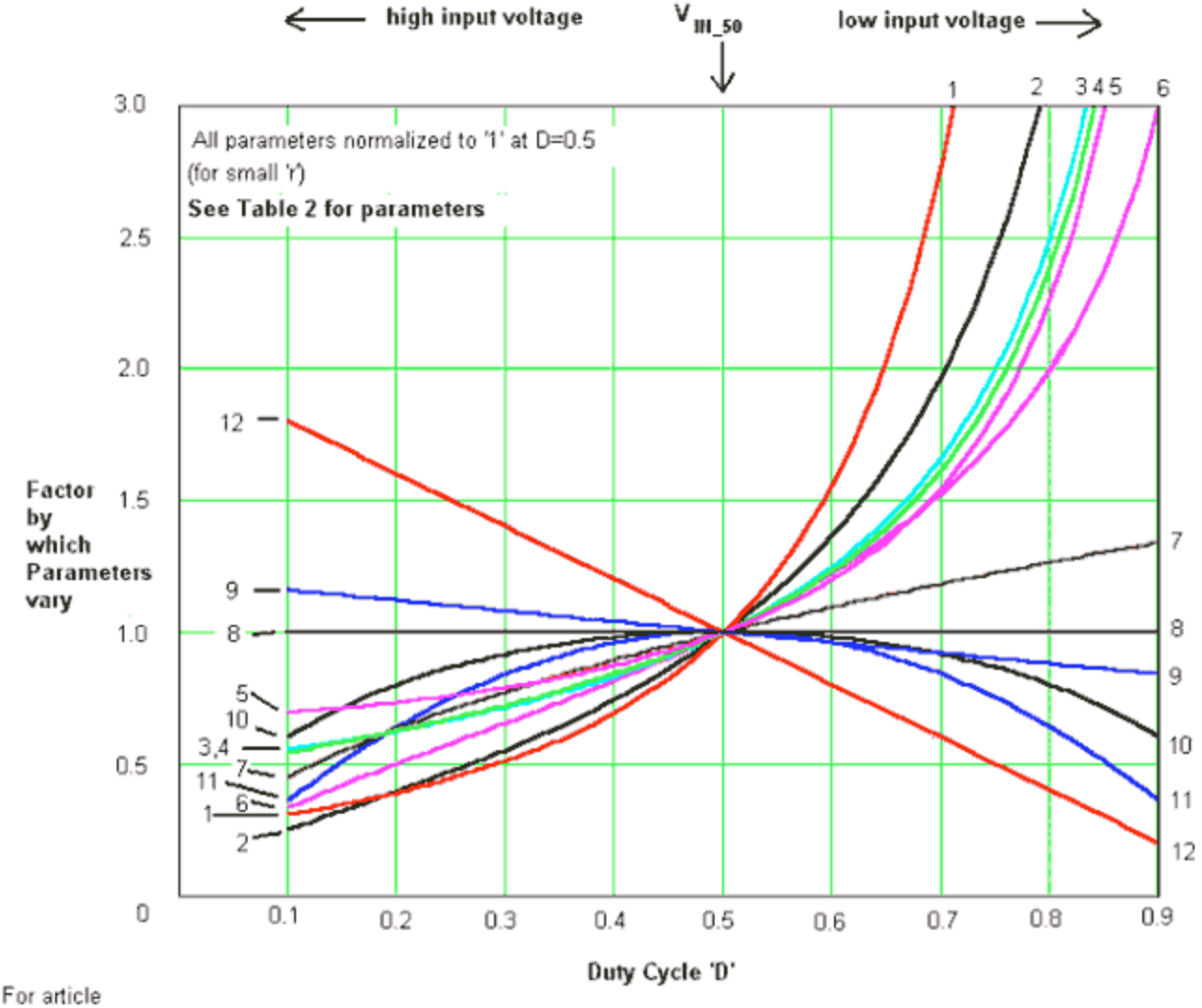
$$I_{PEAK} \propto \frac{\left[1+\frac{r}{2}\right]}{1-D} \propto \frac{\left[2+(D\bullet(1-D)^2)\right]}{1-D}$$ BOOST

$$I_{PEAK} \propto \frac{\left[1+\frac{r}{2}\right]}{1-D} \propto \frac{\left[2+(1-D)^2\right]}{1-D}$$ BUCK-BOOST

Plotting these functions we will see that for the Boost and the Buck-Boost the peak value of switch current occurs at maximum duty cycle (minimum input voltage), whereas for the Buck this occurs at lowest duty cycle (highest input voltage). Therefore Current Limit must be tested at minimum input voltage for the Boost and the Buck-Boost, but for the Buck we must go to the highest input voltage. We conclude

$I_{PEAK} \Rightarrow$ maximum at highest input voltage for Buck
$I_{PEAK} \Rightarrow$ maximum at lowest input voltage for Boost/Buck-Boost

This tells us for example, that the designer can always use **Table 1b** to calculate the peak current, but for the worst case, he must do so at the lowest input voltage for the Boost and Buck-Boost, to ensure that the calculated peak is less than the current limit. For a Buck, the peak current must be calculated and compared to the current limit at the highest input voltage.



For article
"Stresses in wide input DC-DC ..etc"

FIGURE 1

Plotting the variations

In both Parts of this article we presented the proportion by which each of the parameters varied with respect to duty cycle (and input). These functions are called the variation functions here and to get a clearer idea of the shape and extent of the variation, we have plotted these out in **Figure 1**. They are all normalized to unity at D=0.5, which serves as a reference point. The results are summarized in **Table 2**. For example, considering the inductor energy, we can see from **Table 2** that the curve we need to refer to is #1 for Boost and Buck-Boost, whereas it is #8 for the Buck. From **Figure 1**, we go to curve #1 and we can see how steeply the inductor energy goes up as D increases (low input voltage). On the other hand, curve #8 for the Buck shows what we stated earlier, that it hardly matters at what input voltage we design the inductor.

Example:

The LM2593HV (5V fixed output version) is to be used to generate a -5V output from an input voltage

ranging from 4.5V to 20V. This is a 150kHz Buck Regulator IC with a switch current limit of 2.3A (min). What is the maximum load it can deliver in this positive to negative configuration. (Assume V_D=0.5V and V_{SW}=1.5V).

The inductor design must be done at the minimum input i.e. 4.5V for a Buck-Boost topology according to the guidelines in **Table 2**. We fix an 'r' of 0.3 as this always represents an optimum size for the inductor. The duty cycle is calculated from the equation in **Table 1a** or **1b**.

$$D = \frac{V_O + V_D}{V_{IN} + V_O - V_{SW} + V_D} = \frac{5+0.5}{4.5+5-1.5+0.5}$$

$$D = 0.65$$

The peak current in the switch is

$$I_{PEAK} = \frac{I_O}{1-D} \bullet \left[1 + \frac{r}{2}\right]$$

So setting I_{PEAK}=2.3A, we can solve for I_O

$$I_O = \frac{I_{PEAK} \bullet (1-D)}{\left(1+\frac{r}{2}\right)} = \frac{2.3 \bullet (1-0.65)}{\left(1+\frac{0.3}{2}\right)}$$

$$I_O = 0.7 \ \text{A}$$

Therefore we can assure ourselves of only a maximum load of 0.7A in this configuration. The required L can be evaluated from **Table 1a** where we presented the following equation

$$L = \frac{V_O + V_D}{I_O \bullet r \bullet f} \bullet (1-D)^2 \bullet 10^6 \ \mu\text{H}$$

$$L = \frac{5+0.5}{0.7 \bullet 0.3 \bullet 150000} \bullet (1-0.65)^2 \bullet 10^6 \ \mu\text{H}$$

$$L = 21.4 \ \mu\text{H}$$

This is the minimum inductance for the application. If the inductance is higher than this, the calculated peak current may exceed the current limit of the device, causing foldback. Remaining parameters/ratings can be calculated in a similar way, by looking at **Table 1a** and **Table 1b**, while referring to the guidelines in **Table 2**.

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