Application Note

Basic Calculation of a Coupled Inductor SEPIC Power Stage

Elisabetta Mahmutovic

ABSTRACT

This report focuses on designing the power stage for a SEPIC converter. The design procedure is generic on selecting suitable components of the SEPIC power stage for the given application specifications. The LM5155EVM-SEPIC evaluation module is used as the example to illustrate the design procedure, and the circuit performance results are also presented in the *LM5155EVM-SEPIC User's Guide*. For typical applications the *LM5155 and LM5156 Quickstart Calculator for SEPIC Regulator Design (Rev. A)* can also be used to efficiently complete the calculations described in this report.

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Trademarks

1 Introduction

The typical design procedures and calculations to implement a non-synchronous SEPIC power stage operating in continuous conduction mode are presented in this report. The converter in this example is based on the LM5155EVM-SEPIC and can provide a regulated output of 12 V at 1 A from an input of 4 V to 32 V. When the input voltage is between 4 V to 6 V, the output power is derated down to 6 W.

The Figure 1-1 shows the basic configuration of a SEPIC power stage.

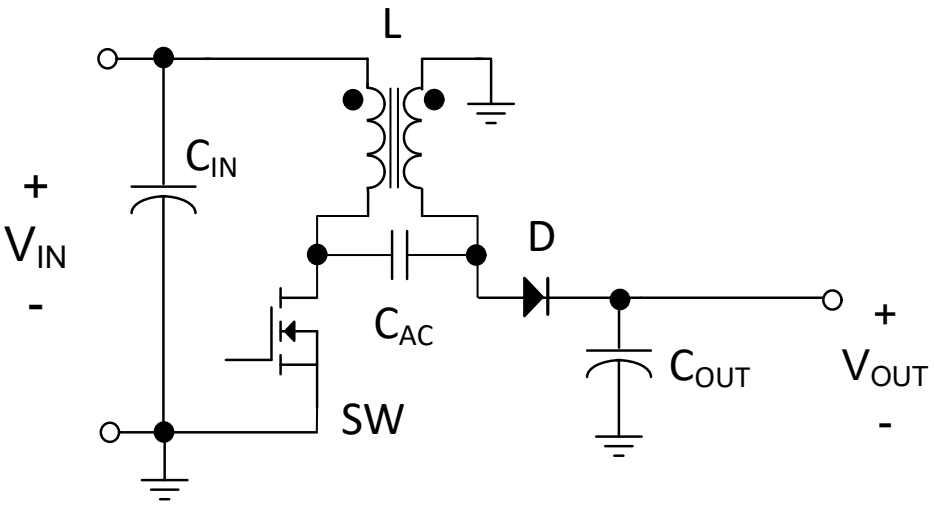

Figure 1-1. Coupled Inductor SEPIC Power Stage

2 Application Parameters

The following parameters are needed to calculate the SEPIC power stage:

- Input voltage range
- Nominal output voltage
- Maximum output current
- Maximum output power
- Desired switching frequency
- Converter IC

Table 2-1 shows the specification for the example application.

Table 2-1. Application Specification

Parameter	
V_{IN}	4 V to 32 V
V_{LOAD}	12 V
I_{LOAD}	1 A
$P_{OUT, max}$	12 W
f_{SW}	2.1 MHz

3 Calculations and Component Selection

This section covers the equations for the selections of the external components with respect to the application specification given in Table 2-1.

Figure 4-1 shows the SEPIC converter topology implemented with the LM5155 to produce a regulated voltage rail as specified in Table 2-1.

3.1 Switching Frequency

Selecting the switching frequency is the first step in the design process. Higher switching frequencies (for example, around 1.8 MHz) yield a smaller total solution size. However, the small size comes at the cost of increased switching losses, decreasing the efficiency of the converter. Higher efficiency is achieved by selecting a relatively lower switching frequency (for example, around 440 kHz) but requires physically larger components. Harmonics of the switching frequency must be considered in designs that have strict EMC requirements. The example application is selected to have a switching frequency of 2.1 MHz.

The LM5155x/LM5156x has a maximum duty cycle limit that is frequency dependent. See the *LM5155x/LM5156x* data sheet for details on the maximum duty cycle limit.

3.2 Coupled Inductor Selection

In a SEPIC converter, selecting the proper coupled inductor is a critical step. The first decision is to select the correct switching type of operation for the application, discontinuous conduction mode (DCM) or continuous conduction mode (CCM). CCM is selected for this design to minimize the RMS currents, maximize full load efficiency while minimizing load voltage ripple. On the other hand, DCM might be chosen if good light load efficiency is required.

A rule of thumb is to use 20 to 40% of the input current for K_{IND}, which represents the peak to peak inductor ripple current, as computed with the power-balance equation where η is the estimated efficiency.

The following value is a good estimate of the efficiency:

$$\eta = 88\ \% \tag{1}$$

The input DC current is calculated as follows:

$$I_{IN,\ DC} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN,min}} \tag{2}$$

The inductor ripple current can be calculated with the following equation:

$$\Delta IL = I_{IN,DC} \times K_{IND} \tag{3}$$

Finally, the coupled inductance value is given by:

$$L \geq \frac{\left(V_{IN,\ MAX} \times D\right)}{2 \times f_{SW} \times \Delta IL} \tag{4}$$

Where D is the duty cycle and f_{SW} is the switching frequency.

Choosing a higher K_{IND} leads to:

- Lower recommended inductance
- Higher current ripple
- Higher EMI
- Faster transient performance
- Larger output capacitance for a desired output ripple

The lower current ripple typically reduces EMI, increases the maximum output current, reduces the needed output capacitance, and slows the transient response. The right tradeoff must be chosen by the designer.

It is worth mentioning that in a coupled inductor, the mutual inductance forces the ripple current to be split equally between the two coupled inductors and therefore the inductance required in a coupled inductor is half of what might be needed with two separate inductors. In addition, differently from a Flyback coupled inductor in which the coupling factor needs to be as high as possible, in a SEPIC it is preferable to have 10%-15% of leakage.

In this case, an inductor of 4.7 uH was chosen.

3.2.1 Coupling Capacitor (AC Cap)

The flying capacitor is chosen so that its ripple voltage is no more than 5% of the maximum input voltage:

$$C_{AC} \geq \frac{I_{OUT} \times D_{MAX}}{0.05 \times V_{IN,MAX} \times f_{SW}} \quad (5)$$

For this design we will choose a value of 10uF. The AC capacitor is charged to the input voltage, therefore its voltage rating must take into account enough margin with respect to the maximum input voltage. In this example the voltage rating for the AC capacitor is chosen to be 50 V.

The RMS current flowing through this capacitor is also an important parameter to take into account as it might cause overheating and damange:

$$I_{RMS,\ C_{AC}} = I_{IN,DC} \times \sqrt{\frac{1 - D_{MAX}}{D_{MAX}}} \quad (6)$$

$$I_{IN,\ DC} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN,min}} \quad (7)$$

3.3 Diode Selection

The rectifier diode on the secondary side must have a reverse voltage rating greater than the maximum input voltage plus the output voltage. The reverse voltage of the secondary diode is calculated as follows:

$$V_{(D,\ reverse)} = V_{IN,MAX} + V_{OUT} \quad + \quad V_D = 32\,V + 12\,V \quad + \quad 0.5 \quad V \quad = 44.5\,V \quad (8)$$

Due to leakage inductance, there is a negative spike when the primary side switch is being turned off. An RC snubber needs to be added across the diode to help minimize this voltage spike. Even if a snubber is added, a margin of at least 30% must be added to the value calculated in Equation 8. For this application, a diode with a reverse voltage rating of 60 V is selected.

The average current of the secondary side diode is estimated using

$$I_{D,avg} = I_{LOAD} = 1\,A \quad (9)$$

The diode must be able to conduct the value calculated in Equation 9 with some margin. For the design, the selected diode is capable of conducting 10 A of average forward current.

In addition, an appropriate package must be selected as the power dissipation can be estimated as:

$$P_{diss,D} = I_{LOAD} \times V_f \quad (10)$$

Where V_f is the forward voltage drop of the chosen diode.

3.4 MOSFET Selection

The MOSFET switch (SW) on the primary side must have a drain-source voltage rating greater than the maximum input voltage plus the output voltage. The drain-source voltage is calculated as follows:

$$V_{DS} = V_{IN,MAX} + V_{OUT} \quad (11)$$

A 30% margin must be added to the previous value.

The current through the MOSFET is calculated as follows:

$$I_{peak} = I_{LOAD} + I_{IN,DC} + \ \Delta I_L \quad (12)$$

For the power dissipation the RMS current is needed:

$$I_{peak,RMS} = \frac{I_{IN}}{\sqrt{D_{MAX}}} \quad (13)$$

In this case, a MOSFET is chosen that is rated for 80 V, 10 A.

3.5 Output Capacitor Selection

The output capacitor is required to smooth the load voltage ripple and provides an energy source during load transients and during the on-time of the MOSFET.

A practical way to size the output capacitor is based on the required load transient specification. The load transient specification is related to the control loop crossover frequency. For this estimate, it is expected that the control loop cross over frequency is set to 1/5th the RHPZ frequency, which is calculated using Equation 14.

$$f_{RHPZ} = \frac{(1 - D_{MAX})^2 \times V_{OUT}}{2\pi \times D \times L \times I_{out}} \quad (14)$$

For this design example, the load transient specification indicates that the load voltage must not overshoot or undershoot more than 100 mV during a load transient from 50% load current (0.5 A) to 100% load current (1 A) occurs. Equation 15 is used to calculate the estimated load capacitance to achieve the specified load transient load voltage ripple requirements.

$$C_{OUT} \geq \frac{\Delta I_{LOAD}}{2\pi \times f_{BW} \times \Delta V_{LOAD}} \quad (15)$$

where

- ΔI_{LOAD} is the difference in the load current conditions (1 A - 0.5 A)
- ΔV_{LOAD} is the specified overshoot voltage specification and undershoot voltage specification

In this design C_{LOAD} is selected to be 150 µF.

3.6 Input Capacitor Selection

The input capacitors smooth the supply ripple voltage during operation. The input capacitor sees fairly low ripple currents due to the input inductor; like in a boost converter, the input current waveform is continuous and triangular. For this design, the input voltage ripple is designed to be less than 250 mV when the supply voltage is at the minimum value. Equation 16 is used to estimate the required input capacitor based on the supply ripple voltage specification.

$$C_{IN\_min} = \frac{\frac{P_{OUT\_total}}{V_{SUPPLY\_min}} \times \left(1 - D\right)}{\Delta V_{SUPPLY} \times f_{SW}} = \frac{\frac{12W}{6V} \times \left(1 - 0.67\right)}{250mV \times 2.1MHz} = 1.26 \ \ \mu F \quad (16)$$

Where ΔV_{SUPPLY} is the maximum ripple that is allowed.

The input capacitor is selected to be > 40 µF. Ceramic capacitors are added to help lower the ESR of the input capacitor bank.

3.7 Output Voltage Setting

The output voltage is set with a resistive divider network. In this case, the top feedback resistor (R_{FBT}) is chose to be 51.1 k. The output voltage is expressed in the equation below, where V_{REF} is a parameter that can be found in the data sheet of the selected IC:

$$V_{LOAD} = V_{REF} \times \left(\frac{R_{FBT}}{R_{FBB}} + 1\right) \quad (17)$$

Therefore, the bottom resistor (R_{FBB}) can be calculated as follows:

$$R_{FBB} = \frac{R_{FBT}}{\frac{V_{LOAD}}{V_{REF}} - 1} \quad (18)$$

4 Simplified SEPIC Schematic

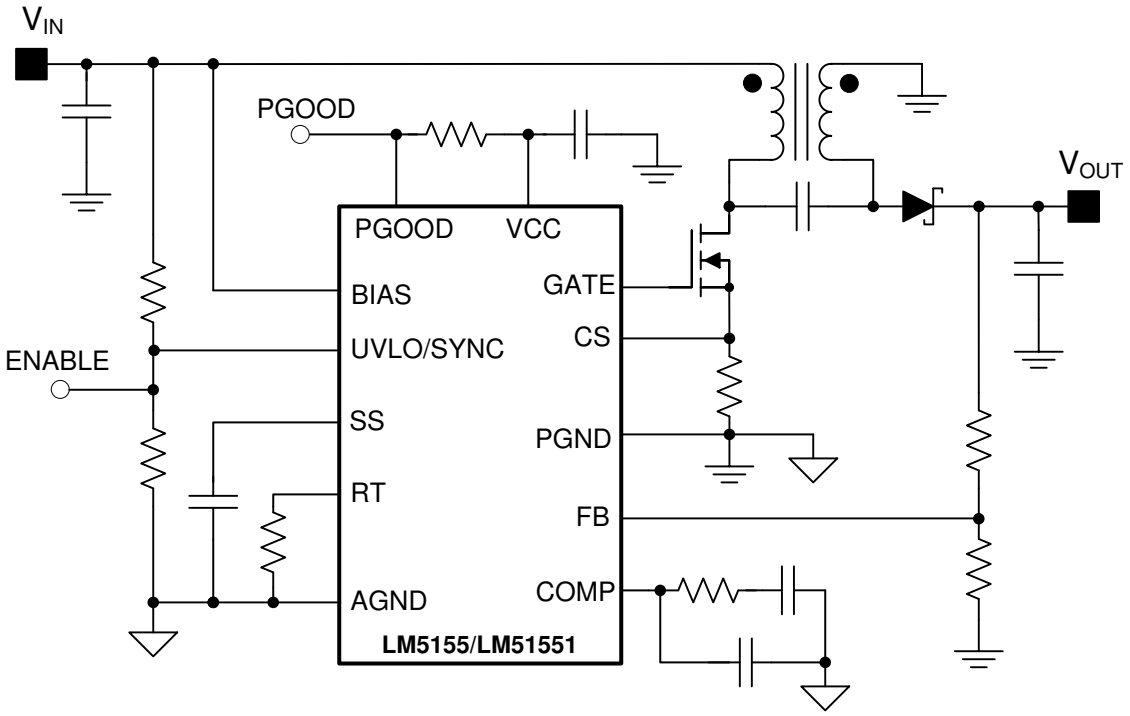

Figure 4-1. Application Circuit

5 References

- Texas Instruments, *LM5155 SEPIC Evaluation Module*.
- Texas Instruments, *LM5155 and LM5156 Quickstart Calculator for SEPIC Regulator Design (Rev. A)*.
- Texas Instruments, *LM5155x 2.2-MHz Wide Input Nonsynchronous Boost, SEPIC, Flyback Controller* data sheet.
- Texas Instruments, *Designing DC/DC Converters Based on SEPIC Topology* Analog Applications Journal.
- Texas Instruments, *TPS61175 SEPIC Design* application note.

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