Application Note

Bi-polar Fly-Buck-Boost Solution for Analog Output Modules

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ABSTRACT

This application brief describes a bi-polar (split-rail) ±15-V and 125-mA output power design usable in analog output modules of PLCs (Programmable Logic Controllers). The input voltage range of the design is 16 V to 35 V to address the standard 24-V rail which typically can be found in PLC applications. A Fly Buck-Boost (FBB) topology with an off-the shelf 1:1 coupled inductor driven by a single DC/DC converter is selected. This selection makes sure that the switching frequency for the positive and the negative output is identical to avoid beat frequencies and support the wide input voltage range. Operation at 1 MHz enables the use of a small coupled inductor and provides low-output ripple voltage of around 40 mVp-p. The selected LMR36506RFRPER forced PWM synchronous buck converter warrants accurate output voltage under symmetrical, as well as under non-symmetrical, loading of the positive and negative output rails.

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1 Introduction

1.1 Topology Selection

Multiple topologies and designs are available for providing a positive (Pos VOUT) and a negative voltage (Neg VOUT) rail from a positive input voltage (VIN). For example, there are dedicated devices containing a boost converter plus an inverting buck-boost converter (TPS65130, TPS65131, TPS65133), devices with boost or LDO plus negative charge pump (TPS65132, LM27762), but also single inductor multiple output split-rail converters (TPS65135). Aside from these devices, designers can also choose from several topologies and related devices typically used for isolated power conversion.[1] These devices are also used for non-isolated applications as well. Open loop push-pull (SN6501, SN6505, SN6507) or LLC (UCC25800) devices belong to this category as well as primary-side-regulated flyback.[2] Furthermore, the use of buck converters in fly-buck or fly-buck-boost topology is a possible solution.

The latter two devices have the advantage of choosing devices from a huge buck converter portfolio and of being usable for applications with a wide VIN tolerance range. The use of these device is also supported by a range of off-the-shelf coupled inductors offered by different inductor vendors. The largest offering of those off-the-shelf inductors is available for a turns ratio of 1:1, enabling straight-forward inductor selection but leading also to specific limitations in regards of the desired designed for duty cycle.

Both topologies generate a very well-regulated non-isolated primary output voltage; with a positive output for fly-buck and negative output for fly-buck-boost. The secondary output voltage is usually an isolated output voltage, by *following* the voltage on the primary side. The energy transfer to the secondary side takes place during the off-time of a switching cycle and leads to a desired duty cycle of less than 50%; leaving more than 50% of the period time available for the energy transfer to the secondary side. Considering the preferable use of a 1:1 coupled inductor, this requirement can be fulfilled for the fly-buck for a VINmin > 2 × VOUT, while the fly-buck-boost is able to fulfill this requirement already for a VINmin > VOUT. Based on these considerations a fly-buck can need a minimum VIN of 30 V to generate the ±15 V, while a fly-buck-boost is able to work with a minimum VIN of 15 V.

1.2 From Buck to Fly-Buck-Boost Converter

The basics of how to use a buck converter in a fly-buck-boost topology are illustrated by Figure 1-1. The left side of this figure illustrates the standard buck, whereas the right side shows how a standard buck converter can be used in the fly-buck-boost topology.

To achieve this design, the buck converter is first converted into an inverting buck-boost topology. The needed modifications for that are shown in red. VOUT and GND label or symbol on the output of the buck converter needs to be interchanged as a first step. An additional bypass capacitor (Cbyp) is needed for bypassing the buck converter-IC U1 supply voltage. Schottky diode D3 avoids the possibility that U1 is overstressed by the charging current of Cbyp during start-up. Special care is required for the signals referred, directly, or through resistors or capacitors connected to ground in a normal buck converter. For example, for the GND-, FB-, EN-/UVLO-, PG-, RT- and VCC-pin of U1, the signals need to be referred in an inverting buck-boost to neg VOUT instead. The input voltage that can be applied to an inverting buck-boost converter is less than the input voltage that can be applied to the same buck converter. This relationship is because the GND-pin of the IC is connected to the negative output voltage Neg VOUT. Therefore, the input voltage across the converter-IC U1 is VIN + |Neg VOUT|.

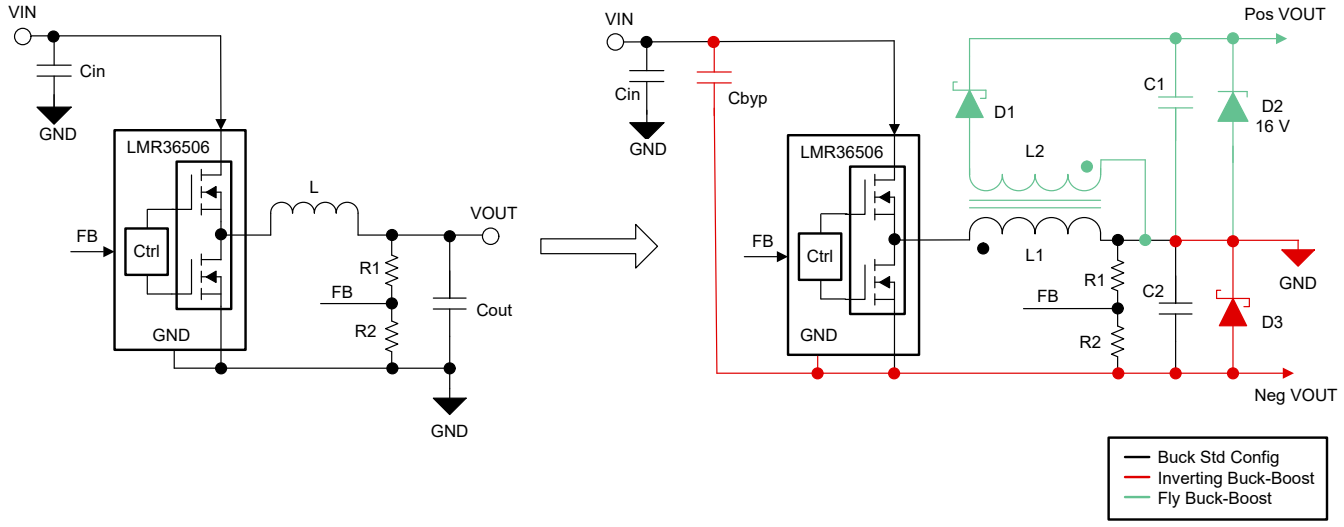

Figure 1-1. Buck Converter Versus Fly-Buck-Boost Converter

As a next step, the inverting buck-boost is converted into the desired fly-buck-boost topology by adding the components and connections shown in green. Those connections are a second winding (L2) on the existing inductor (L1), a rectifying Schottky diode (D1), an output capacitor (C1), and the clamping Zener diode (D2). The two windings L1 and L2 preferably have the same number of turns, resulting in a coupled inductor with a 1:1 turns ratio. Such configuration of inductors is available as off-the-shelf product from the majority of inductor manufacturers. The energy stored during the ON-time of the converter by L1 releases during the OFF-time by L1 and L2 through the low-side FET of U1 and the Schottky diode D1 to the output capacitors C2 and C1. Because of the 1:1 turns ratio across the windings, L1 and L2 have the same voltage during the OFF-time leading to a good match of the non-regulated positive output voltage (Pos VOUT) to the well-regulated negative output voltage (Neg VOUT). The remaining tolerances of the Pos VOUT are due to the temperature- and load-dependent forward voltage drop of D1 at medium-to-maximum output current on the Pos VOUT. At very low output current on Pos VOUT there is a slight rise of that rail caused by the peak rectification of unavoidable spikes. The latter behavior is addressed by the clamping Zener diode D2, which has a Zener voltage slightly larger than the maximum nominal voltage to be expected as Pos VOUT.

2 Specific Implementation of the Fly-Buck-Boost Converter

The schematic of the implemented design is shown in Figure 2-1. An adjustable version of a LMR36506 buck converter is selected for U1 due to the wide VIN range and small size of 2 mm × 2 mm. The maximum recommended 65-V input voltage supports the targeted 35-V supply and the -15-V Neg VOUT. The resulting supply voltage stress for U1 is 35 V + |-15 V| = 50 V, as outlined in the schematic.

This implementation leaves an ample margin for increasing the Neg VOUT or for transients on VIN. The Forced PWM version (LMR36506RFRPER) of the device is selected to provide the operation with a fixed frequency. This version is also selected for the best load and cross-regulation, independent of the load conditions (that is from no-load to full-load) as well as from balanced-load to completely non-symmetrical loading of the two outputs. The device allows for adjusting the switching frequency over a wide range from 200 kHz to 2.2 MHz. By connecting the RT-pin of U1 to the VCC-pin, a 1-MHz frequency is selected as a reasonable tradeoff between size and efficiency. The selected frequency enables the use of a small coupled inductor (L1) with a size of 6 mm × 6 mm. The negative output voltage (Neg VOUT) is adjusted by the output voltage divider R3, R7 (and R10) to -15 V. R10 allows the injection of a small AC signal, using the test points A and B for the purpose of loop-stability evaluation and measurement and can be replaced by a 0-Ω resistor in a final circuit. C10 is an optional feed-forward capacitor (not used in the evaluated circuit) for modifying the loop (transfer function).

The PNP BJT Q1 forms together with R1, R2, R4, and R9 to make a level shifter to generate a VIN dependent EN signal for U1, which is completely independent of the value of Neg VOUT. The complete circuit turns on for supply voltage levels of approximately 14.4 V and turns off at approximately 10.7 V, with the specific component values of this level shifter.

2.1 Schematic

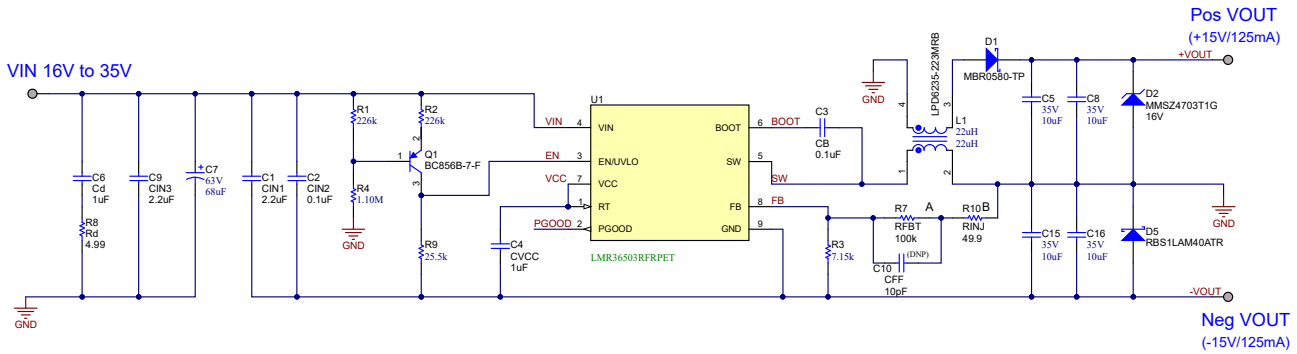

Figure 2-1. Split-Rail Fly-Buck-Boost Topology

2.2 Bill of Materials

The Table 2-1 highlights the parts used to design the schematic in Section 2.1.

Table 2-1. Bill of Materials

Item #	Designator	Quantity	Part Number	Manufacturer	Description	Package Reference
1	!PCB	1	BSR086	Any	Printed Circuit Board	
2	C1, C9	2	CGA5L3X7S2A225K160AB	TDK	CAP, CERM, 2.2 uF, 100 V, +/- 10%, X7S, AEC-Q200 Grade 1, 1206	1206
3	C2	1	GRM188R72A104KA35D	MuRata	CAP, CERM, 0.1 uF, 100 V, +/- 10%, X7R, 0603	603
4	C3	1	GCM155R71C104KA55D	MuRata	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402	402
5	C4	1	8.85012E+11	Wuerth Elektronik	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603	603
6	C5, C8, C15, C16	4	CGA5L1X7R1V106K160AC	TDK	CAP, CERM, 10 uF, 35 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206_190	1206_190
7	C6	1	C3216X7R2A105K160AA	TDK	CAP, CERM, 1 uF, 100 V, +/- 10%, X7R, 1206	1206
8	C7	1	UCD1J680MNL1GS	Nichicon	CAP, AL, 68 uF, 63 V, +/- 20%, SMD	D10xL10mm
9	D1	1	MBR0580-TP	Micro Commercial Components	Diode, Schottky, 80 V, 0.5 A, SOD-123	SOD-123
10	D2	1	MMSZ4703T1G	ON Semiconductor	Diode, Zener, 16 V, 500 mW, SOD-123	SOD-123
11	D5	1	RBS1LAM40ATR	Rohm	DIODE SCHOTTKY 20 V 1 A PMDTM	SOD128

Table 2-1. Bill of Materials (continued)

Item #	Designator	Quantity	Part Number	Manufacturer	Description	Package Reference
12	L1	1	LPD6235-223MRB	Coilcraft	inductor, 22 uH, 1.73 A, 0.3 ohm, SMD	6x6mm
13	LBL1	1	THT-14-423-10	Brady	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch
14	Q1	1	BC856B-7-F	Diodes Inc.	Transistor, PNP, 65 V, 0.1 A, SOT-23	SOT-23
15	R1	1	CRCW04021M10FKED	Vishay-Dale	RES, 1.10 M, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402
16	R2, R4	2	CRCW0402226KFKED	Vishay-Dale	RES, 226 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402
17	R3	1	CRCW04027K15FKED	Vishay-Dale	RES, 7.15 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402
18	R7	1	CRCW0402100KFKED	Vishay-Dale	RES, 100 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402
19	R8	1	CRCW06034R99FKEA	Vishay-Dale	RES, 4.99, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603
20	R9	1	CRCW040225K5FKED	Vishay-Dale	RES, 25.5 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402
21	R10	1	CRCW040249R9FKED	Vishay-Dale	RES, 49.9, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	402
22	TP1, TP6, TP7	3	1502-2	Keystone	Terminal, Turret, TH, Double	Keystone1502-2
23	U1	1	LMR36506RFRPER	Texas Instruments	LMR36503/06-Q1 Wide Input 60-V Synchronous, DC-DC Buck Converter, RPE0009A (VQFN-9)	RPE0009A
24	C10	0	CGA2B2C0G1H100D050BA	TDK	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	402
25	FID1, FID2, FID3, FID4, FID5, FID6	0	N/A	N/A	Fiduciary mark. There is nothing to buy or mount.	N/A

3 Test Results

3.1 Start-up Behavior

Figure 3-1 shows the typical start-up behavior of fly-buck-boost configuration where the signals on the positive and negative rails ramp-up symmetrically on the supply of VIN. The pink line indicates the input voltage of 16 V and the dark and light-blue lines are the positive and negative rail signals ramping up to ±15 V symmetrically.

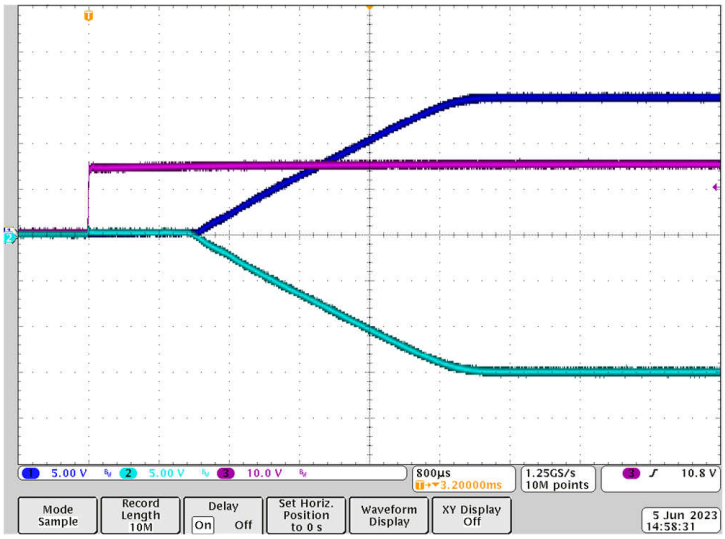

Figure 3-1. Start-up Behavior of Fly-Buck-Boost Topology

3.2 System Loop Stability

Loop stability is an important factor in the system. The guideline for a stable design is a desired phase margin of at least 45°. The loop stability is measured for the designed fly-buck-boost design with the following conditions:

1. VIN 16 V, Load resistance of 240 Ω between Pos VOUT and Neg VOUT
2. VIN 24 V, Load resistance of 170 Ω between Pos VOUT and Neg VOUT
3. VIN 35 V, Load resistance of 150 Ω between Pos VOUT and Neg VOUT

Gain and phase margin plots measured for the previous conditions are shown in Figure 3-2 with the cross-over frequency of approximately 20 kHz and phase margin in the range of 60°. These test points make sure that the design is stable.

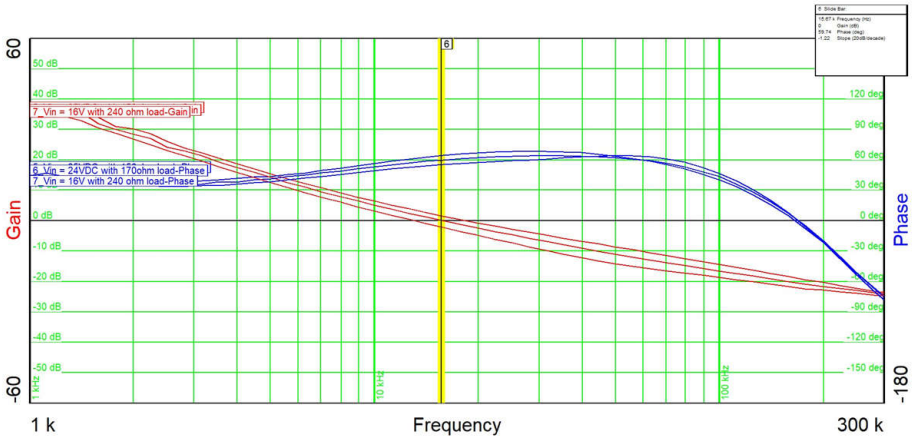

Figure 3-2. System Loop Stability

3.3 Thermal Behavior

The thermal test is conducted on a modified LMR36506RFRPER EVM board to make sure that the components can withstand the industrial temperature range. The temperatures of three major components such as Inductor, DC/DC converter and the diode are observed for the minimum and maximum VIN, as shown in Figure 3-3 and Figure 3-4, respectively.

The temperature of an inductor and DC/DC converter are in the range of 48°C with the VIN of 16 V and a load of 175 mA applied on both output channels, while the diode remains at 32.6°C. With the VIN of 35 V and load of 250 mA on both output channels, the temperature of an inductor and DC/DC converter are in the range of 50°C while the diode remains at 33.4°C. This thermal output demonstrates the thermal metrics of the board, which are well within the industrial temperature range.

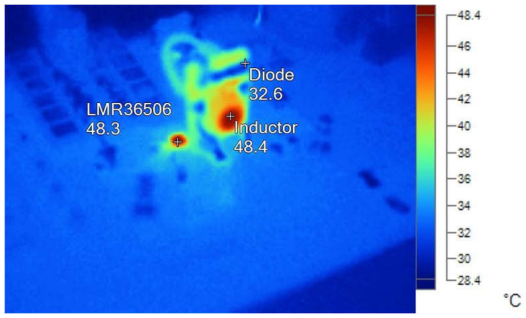

Figure 3-3. Thermal Behavior at 16-V Vin, 175-mA Load on Both Rails

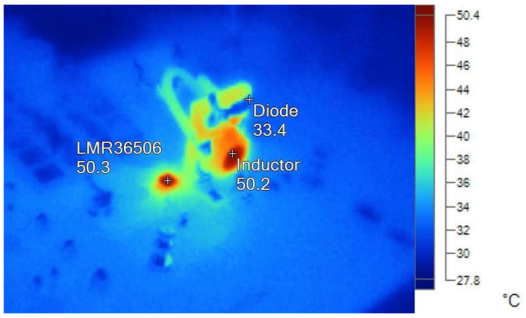

Figure 3-4. Thermal Behavior at 35-V Vin, 250-mA Load on Both Rails

3.4 VOUT Ripple and SW Node Waveforms

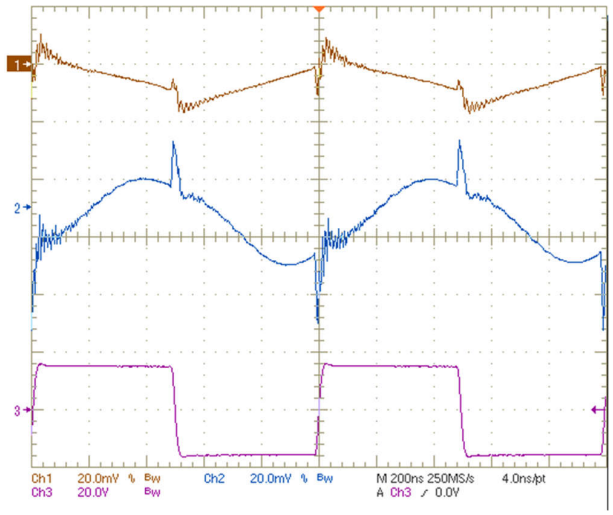

Figure 3-5. VOUT Ripple and SW Node Waveforms With Both Rails Loaded With 125 mA at 16-V Vin

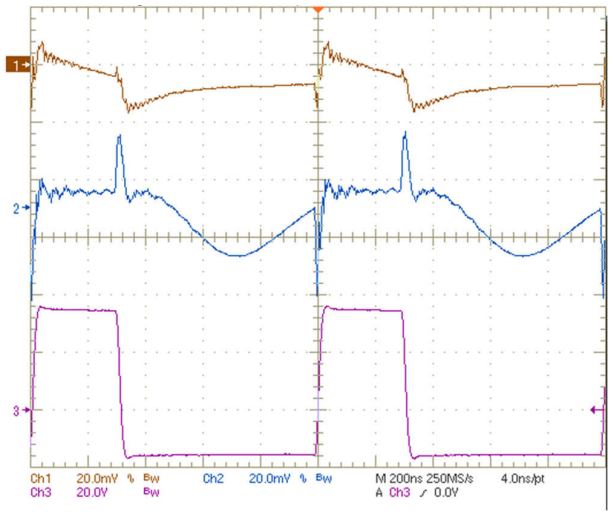

Figure 3-6. VOUT Ripple and SW Node Waveforms With Both Rails Loaded With 125 mA at 35-V Vin

3.5 Efficiency Data

3.5.1 Efficiency Data for Balanced Loads

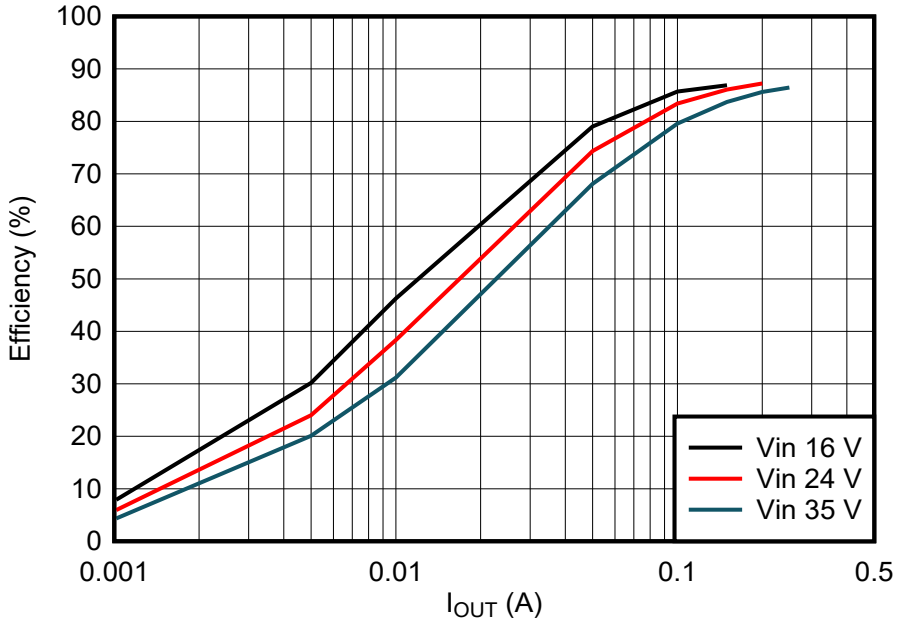

Figure 3-7. Efficiency Versus Output Current for Balanced Loads

3.5.2 Efficiency Data for Unbalanced Loads

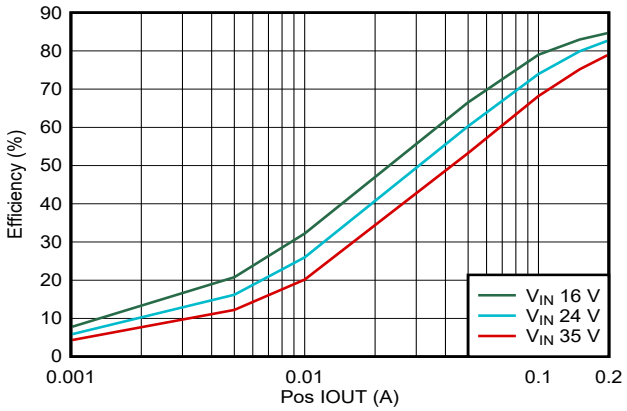

Figure 3-8. Efficiency With Neg IOUT Set at 1 mA and Pos IOUT Increasing From 1 mA to 150 mA

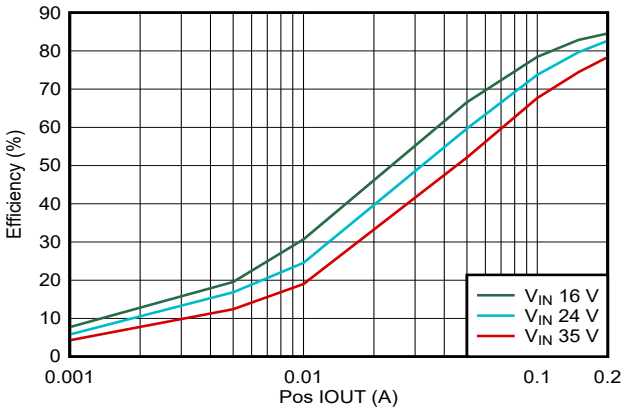

Figure 3-9. Efficiency With Pos IOUT Set at 1 mA and Neg IOUT Increasing From 1 mA to 150 mA

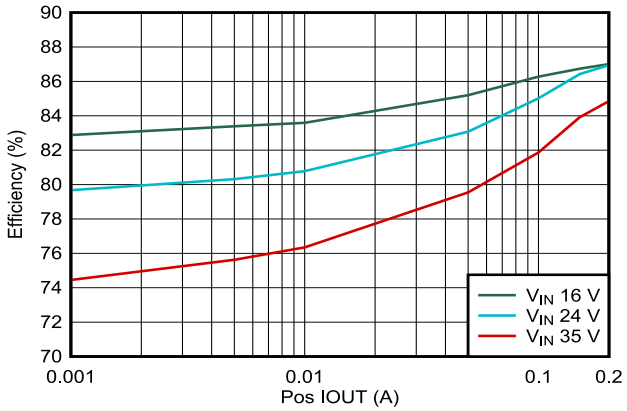

Figure 3-10. Efficiency With Neg IOUT Set at 150 mA and Pos IOUT Increasing From 1 mA to 150 mA

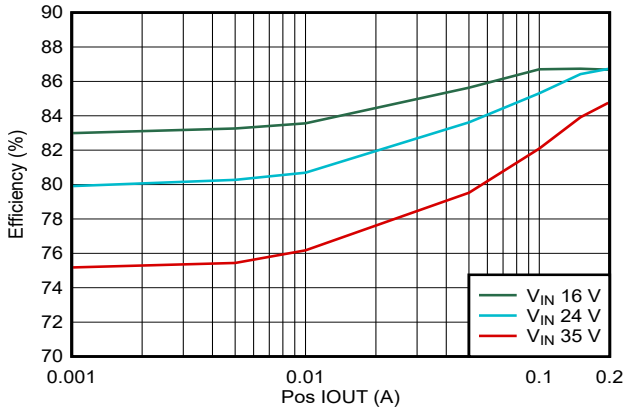

Figure 3-11. Efficiency With Pos IOUT Set at 150 mA and Neg IOUT Increasing From 1 mA to 150 mA

3.6 Load Regulation

3.6.1 Load Regulation for Balanced Loads

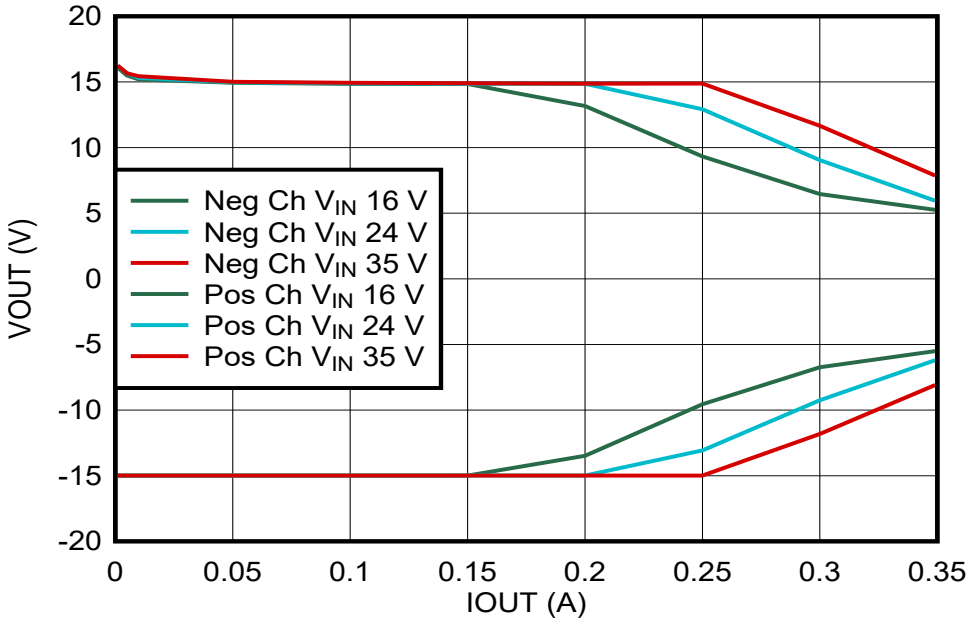

Figure 3-12. Output Voltage Versus Output Current for Balanced Loads

3.6.2 Load Regulation for Unbalanced Loads

Note

Dashed lines indicate Pos VOUT (V) and solid lines indicate Neg VOUT (V) in the following graphs.

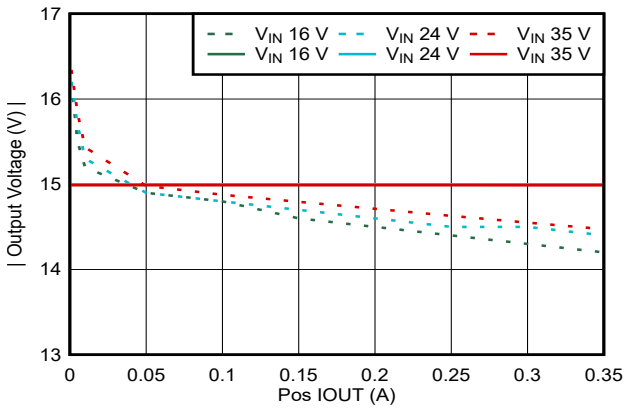

Figure 3-13. Load Regulation With Neg IOUT Set at 1 mA and Pos IOUT Increasing From 1 mA to 150 mA

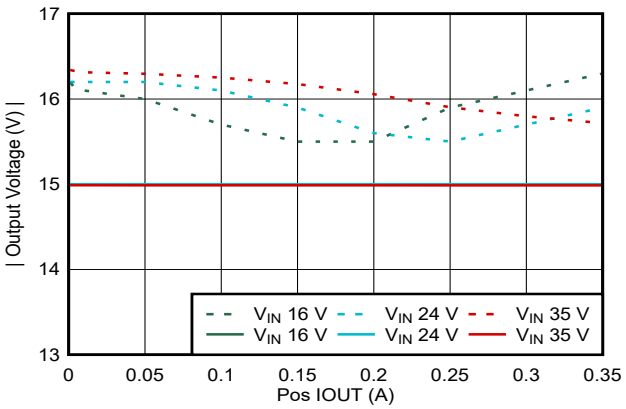

Figure 3-14. Load Regulation With Pos IOUT Set at 1 mA and Neg IOUT Increasing From 1 mA to 150 mA

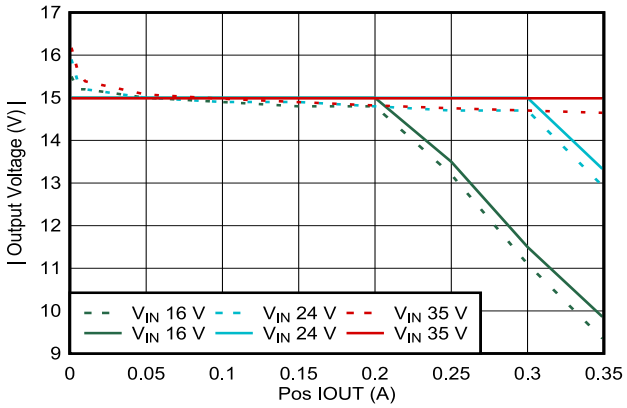

Figure 3-15. Load Regulation With Neg IOUT Set at 150 mA and Pos IOUT Increasing From 1 mA to 150 mA

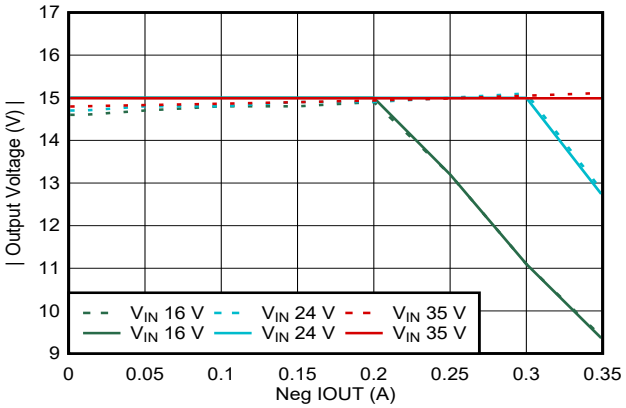

Figure 3-16. Load Regulation With Pos IOUT Set at 150 mA and Neg IOUT Increasing From 1 mA to 150 mA

4 Summary

The LMR36506RFRPER can be configured as a split-rail output Fly Buck Boost to generate a positive and a negative output supply rail for balanced loads as well as for non-symmetrical loads. The Fly Buck Boost topology changes some system characteristics and limitations, such as input voltage range and maximum output current. The desired 125-mA load current can be supported by the topology with an input voltage range of 16 V to 35 V. The output is regulated on the negative channel in the design. This application note explains the Split Rail Fly Buck-Boost topology with the design considerations. Measurement data based on a modified EVM design is provided in this application note.

5 References

1. Texas Instruments, *Isolated Power Topologies for PLC I/O Modules and Other Low-Power Applications*, application note.
2. Texas Instruments, *LM5181 Bipolar + and - 18 V Output Design for Signal Chains in PLC Applications*, application note.
3. Texas Instruments, *Using the TPS62150 in a Split Rail Topology*, application note.
4. Texas Instruments, *Using the TPS54335A to Create an Inverting Power Supply*, application note.

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