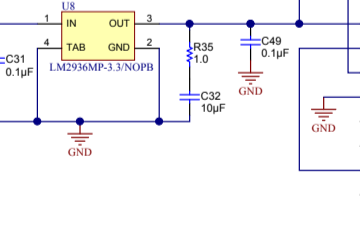
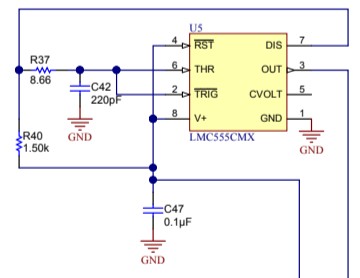
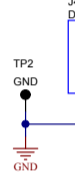


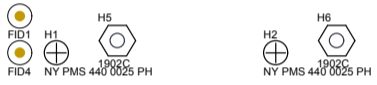
Input Voltage = 9Vin to 16Vin

24Vout @ 25A max.

Drive low = Corresponding phase enabled.
 Drive high = Corresponding phase disabled.
 If Phase 1 (Master) is disabled,
 all other phases will also be disabled.



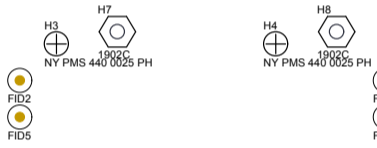
Revision History	
Revision	Notes
E1	Initial Design
A	Changes for PCB layout



PCB Number: PMP7969
PCB Rev: A

PCB LOGO
Texas Instruments

PCB LOGO
ESD Susceptible



LBL1
PCB Label
Size: 0.65" x 0.20"

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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Designed for Public Release		Mod. Date: 2/18/2015	
Number: PMP7969		Rev: A	
SVN Rev: Version control disabled		Assembly Variant: 001	
Drawn By: Robert Sheehan		File: PMP7969A_Hdrw_SchDoc	
Engineer: Robert Sheehan		Contact: http://www.ti.com/support	
Project Title: LMS122 4 phase boost		Sheet: 2 of 2	
Size: B		http://www.ti.com	
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