Test Data
For PMP7877 RevB
11/29/2012

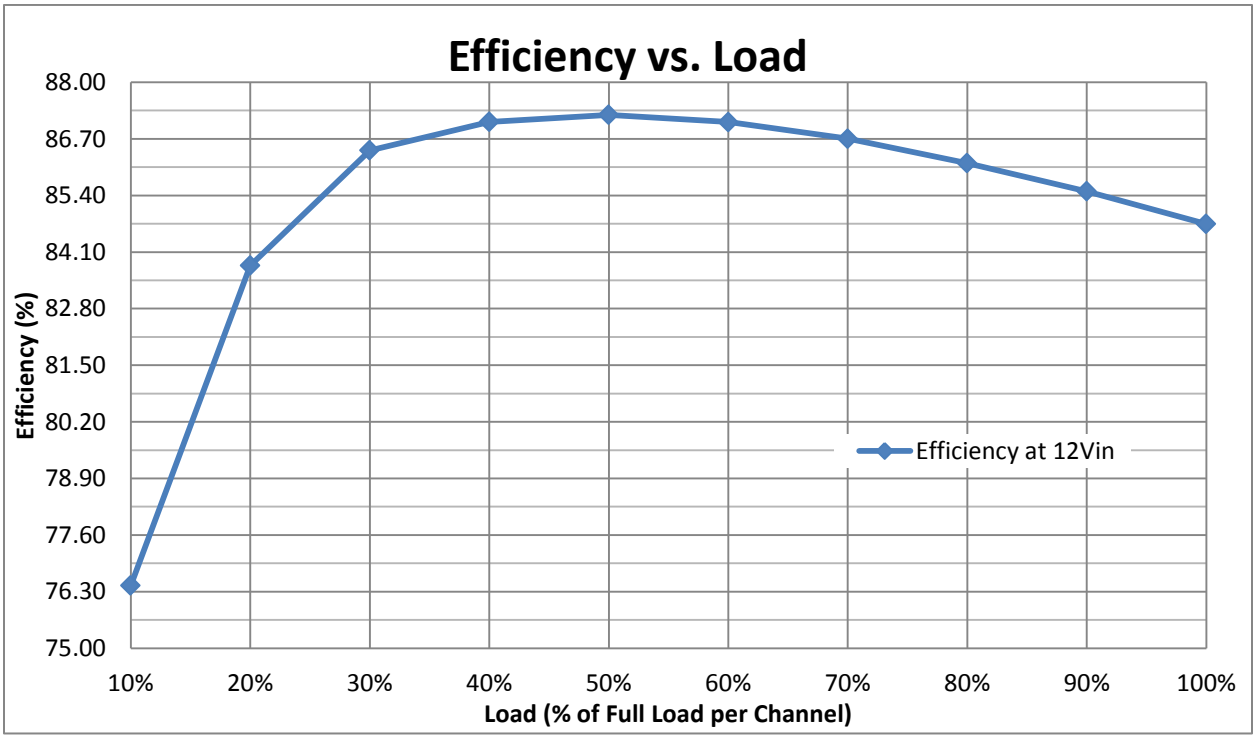
Test SPECIFICATIONS

Vin Nominal	**12V**
Vout 1 (U2 Output) LM2130	**1V @ 5A**
Vout 2 (U4 CH1 Output) LM25119 (-A)	**1.8V @ 2.5A**
Vout 3 (U4 CH2 Output) LM25119 (-B)	**1.5V @ 6A***
Vout 4 (U7 Output) (LM21305)	**3.3V @ 5A**
Vout 5 (U8 Output) (LM21305)	**3.3V @ 5A**
Vout 6 (U6 Output) (LMR12020)	**5V @ 2A**
Vout 7 (U5 Output) (TPS51200)	**0.75V @ 1A continuous; 3A peak**

***Note: The U4 CH2 Output of 6A includes the 1A drawn by the U5 LDO.**

TYPICAL PERFORMANCE

EFFICIENCY

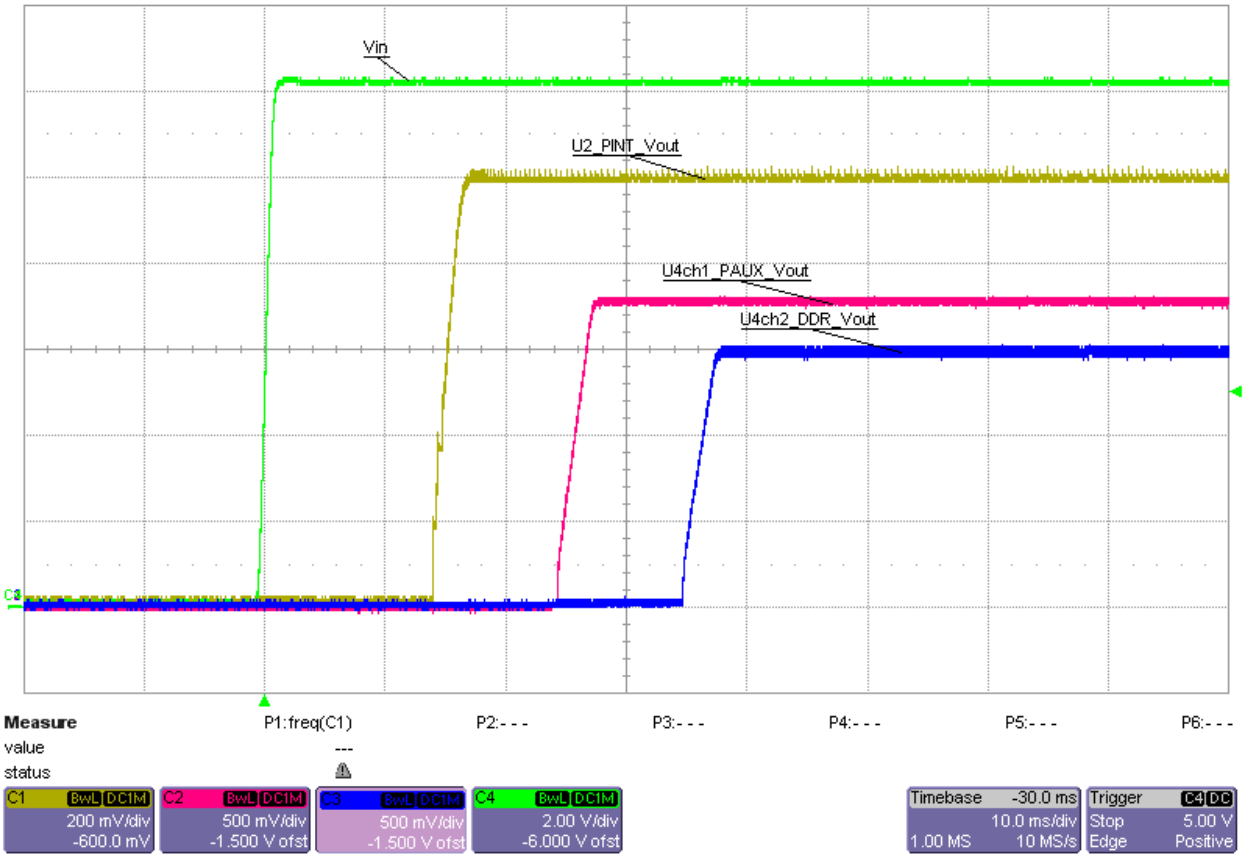


Load	Pin	Pout Total	Efficiency
10%	7.922105	6.05595	76.44
20%	14.45645	12.113238	83.79
30%	20.99702	18.149403	86.44
40%	27.7812	24.194852	87.09
50%	34.64134	30.225695	87.25
60%	41.63847	36.260918	87.09
70%	48.77706	42.291847	86.70
80%	56.09169	48.317999	86.14
90%	63.55573	54.338344	85.50
100%	71.23649	60.370435	84.75

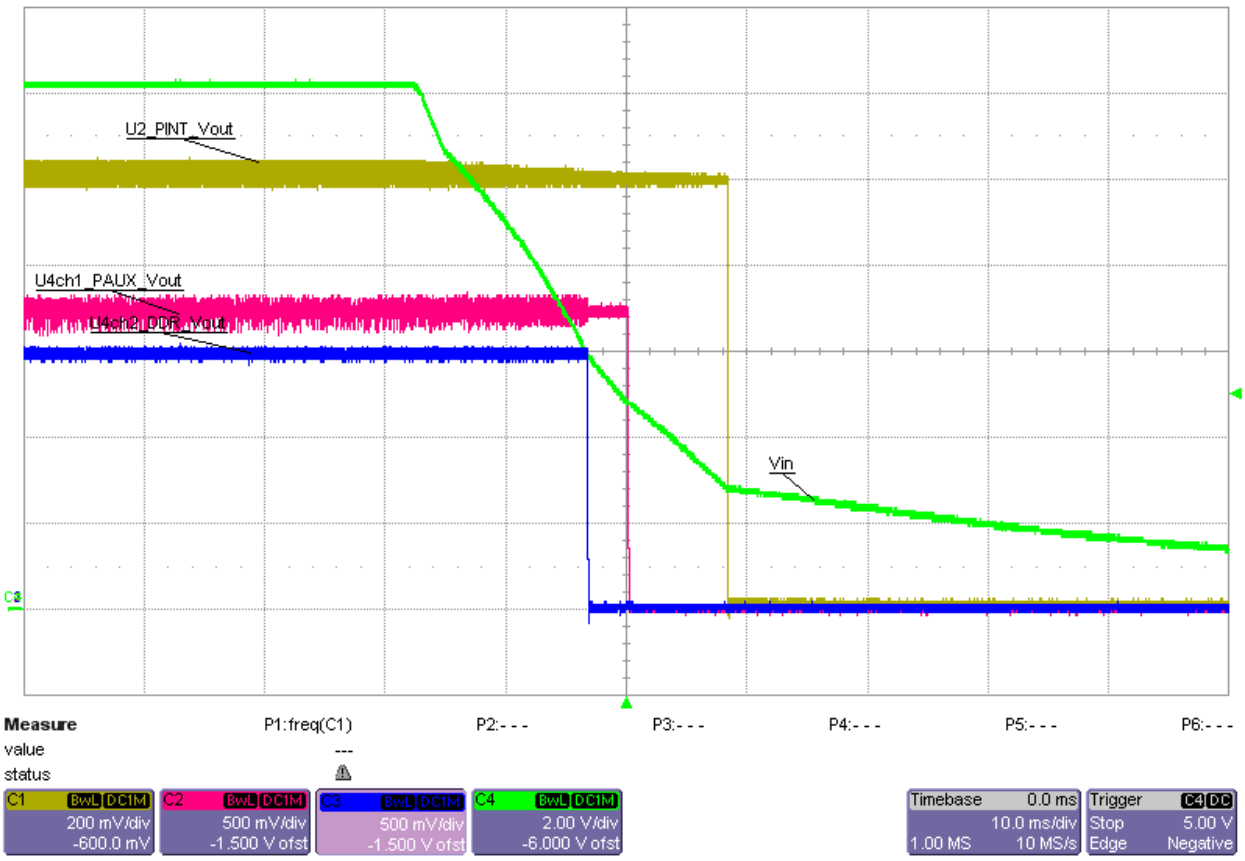
Efficiency was measured with each output channel being incremented by 10% of their corresponding full load current.

Waveforms

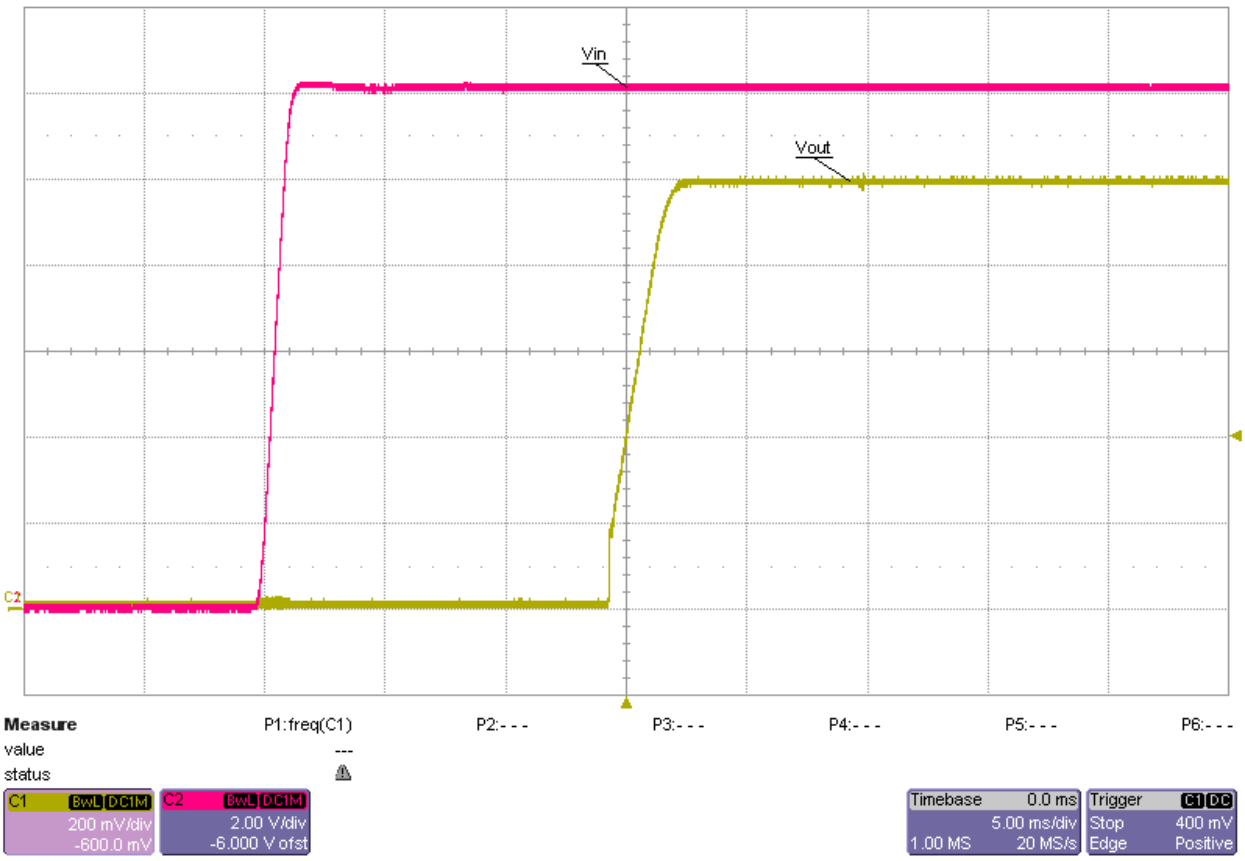
Startup



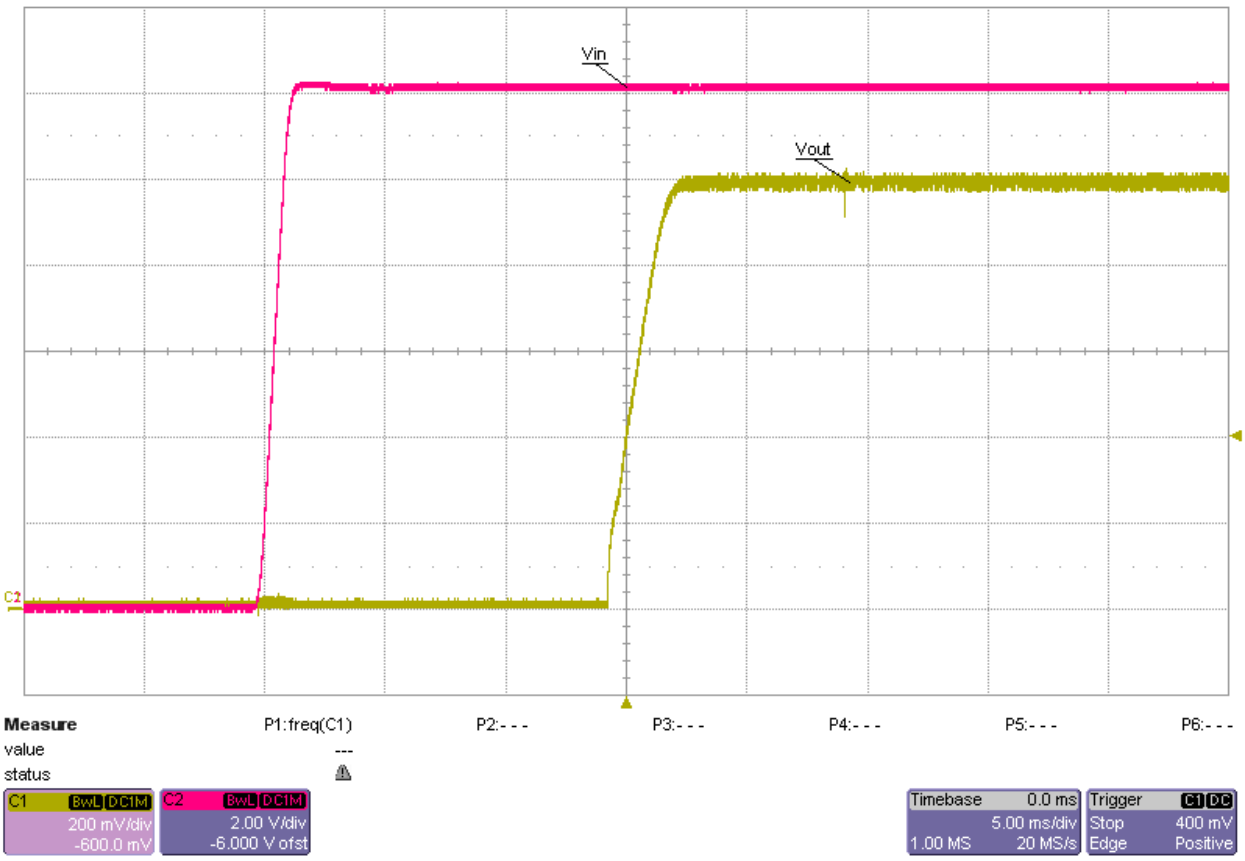
Startup Sequencing (into no load)



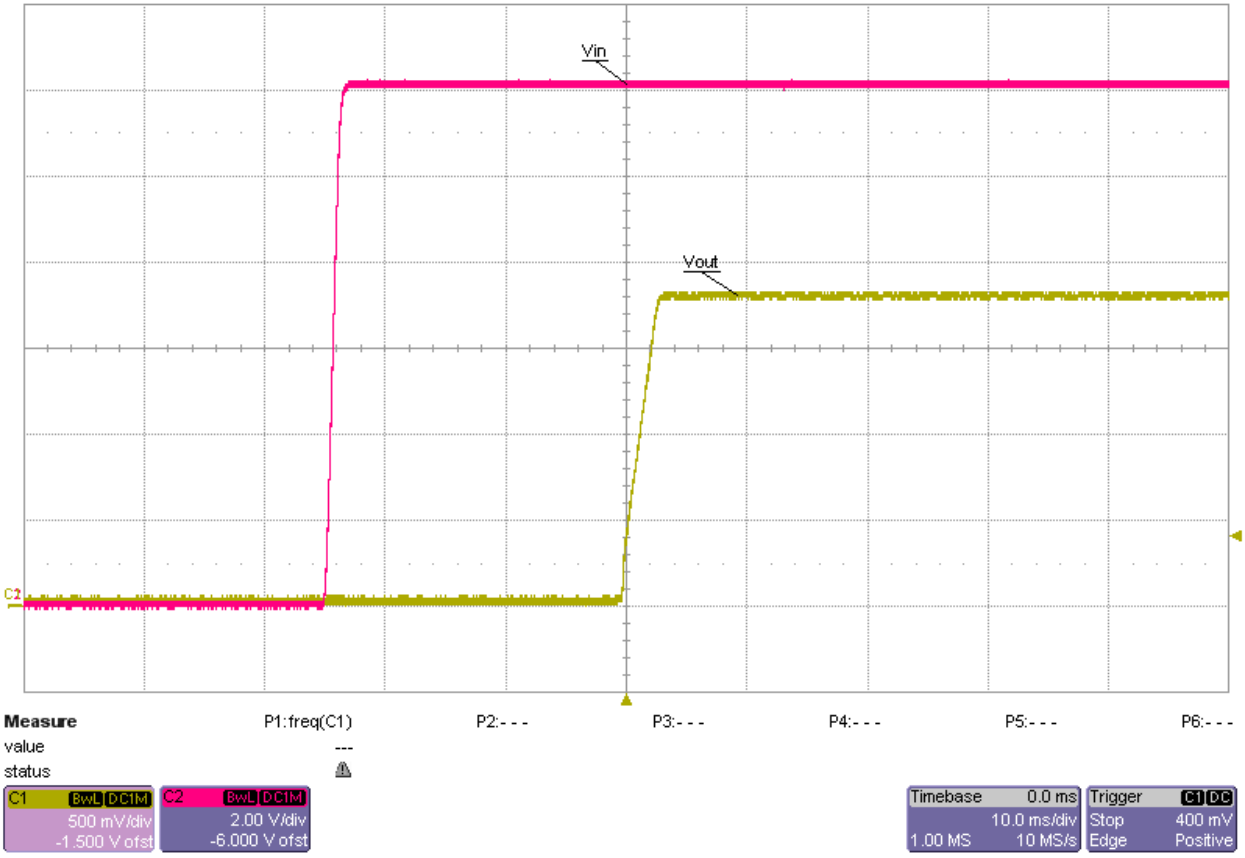
Shutdown Sequencing (Each output loaded to 50% of corresponding channel's full load value)



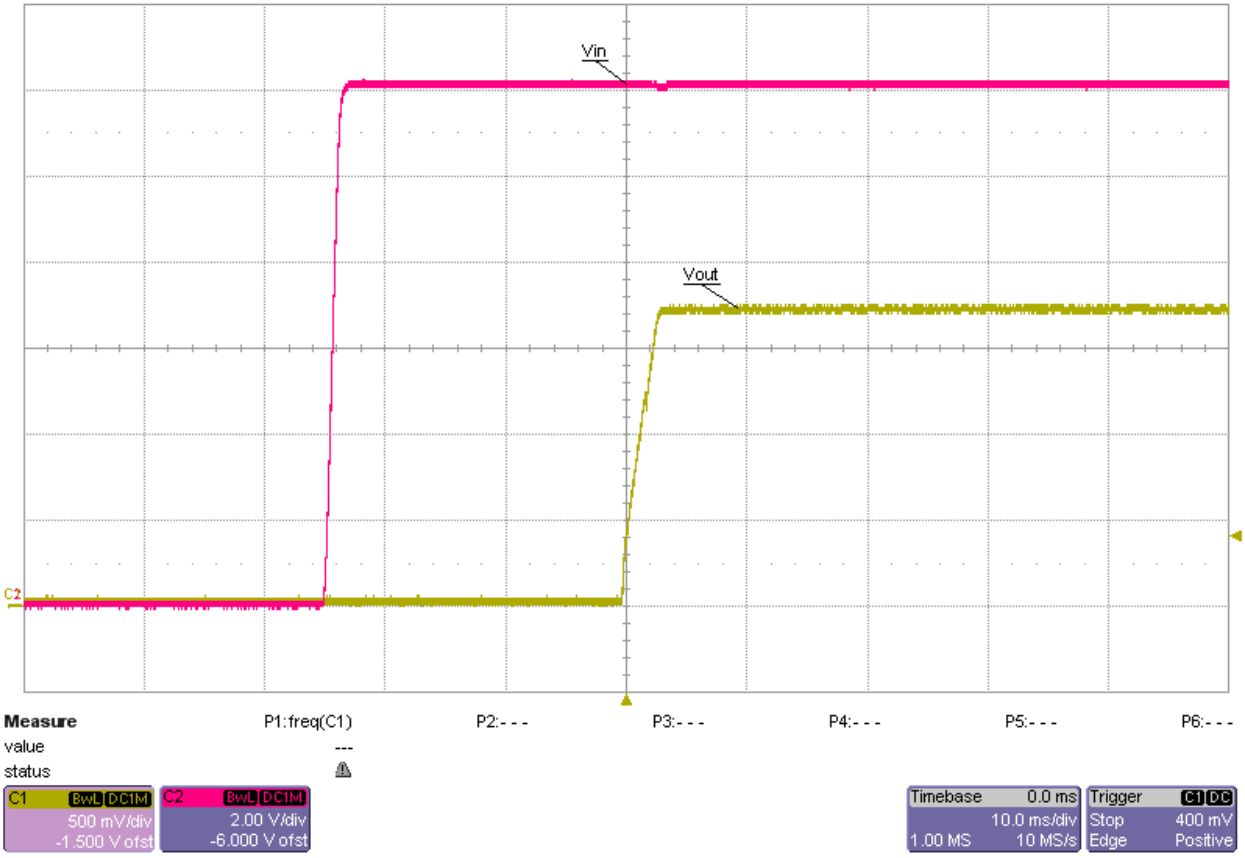
U2 (1V @ 5A) Startup into No Load (all other channel outputs not loaded)



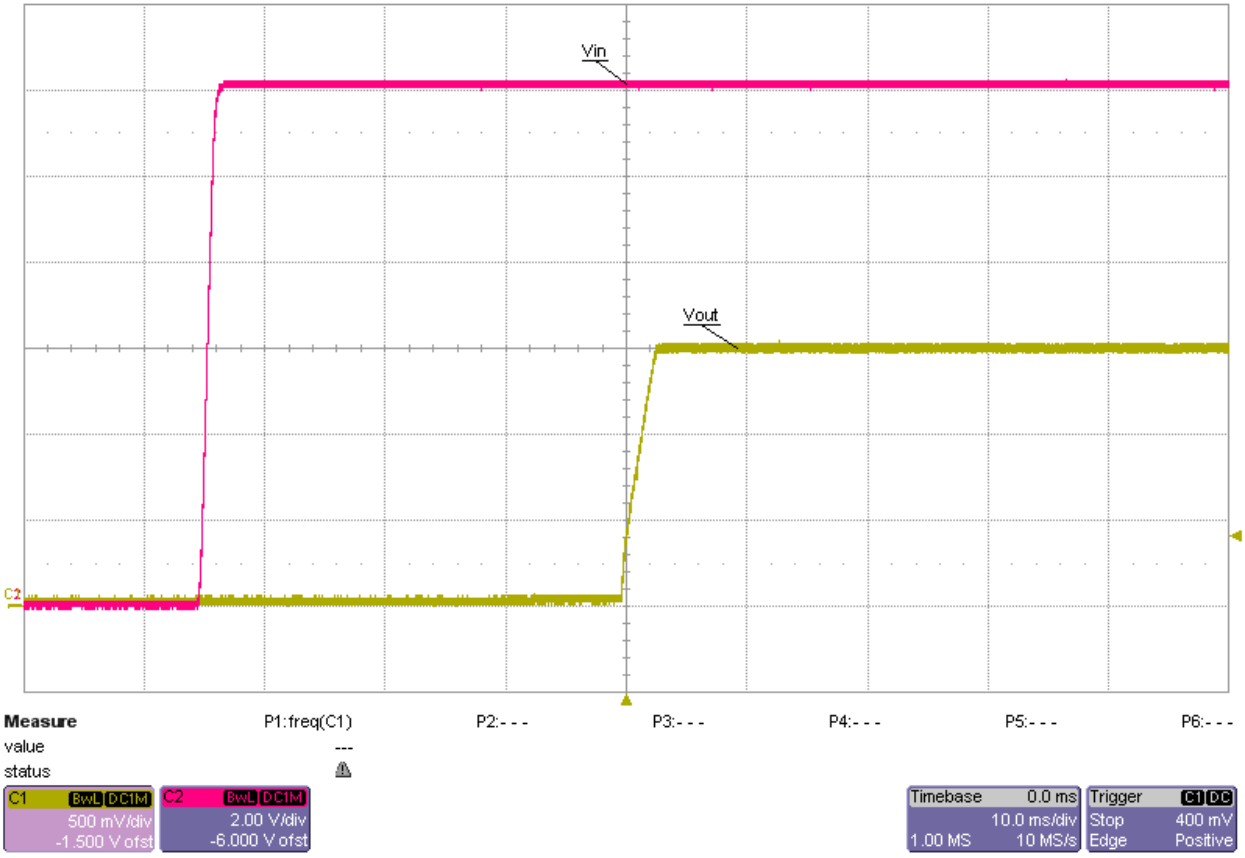
U2 (1V @ 5A) Startup into 5A Load (all other channel outputs not loaded)



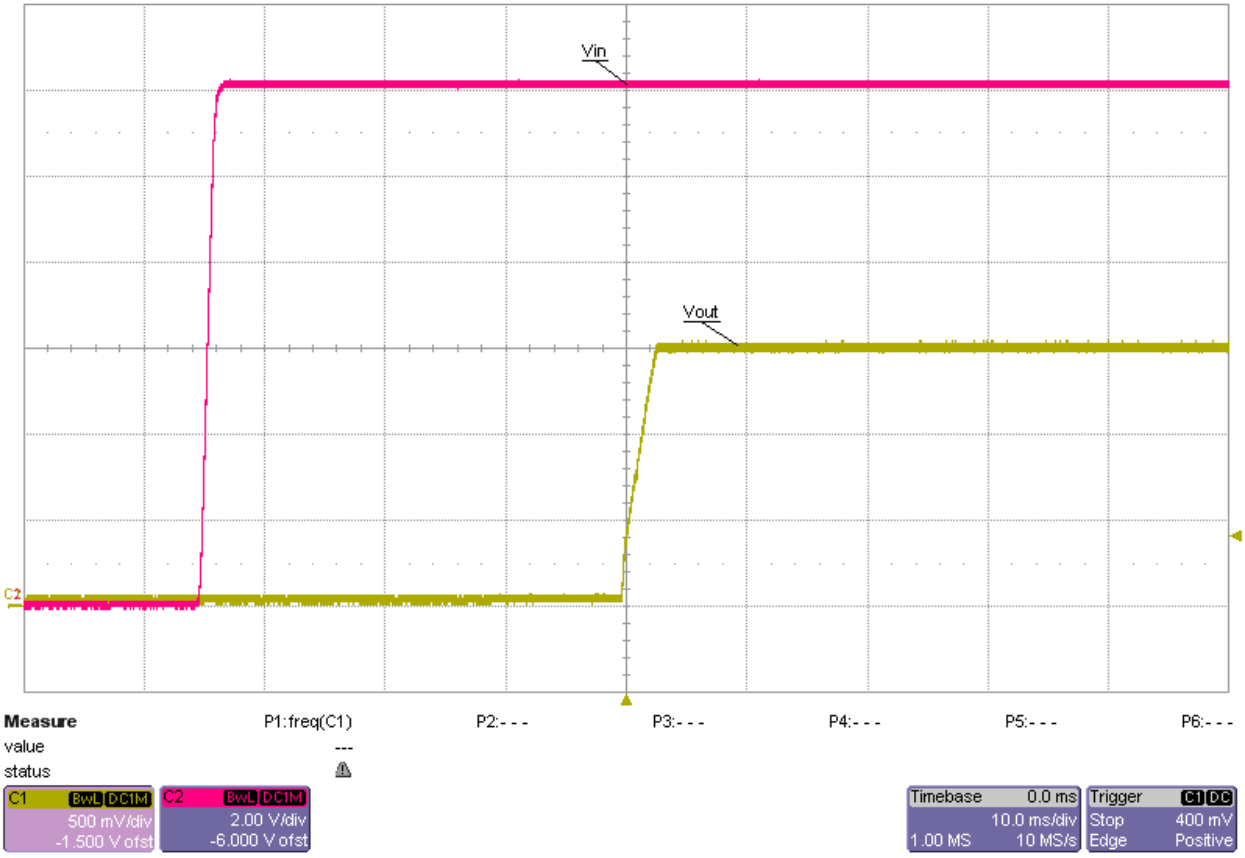
U4 CH1 (1.8V @ 2.5A) Startup into No Load (all other channel outputs not loaded)



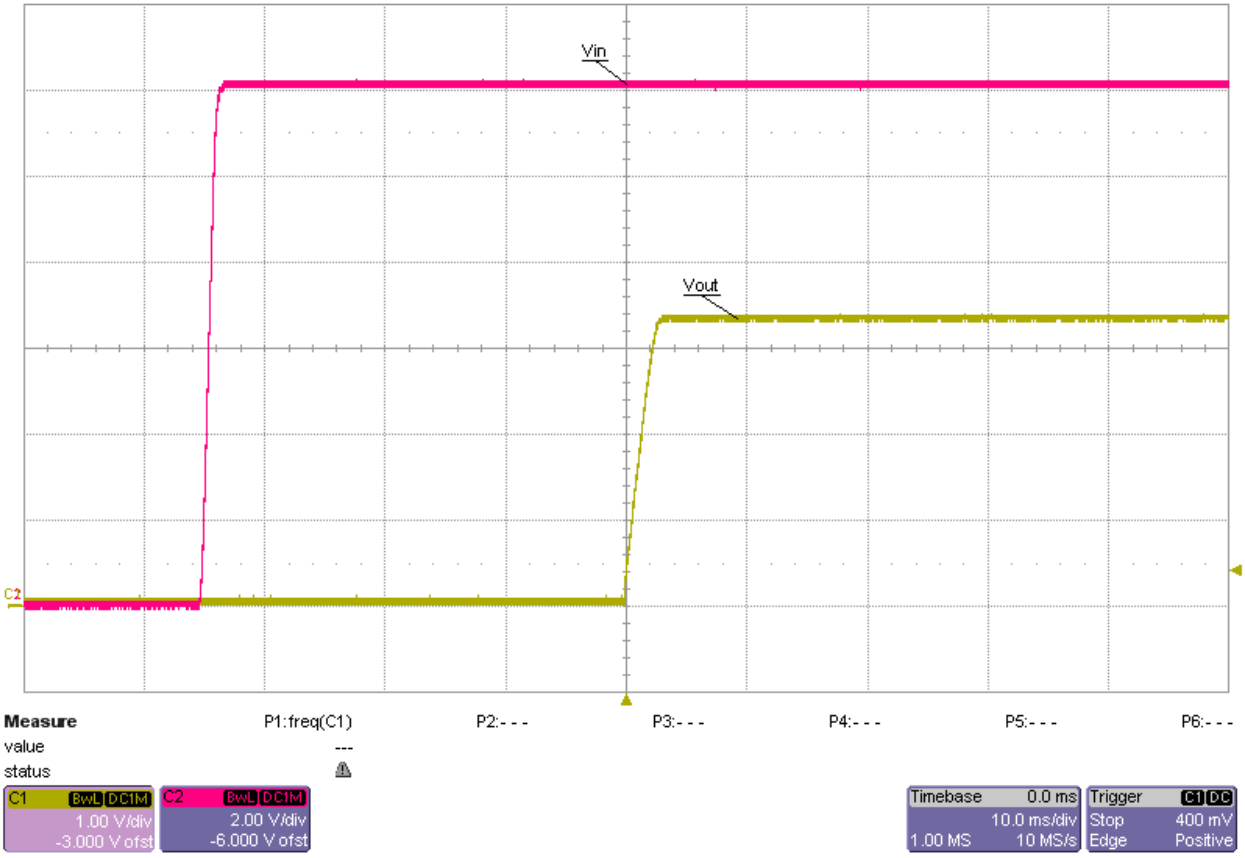
U4 CH1 (1.8V @ 2.5A) Startup into 2.5A Load (all other channel outputs not loaded)



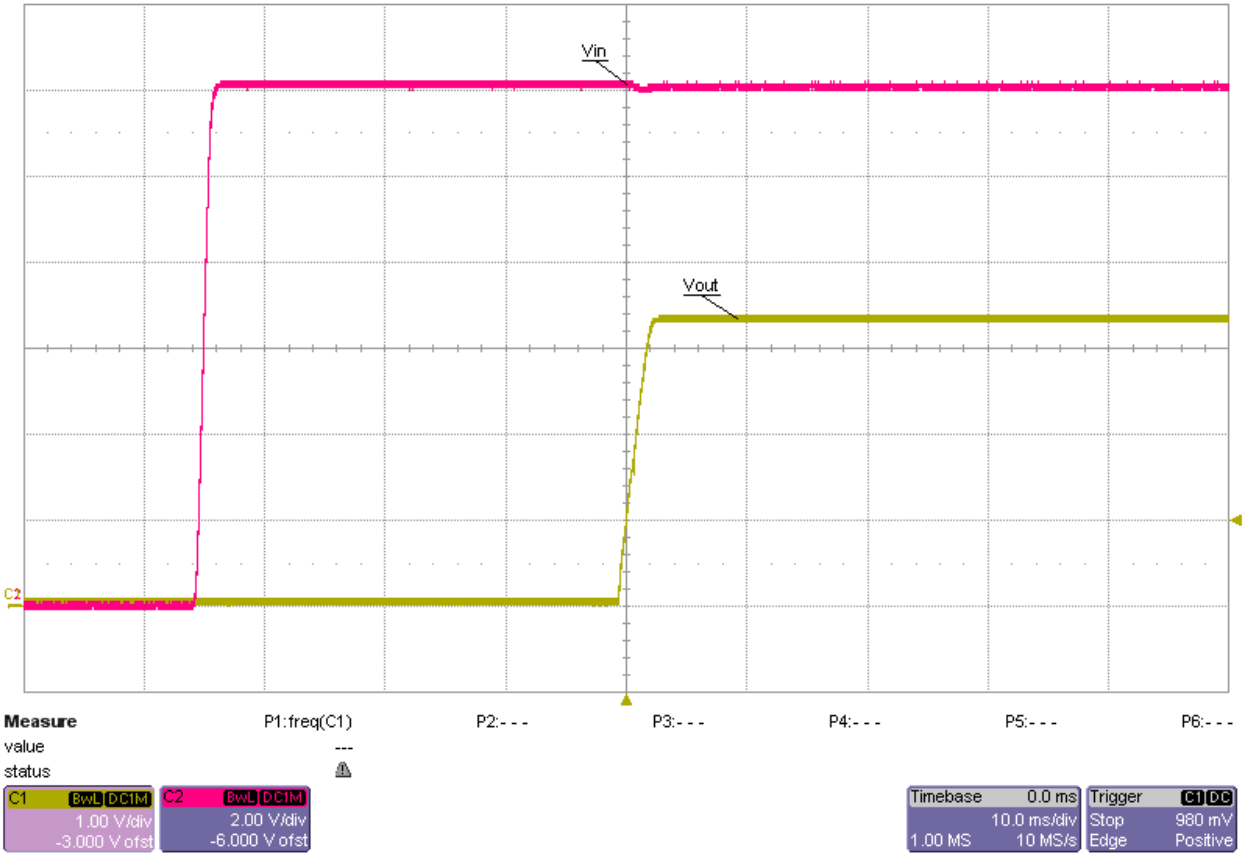
U4 CH2 (1.5V @ 6A) Startup into No Load (all other channel outputs not loaded)



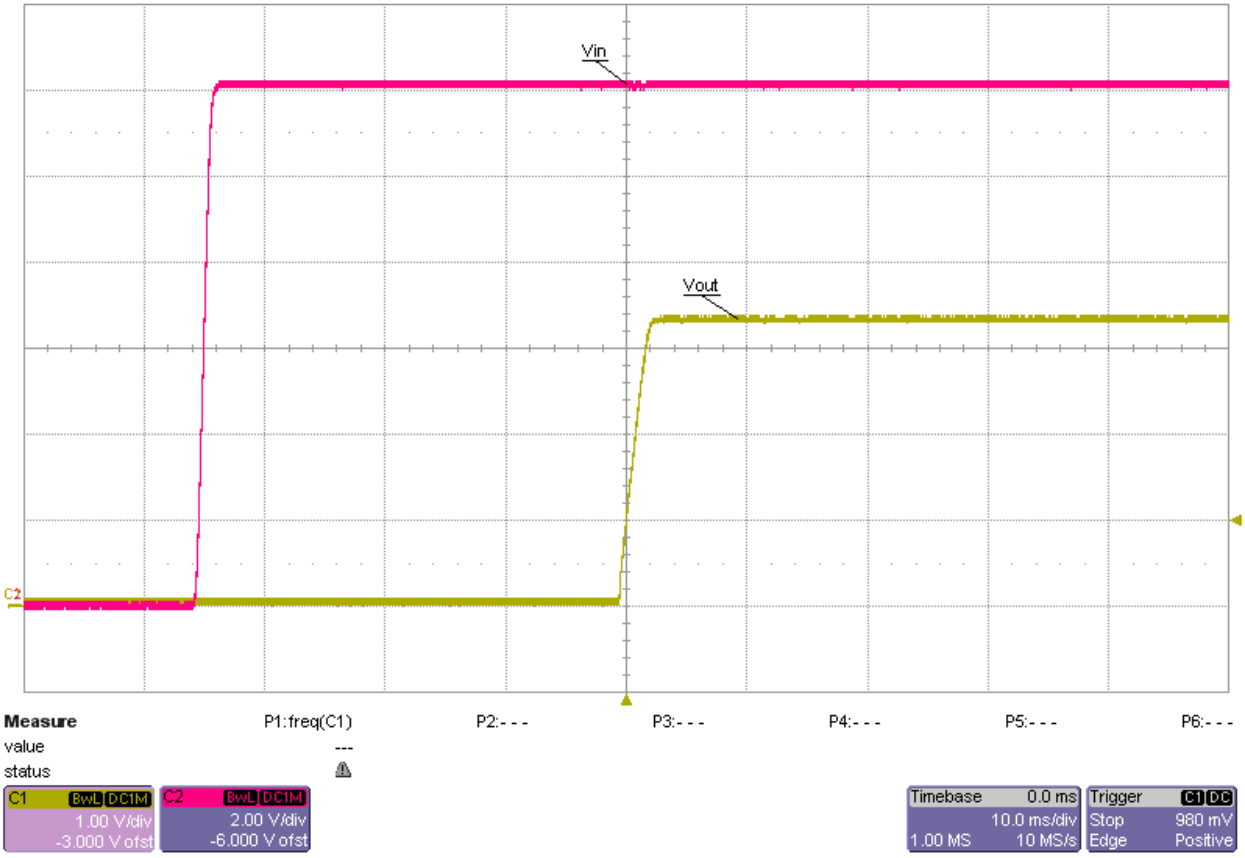
U4 CH2 (1.5V @ 6A) Startup into 6A Load (all other channel outputs not loaded)



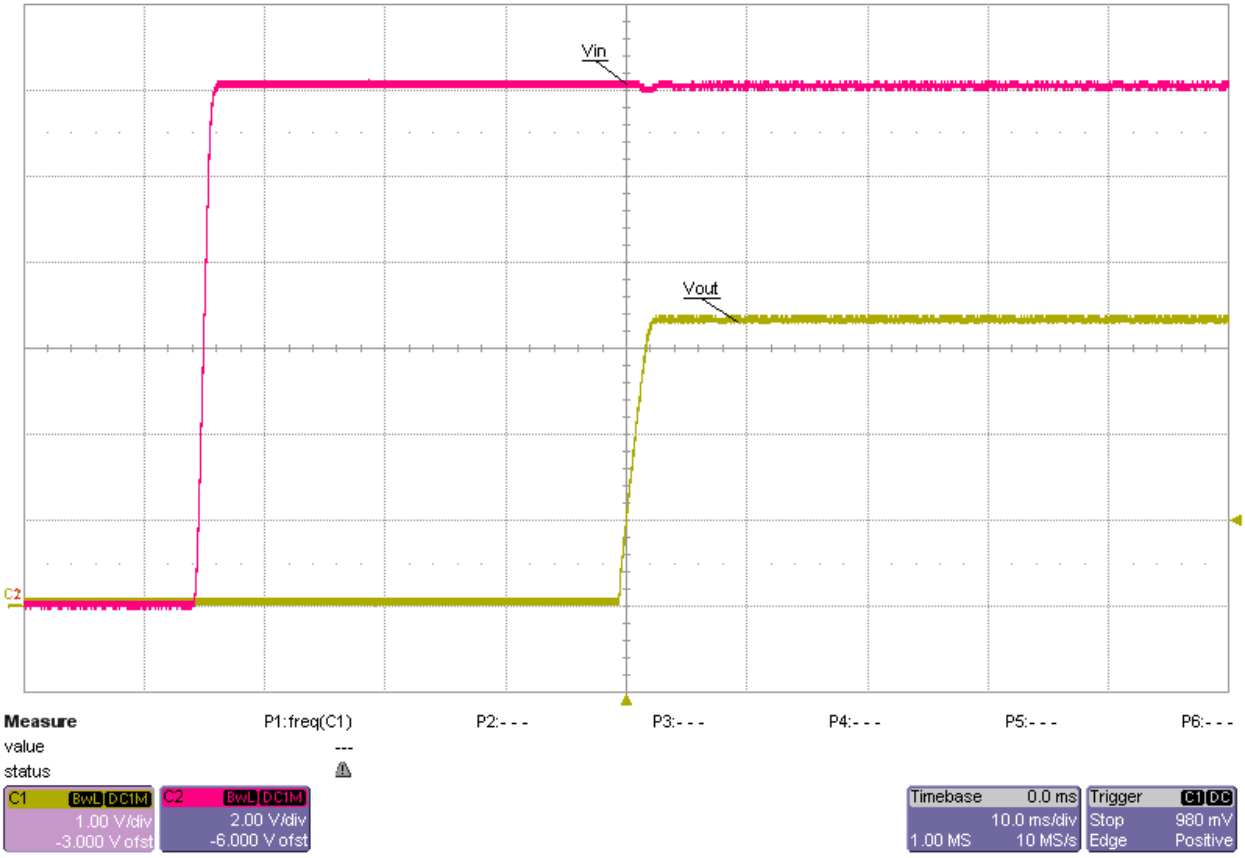
U7 (3.3V @ 5A) Startup into No Load (all other channel outputs not loaded)



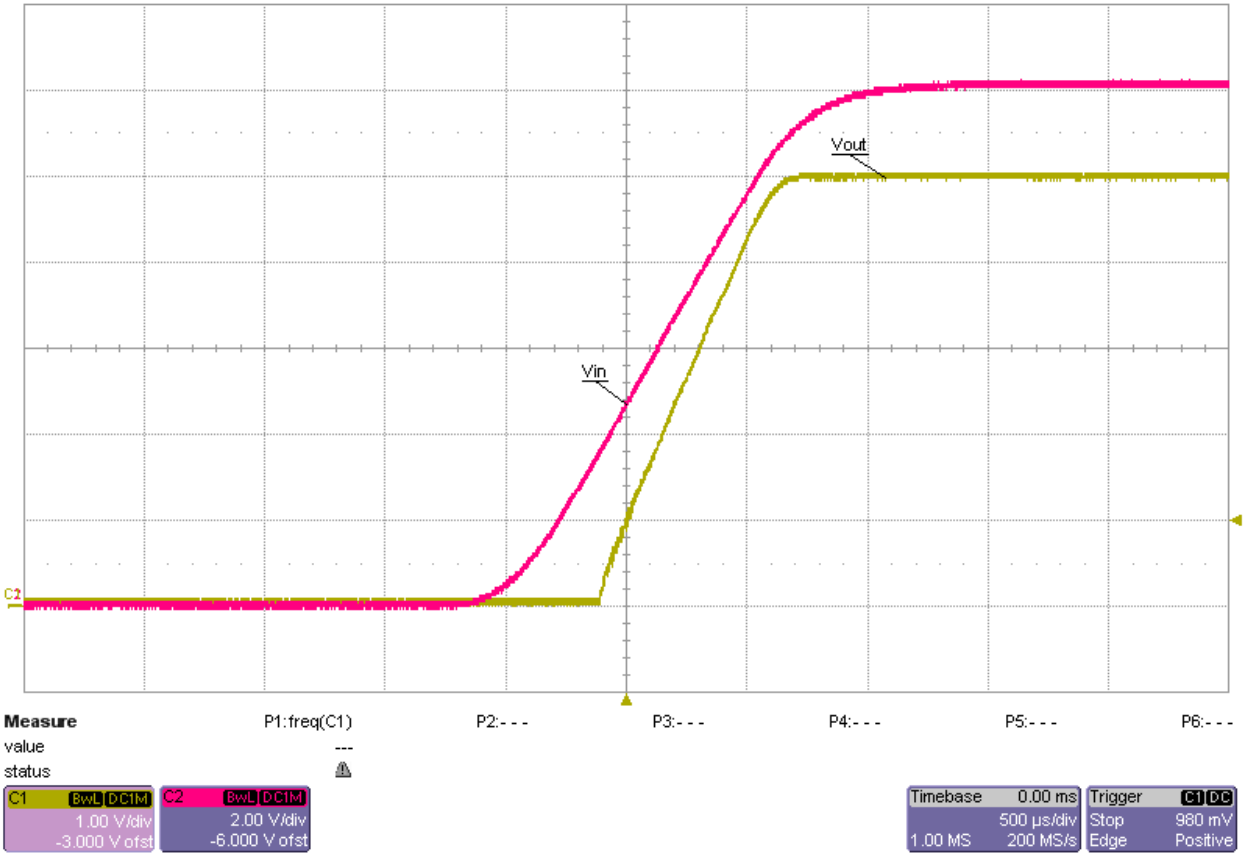
U7 (3.3V @ 5A) Startup into 5A Load (all other channel outputs not loaded)



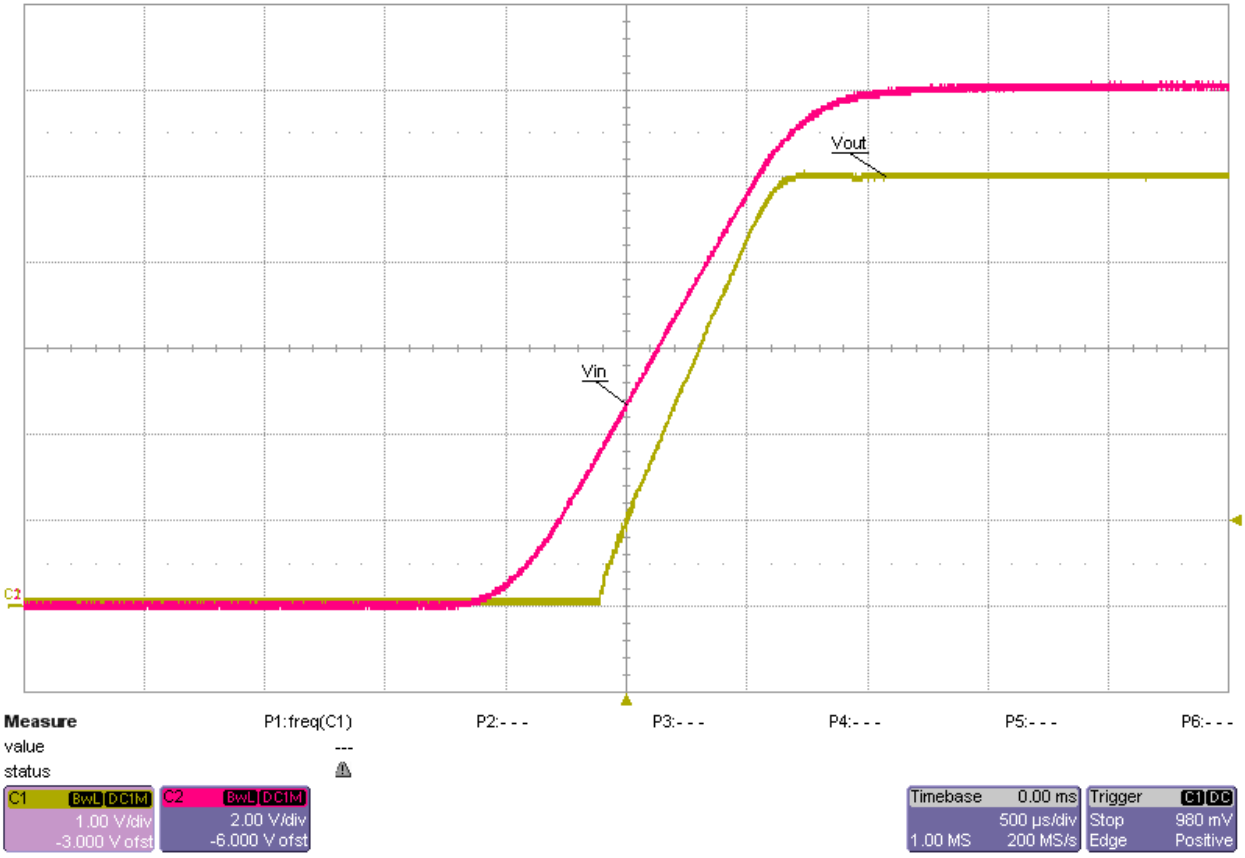
U8 (3.3V @ 5A) Startup into No Load (all other channel outputs not loaded)



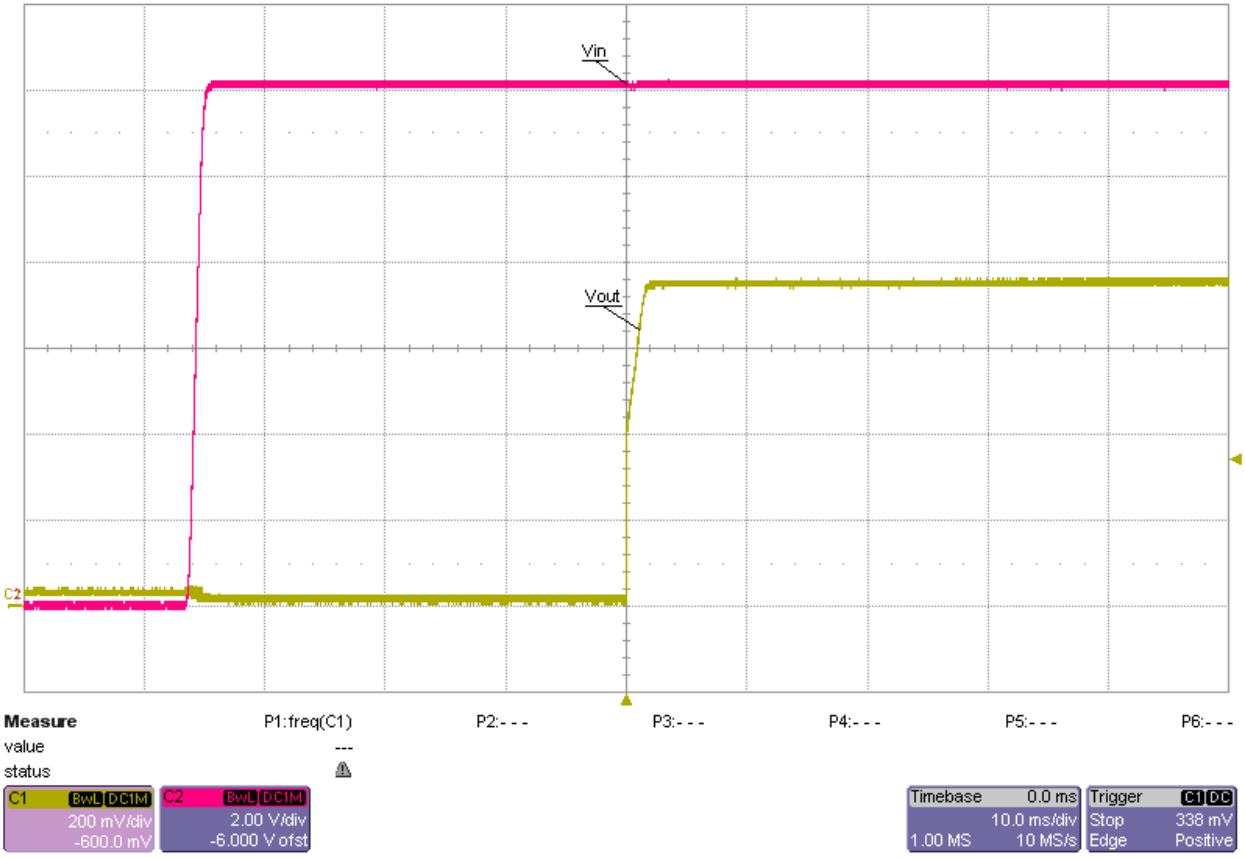
U8 (3.3V @ 5A) Startup into 5A Load (all other channel outputs not loaded)



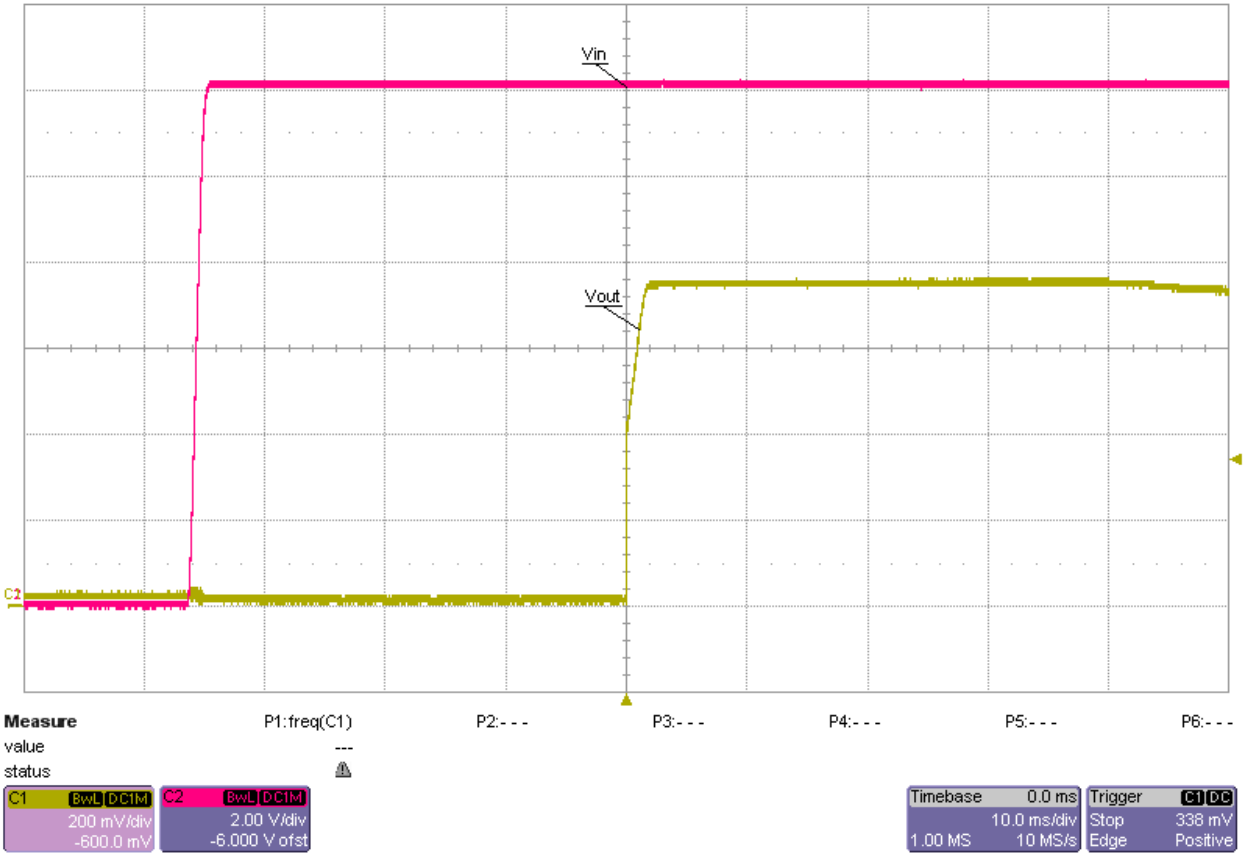
U6 (5V @ 2A) Startup into No Load (all other channel outputs not loaded)



U6 (5V @ 2A) Startup into 2A Load (all other channel outputs not loaded)

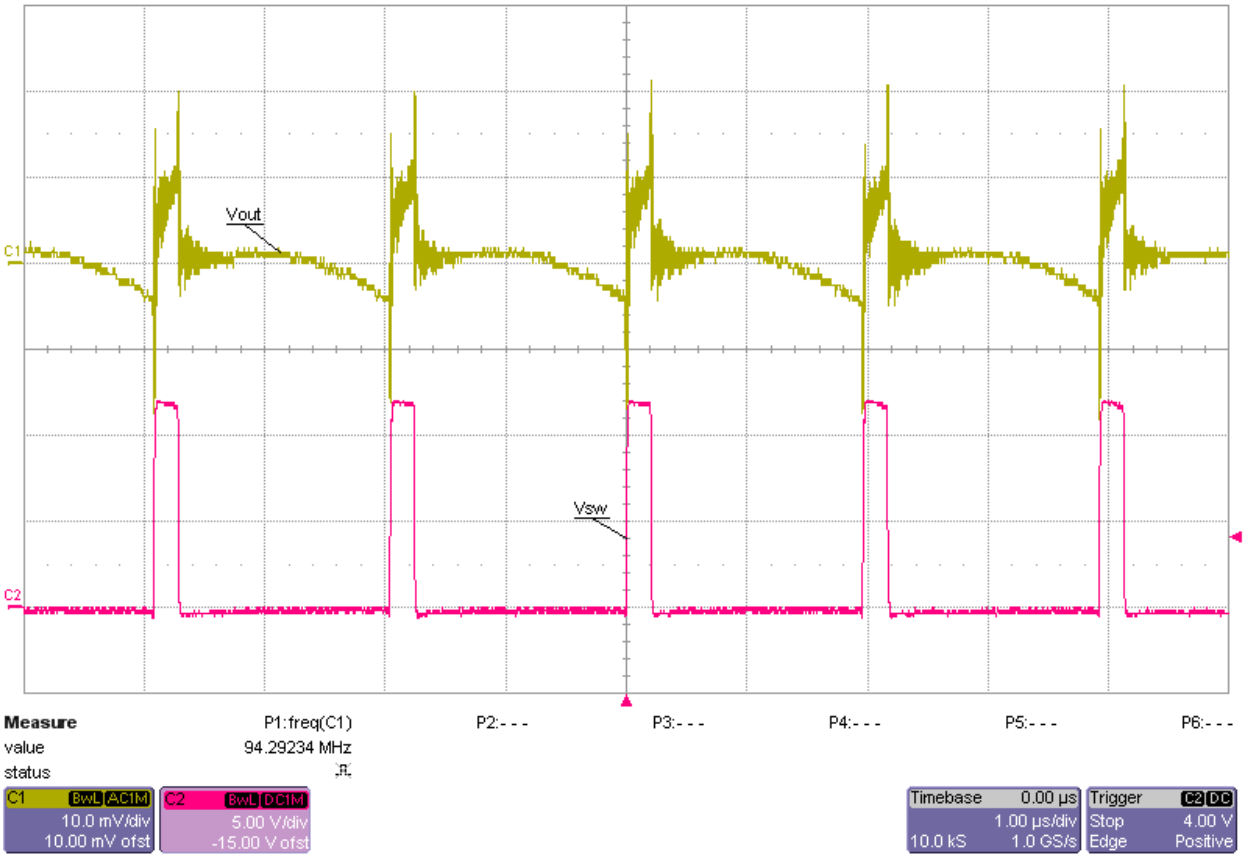


U5 (0.75V @ 1A continuous; 3A peak) Startup into No Load (all other channel outputs not loaded)

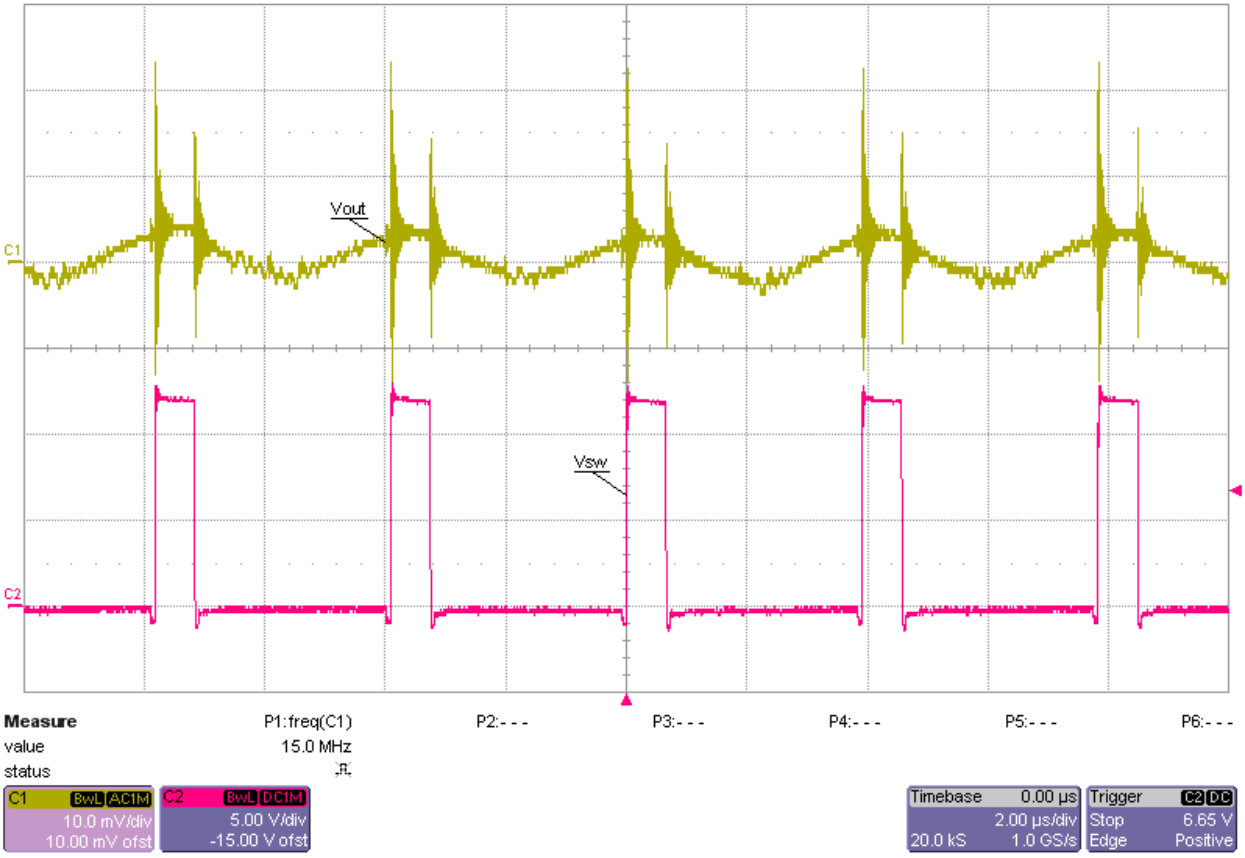


U5 (0.75V @ 1A continuous; 3A peak) Startup into 1A Load (all other channel outputs not loaded)

Output Voltage Ripple

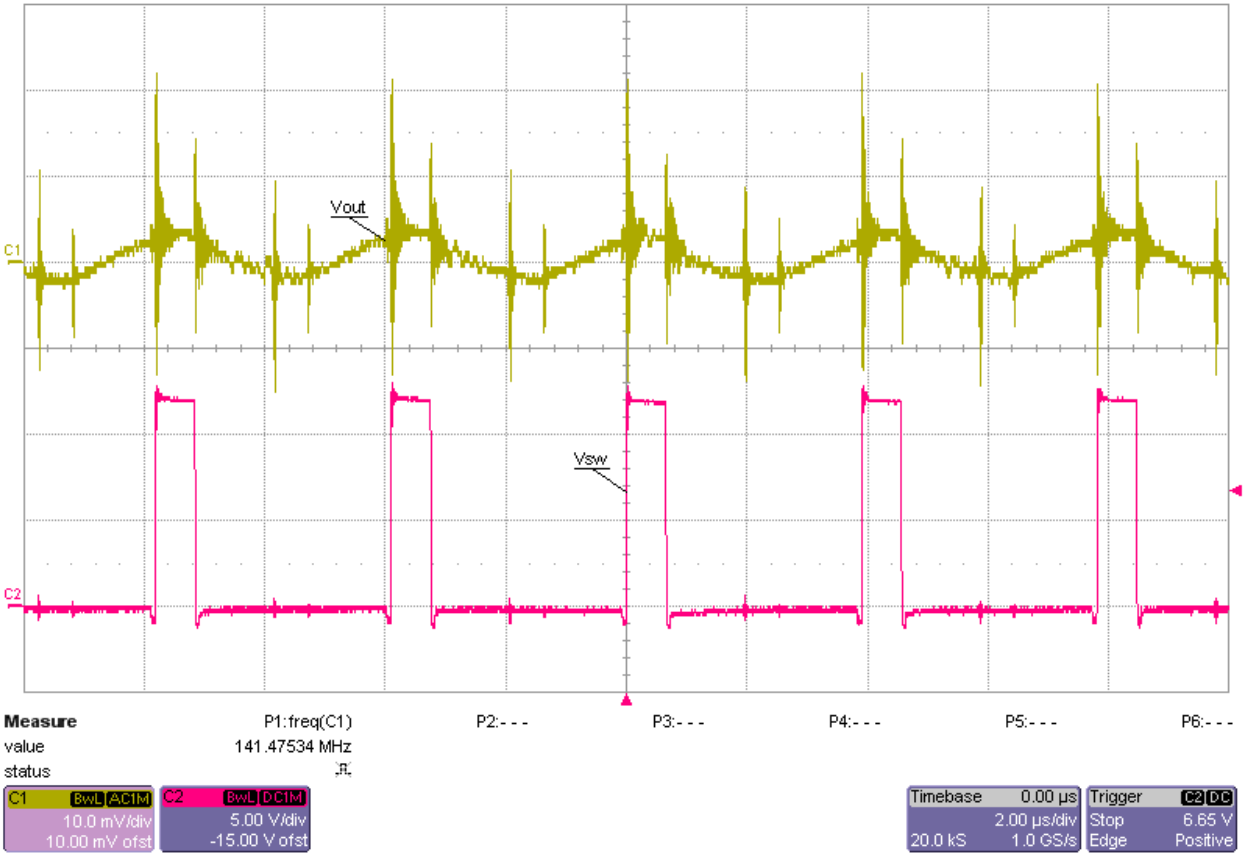


U2 (1V @ 5A) Output Voltage Ripple at 5A Load (Vripple ≈ 10mV)



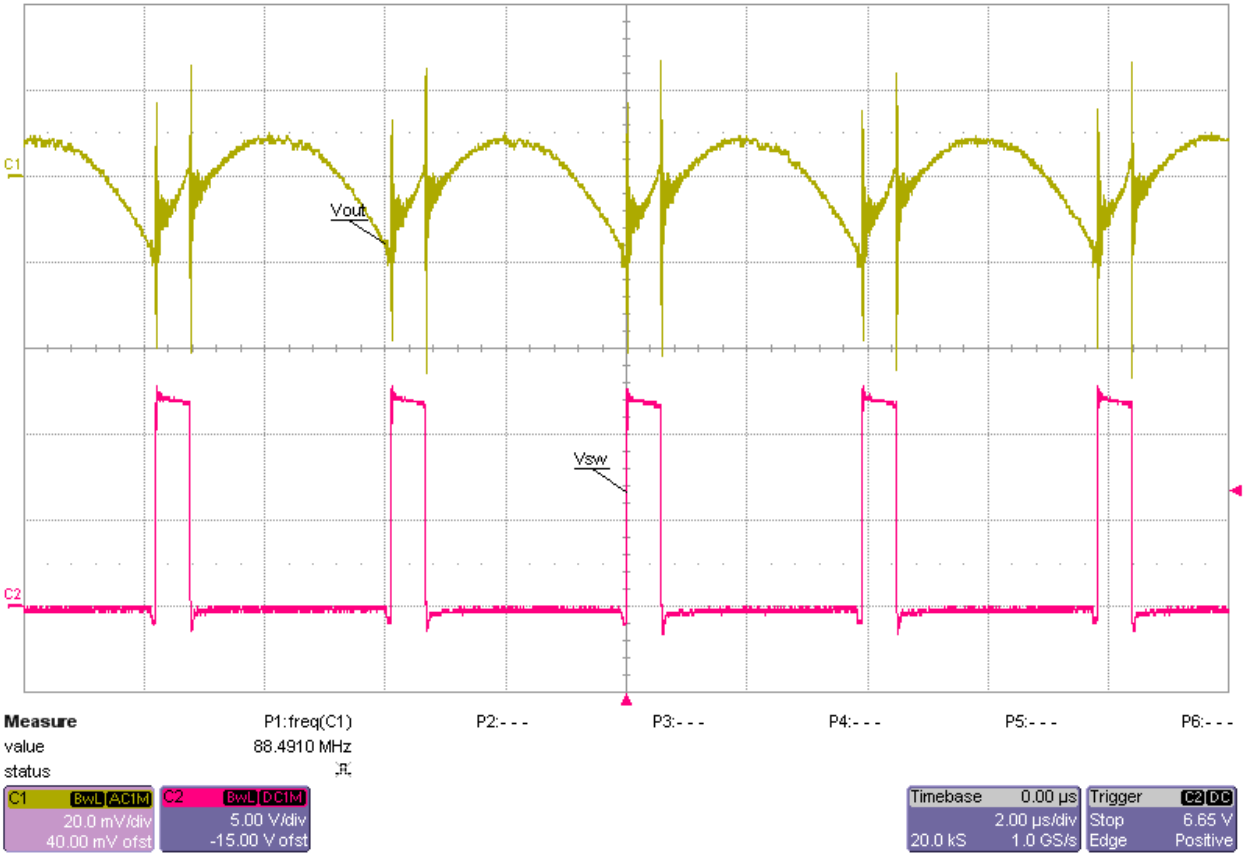
U4 CH1 (1.8V @ 2.5A) Output Voltage Ripple at 2.5A Load (while U4 CH2 output not loaded)

(Vripple ≈ 10mV)



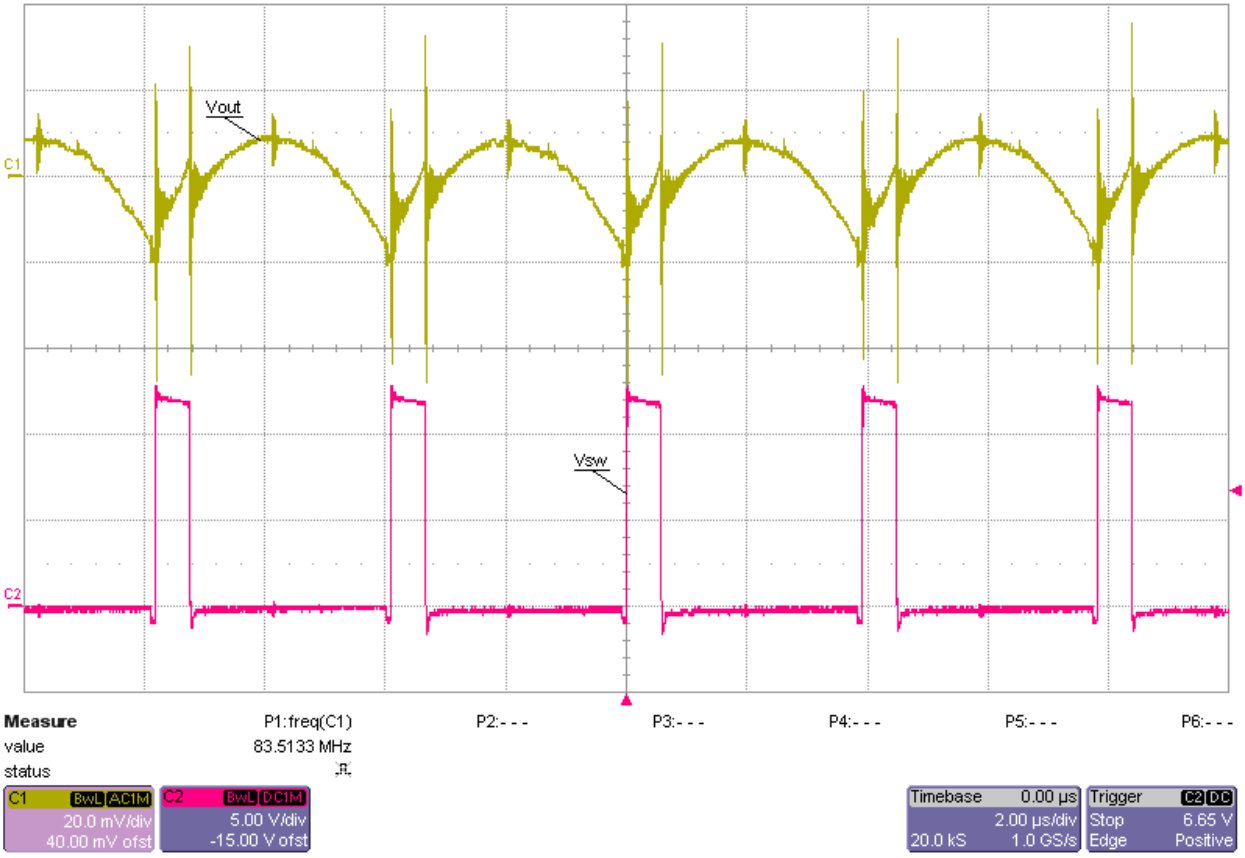
U4 CH1 (1.8V @ 2.5A) Output Voltage Ripple at 2.5A Load (while U4 CH2 output loaded at 6A)

(Vripple ≈ 10mV)



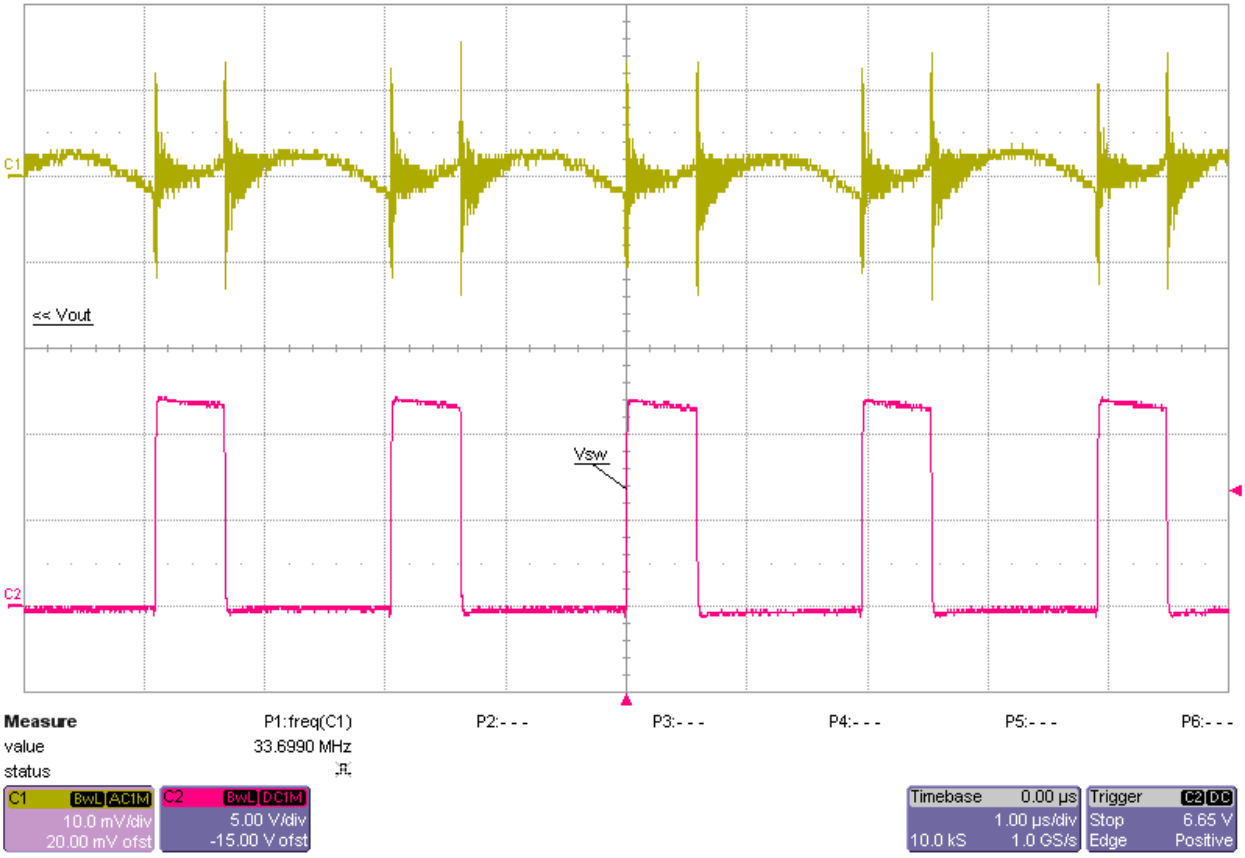
U4 CH2 (1.5V @ 6A) Output Voltage Ripple at 6A Load (while U4 CH1 output not loaded)

(Vripple ≈ 28mV)

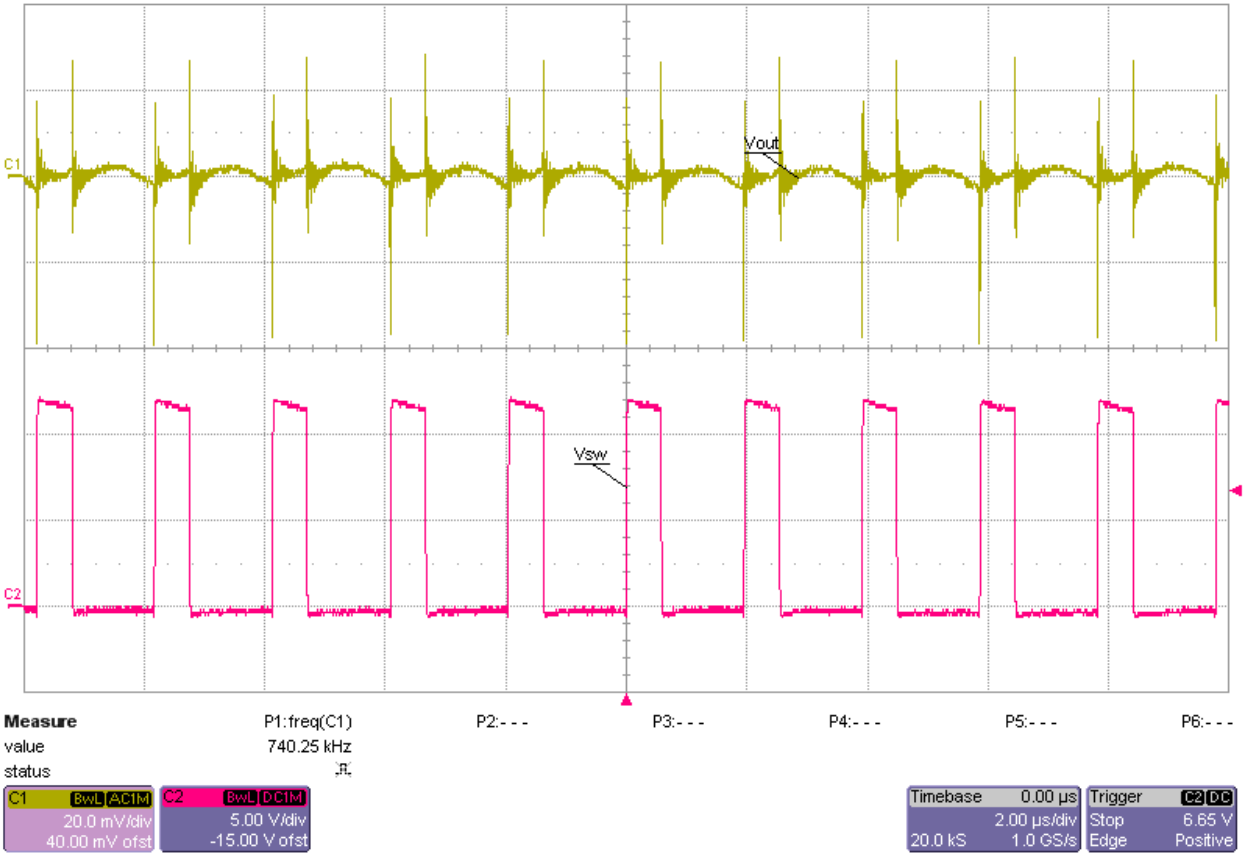


U4 CH2 (1.5V @ 6A) Output Voltage Ripple at 6A Load (while U4 CH1 output loaded at 2.5A)

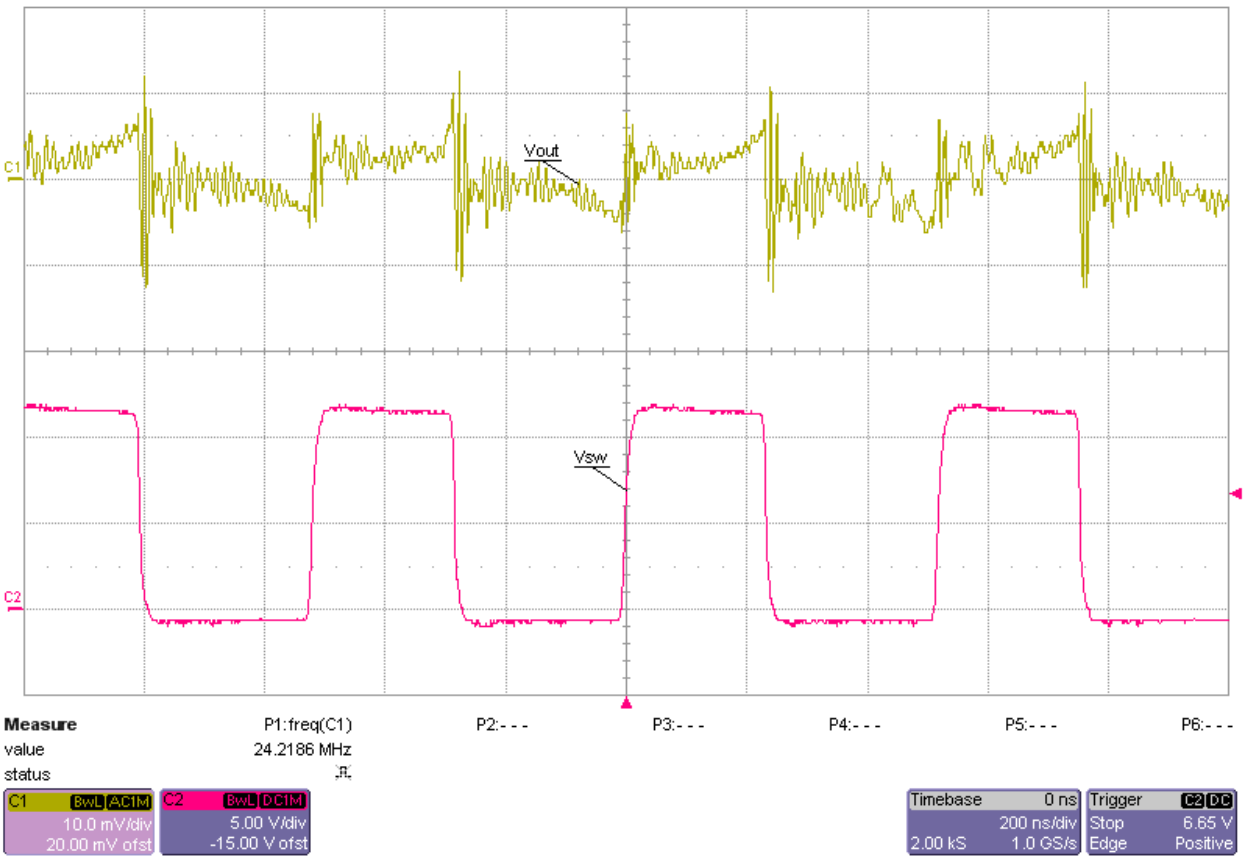
(Vripple ≈ 28mV)



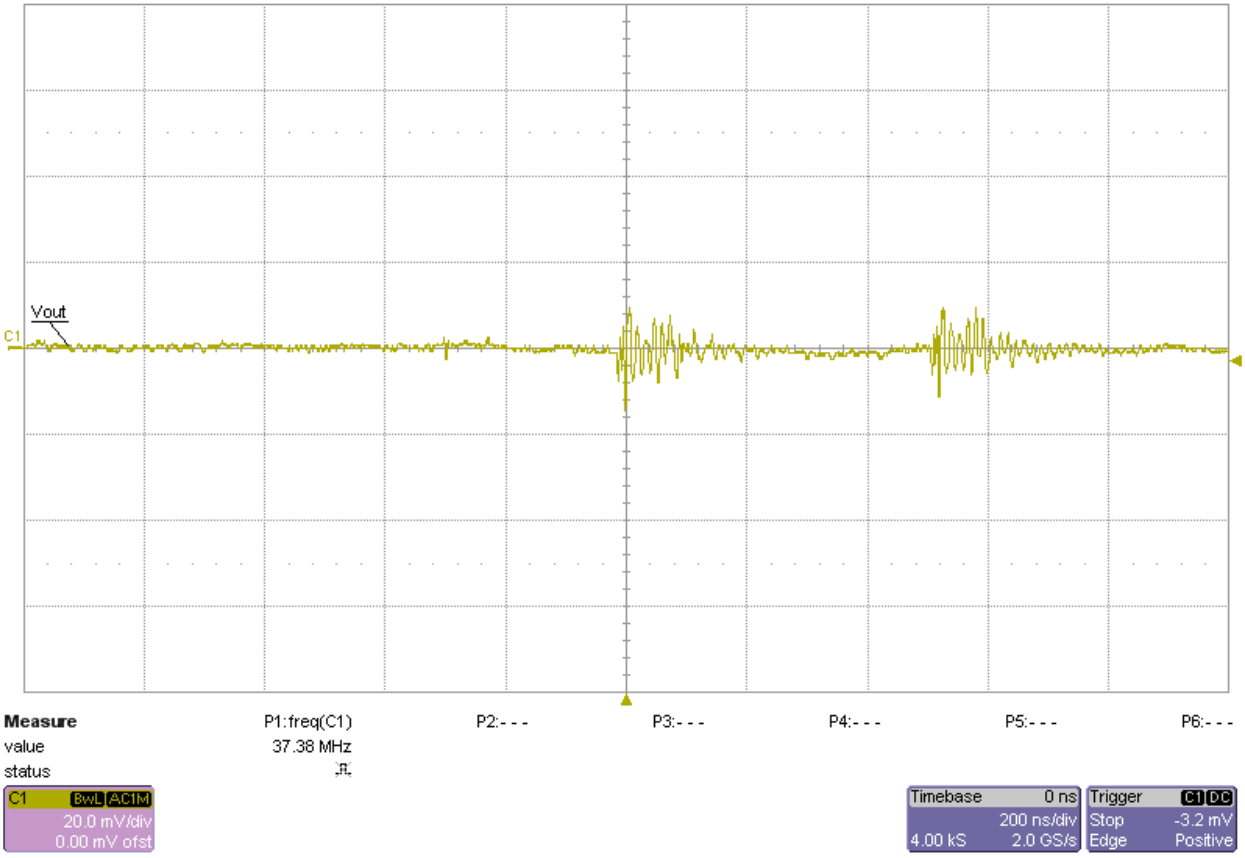
U7 (3.3V @ 5A) Output Voltage Ripple at 5A Load (Vripple ≈ 8mV)



U8 (3.3V @ 5A) Output Voltage Ripple at 5A Load (Vripple ≈ 8mV)

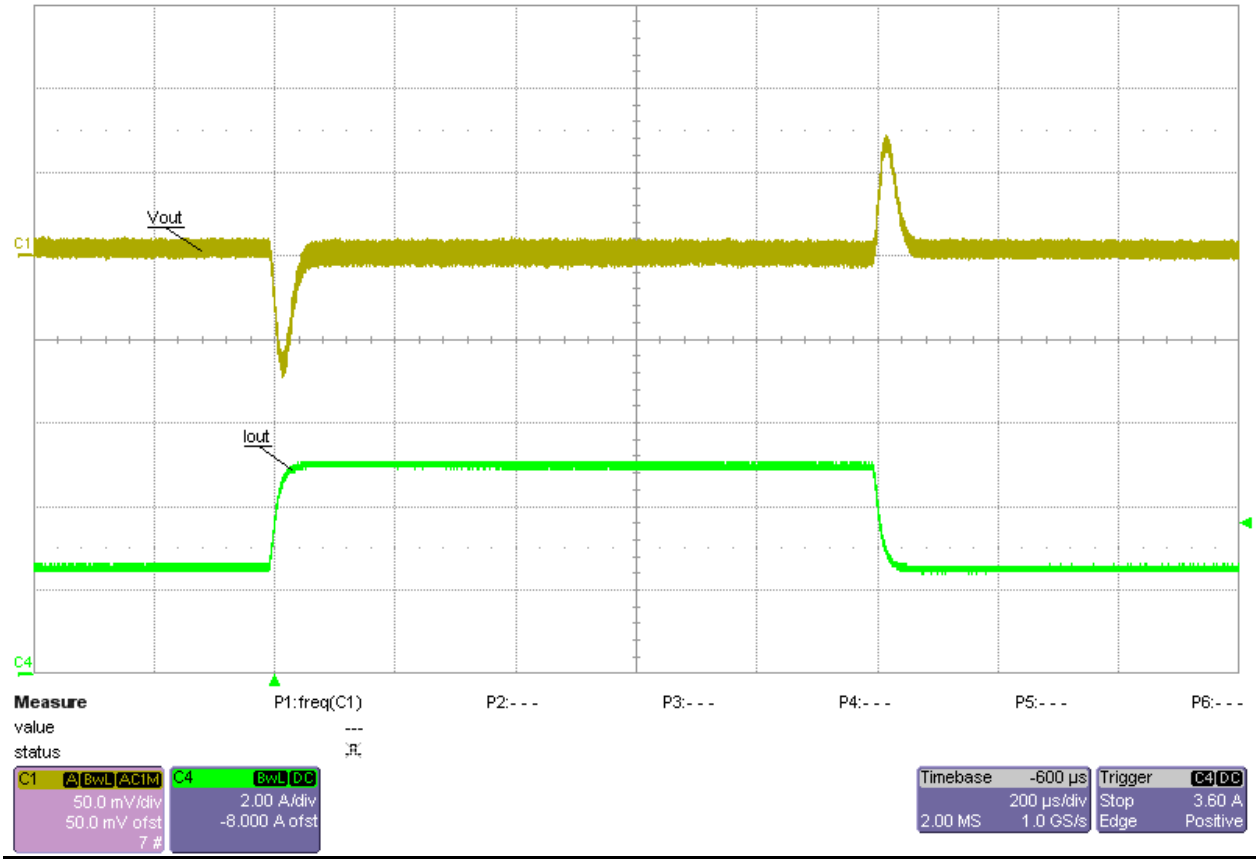


U6 (5V @ 2A) Output Voltage Ripple at 2A Load (Vripple ≈ 20mV)

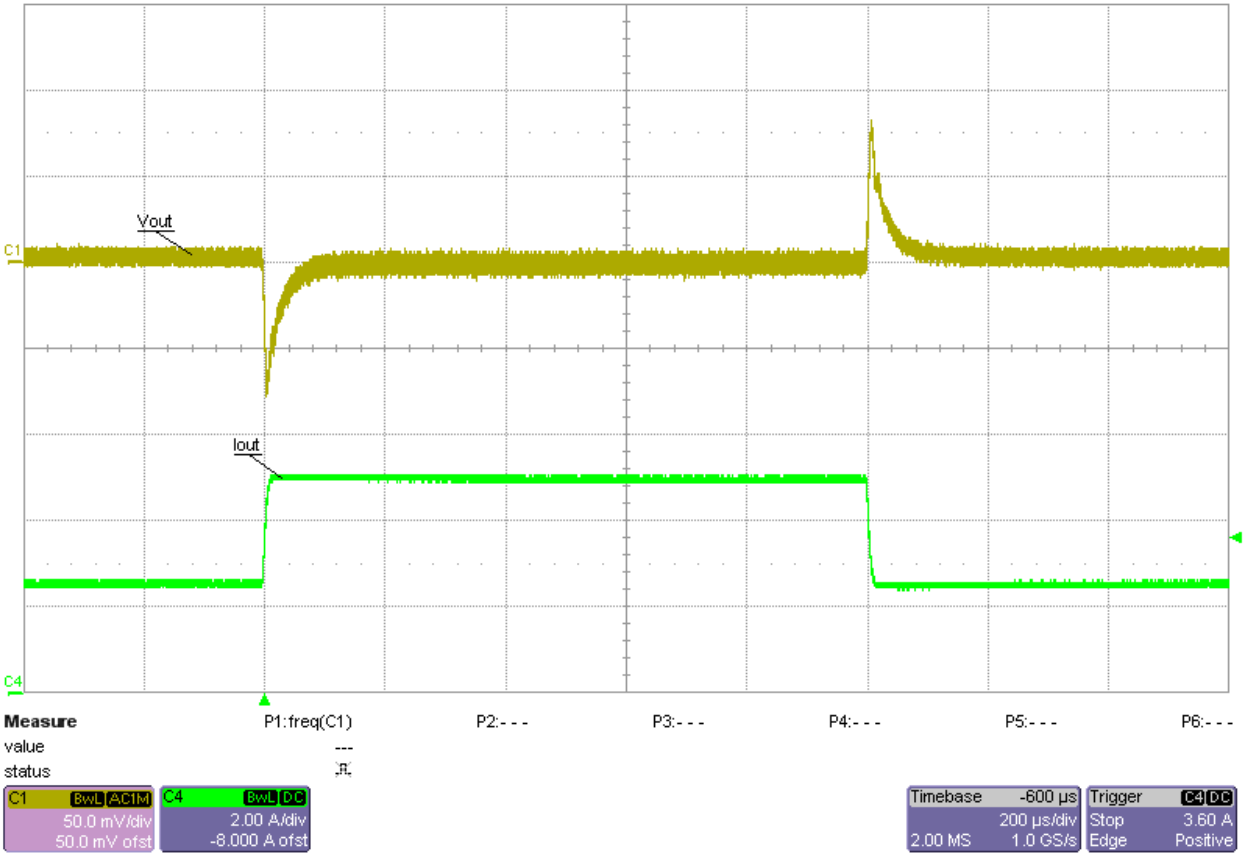


U5 (0.75V @ 1A continuous; 3A peak) Output Voltage Ripple at 1A Load (while U6 output not loaded) (Vripple ≈ 15mV)

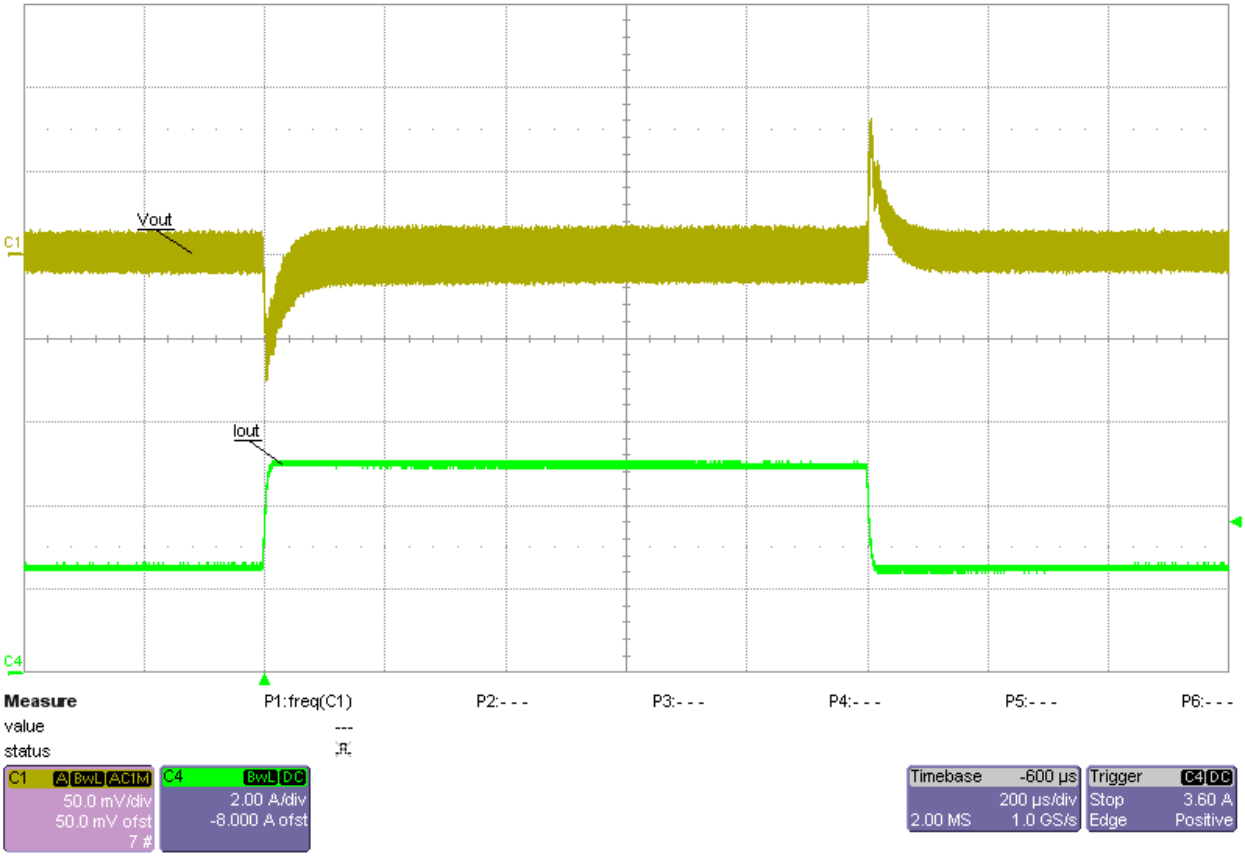
Load Transient Response



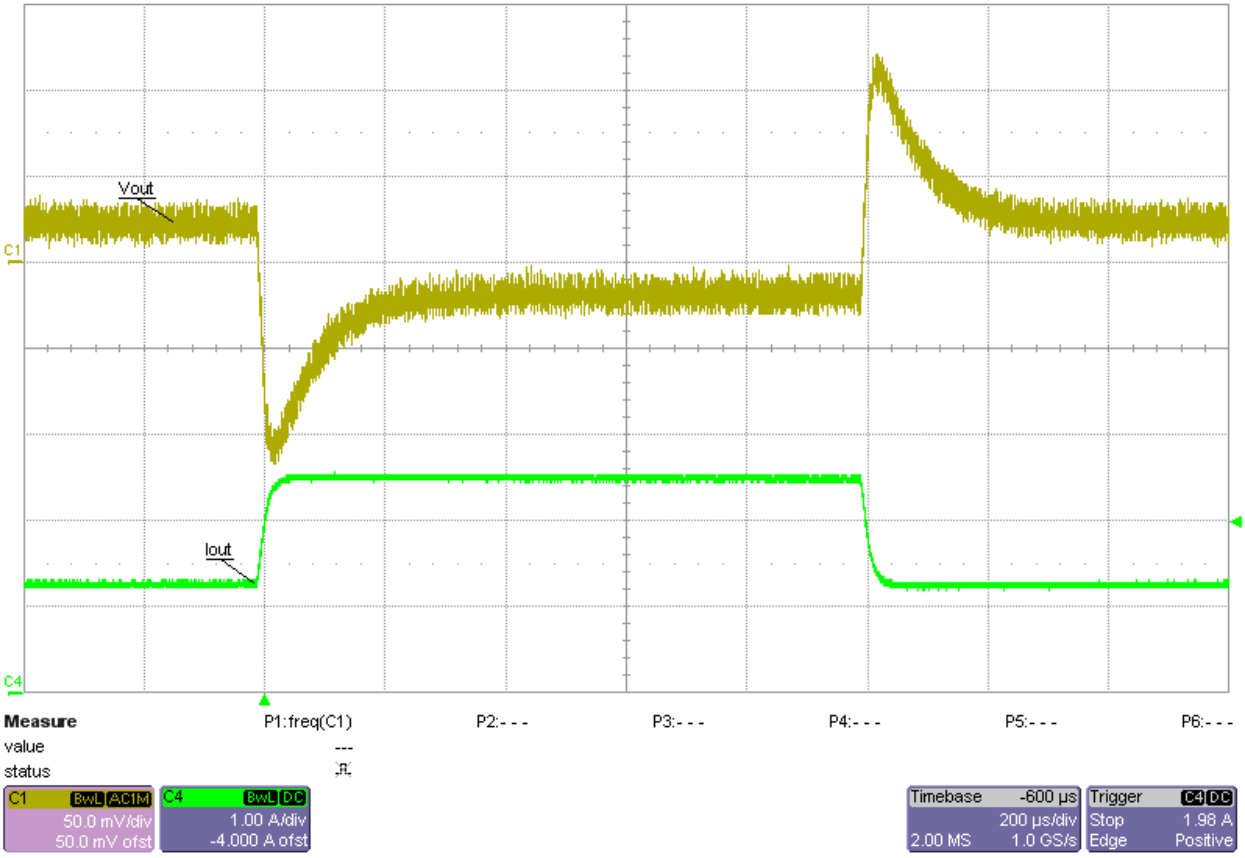
U2 (1V @ 5A) Output Load Transient Response (50%-to-100% Load Step)



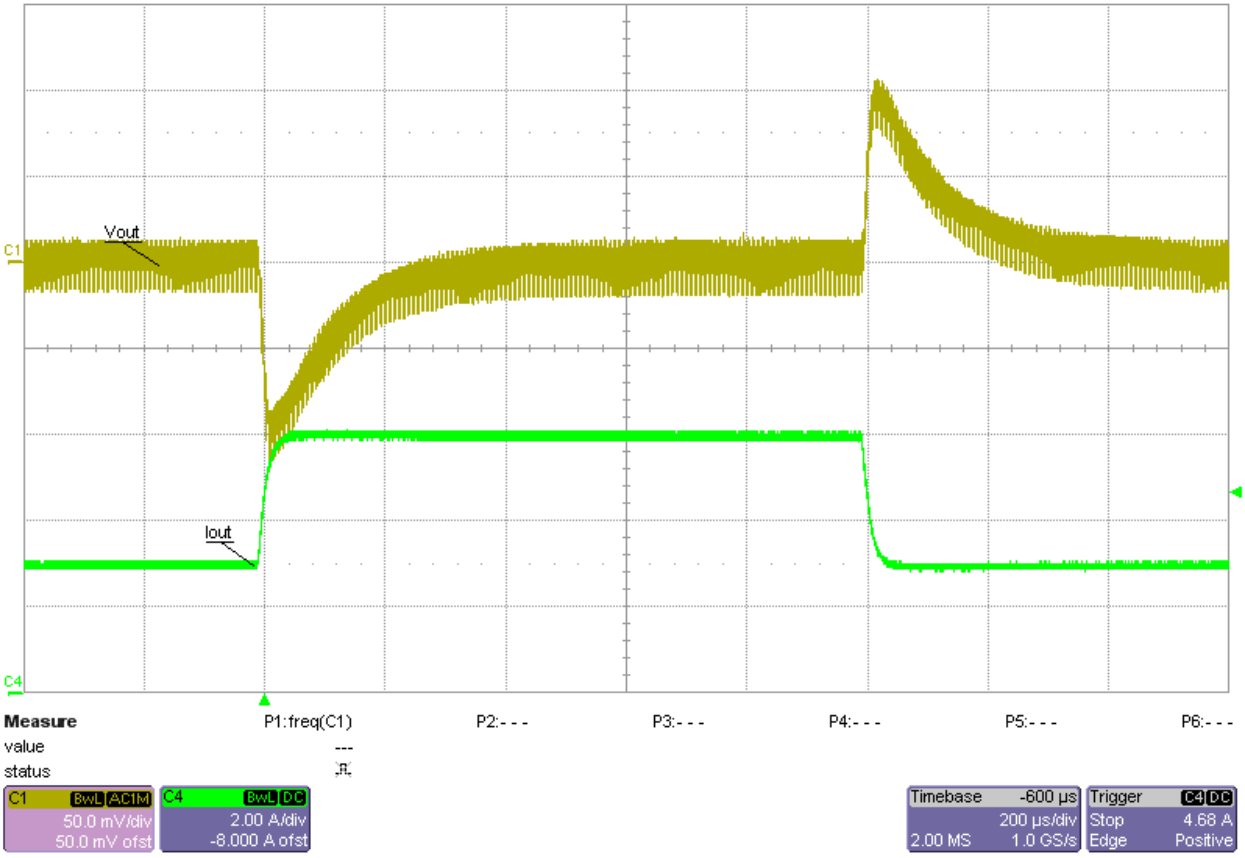
U7 (3.3V @ 5A) Output Load Transient Response (50%-to-100% Load Step)



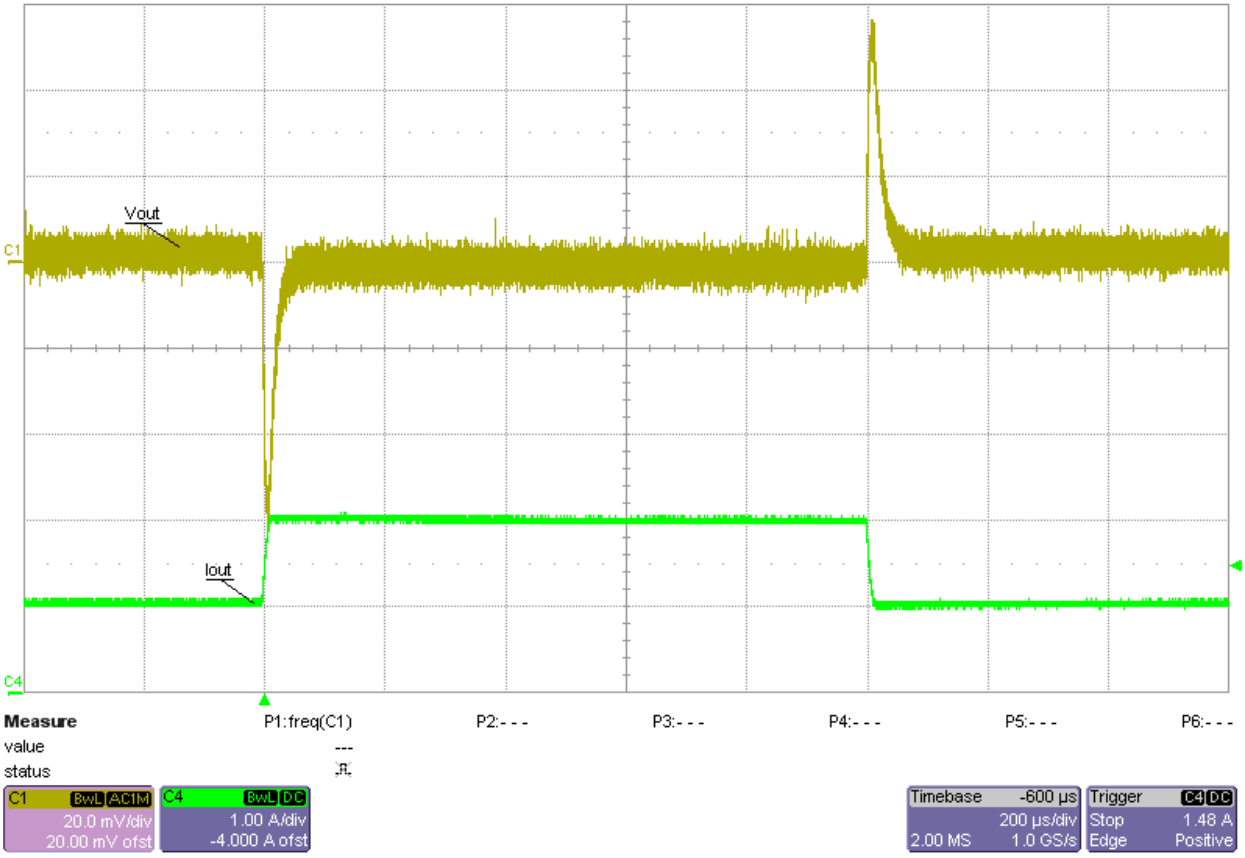
U8 (3.3V @ 5A) Output Load Transient Response (50%-to-100% Load Step)



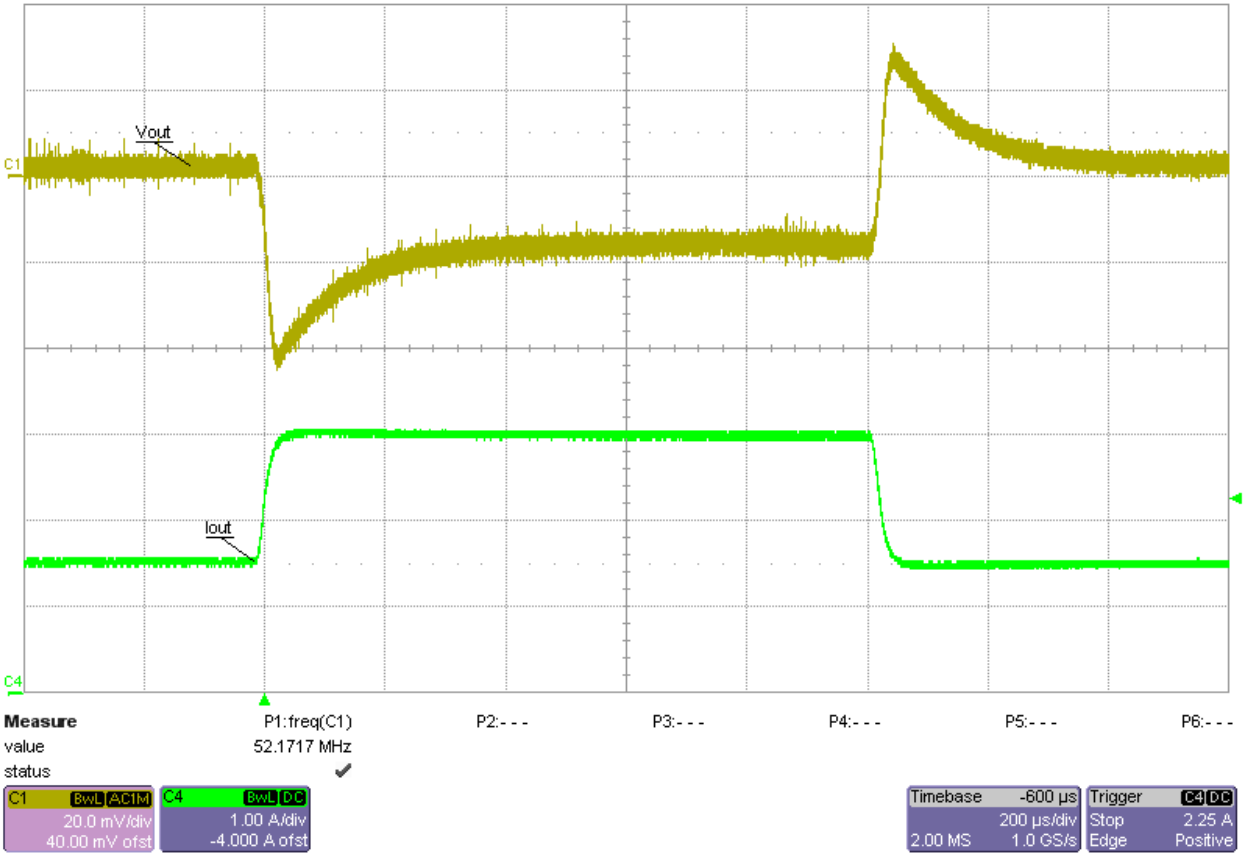
U4 CH1 (1.8V @ 2.5A) Output Load Transient Response (50%-to-100% Load Step)



U4 CH2 (1.5V @ 6A) Output Load Transient Response (50%-to-100% Load Step)

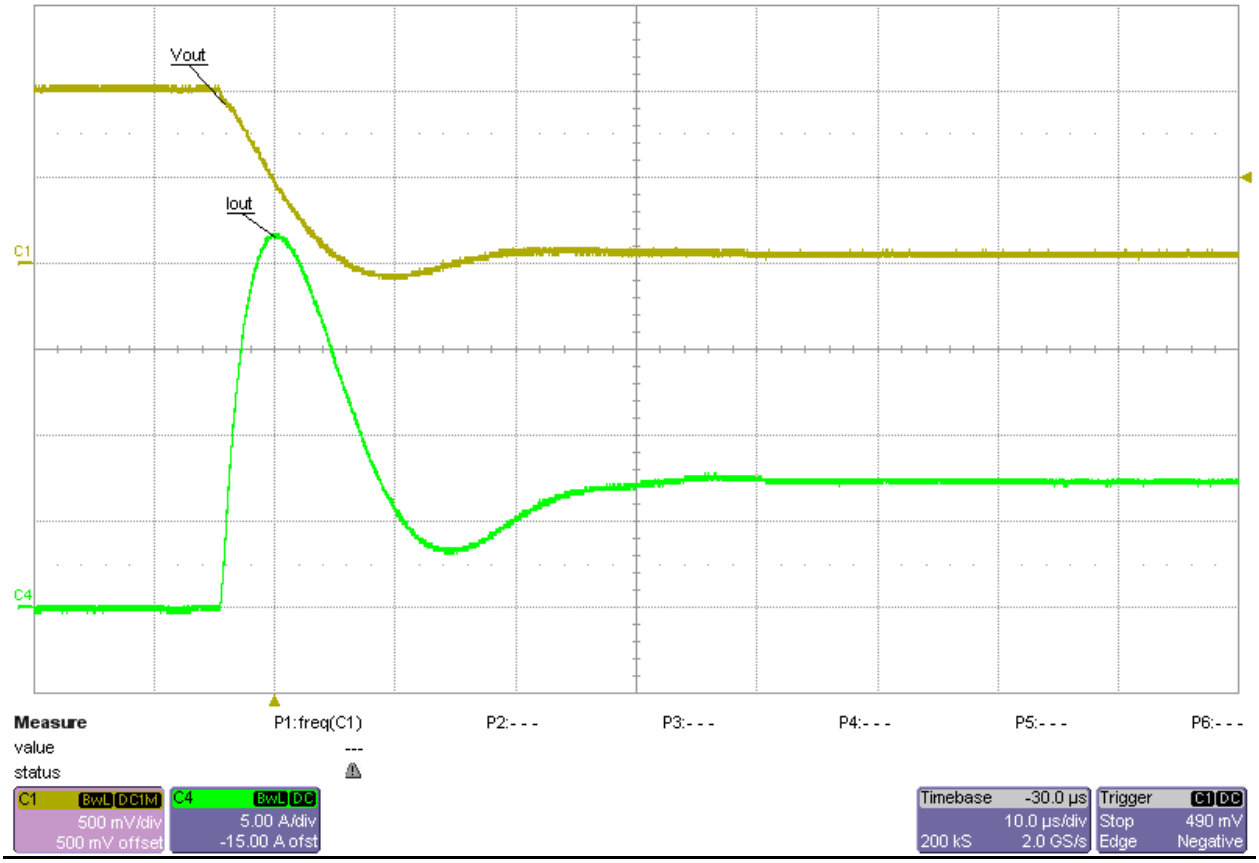


U6 (5V @ 2A) Output Load Transient Response (50%-to-100% Load Step)

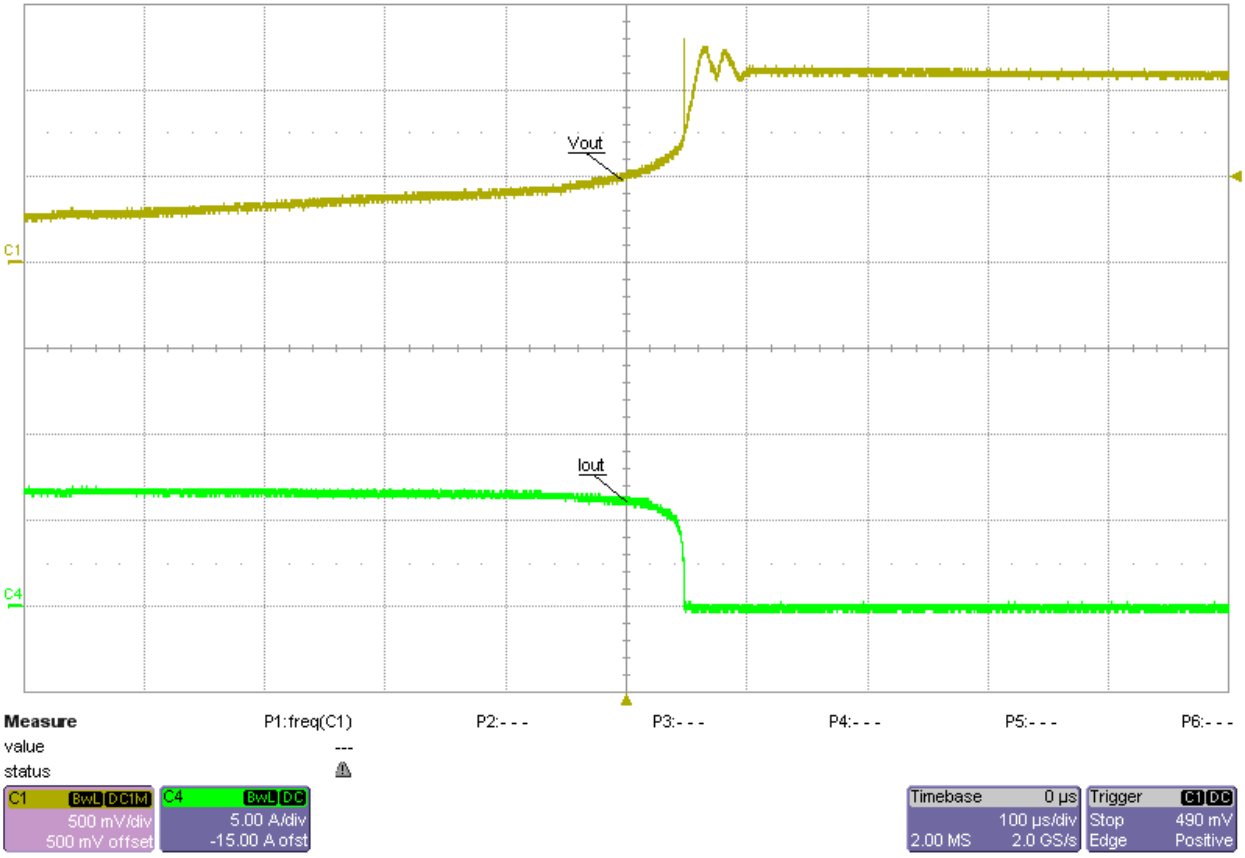


U5 (0.75V @ 1A continuous; 3A peak) Output Load Transient Response (50%-to-100% Load Step)

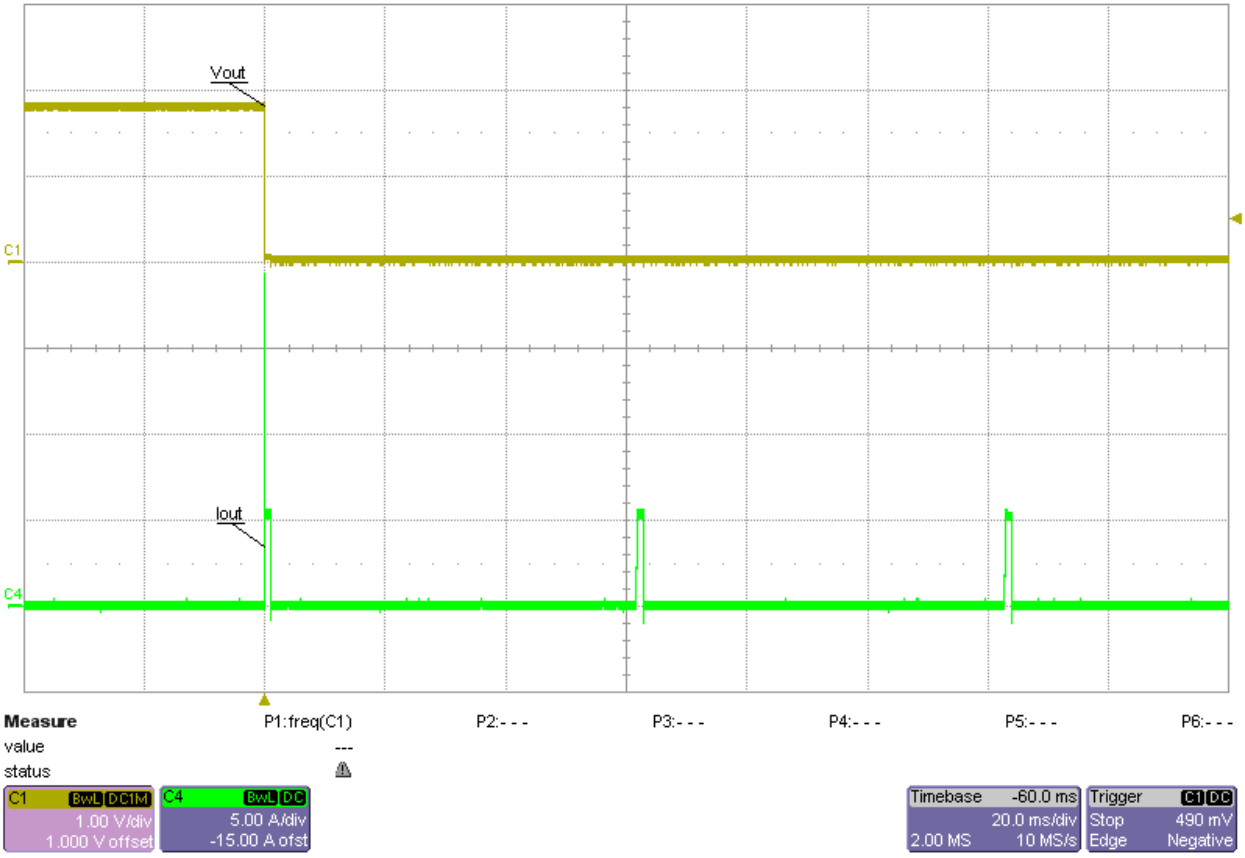
Short Circuit Testing



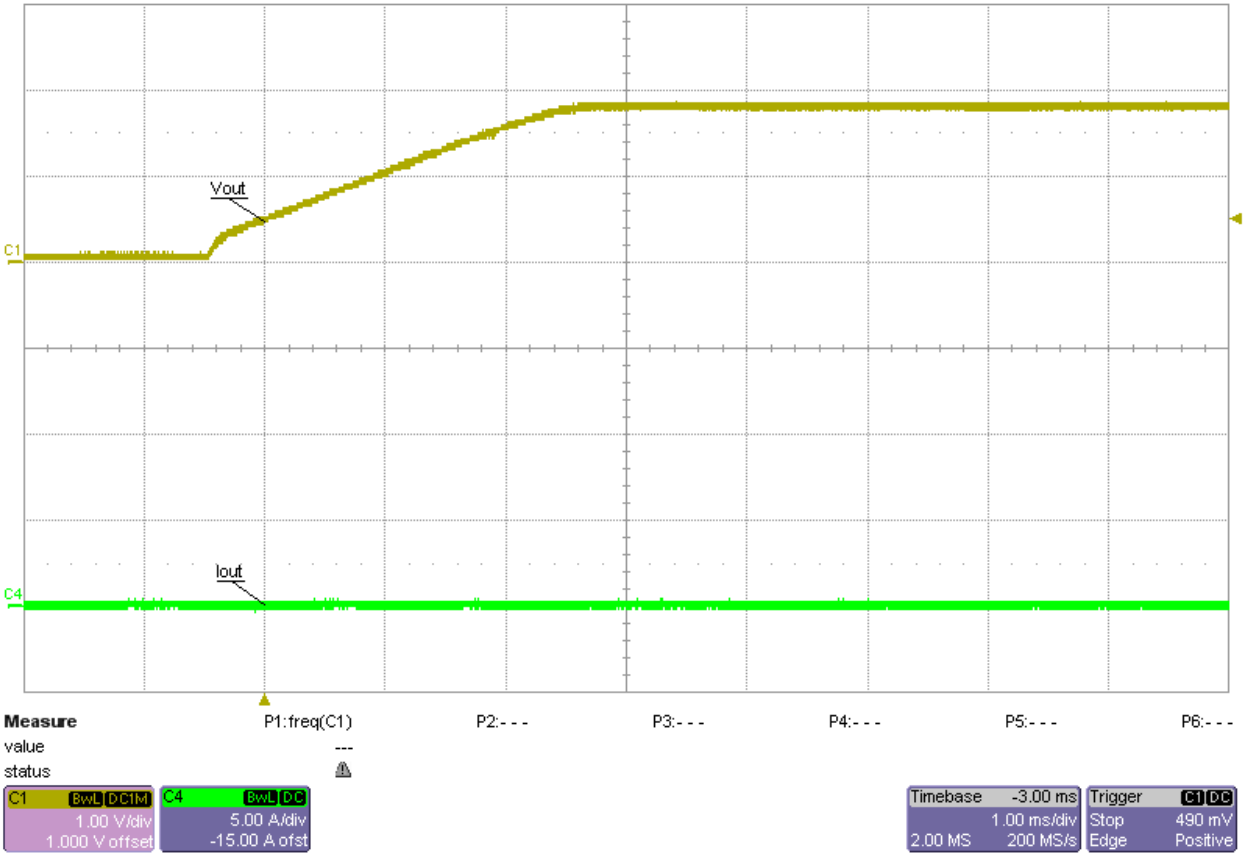
U2 (1V @ 5A) Output Short Circuit



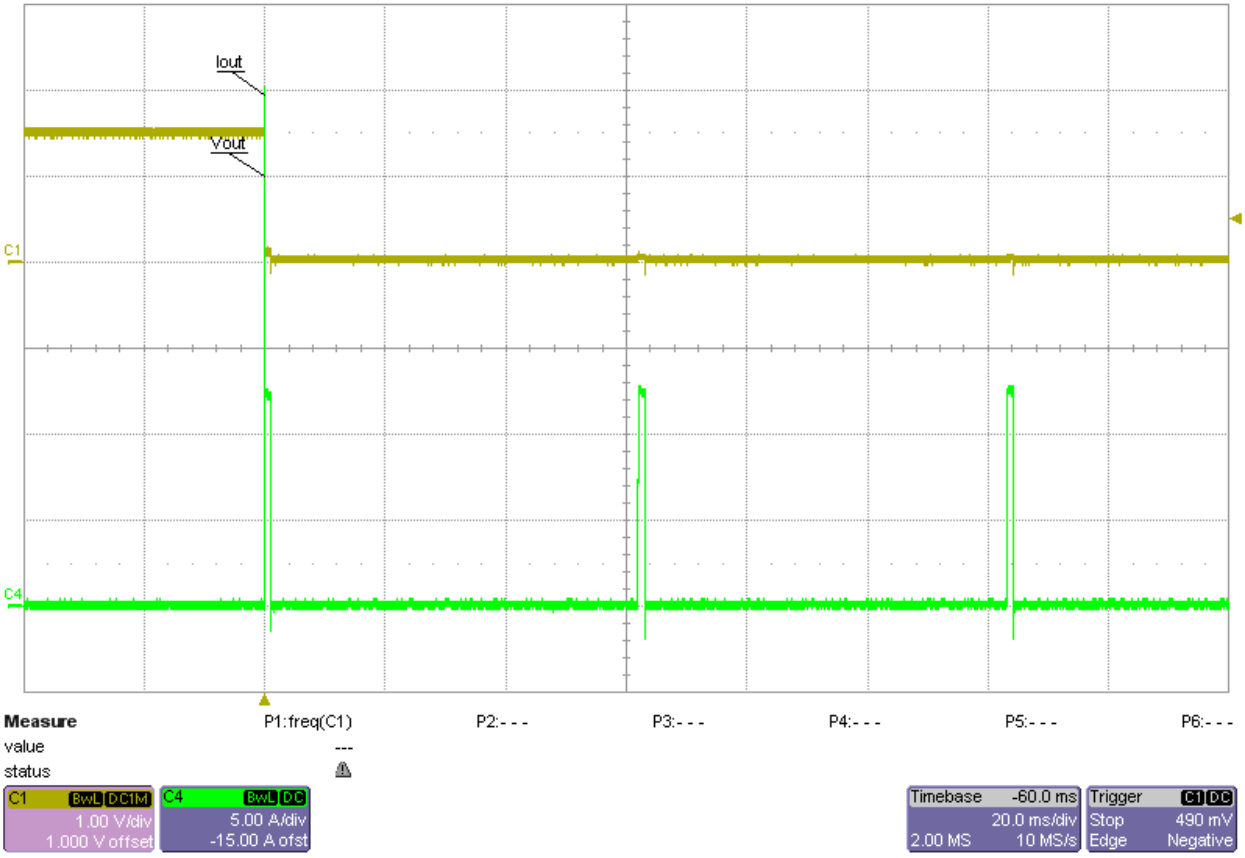
U2 (1V @ 5A) Output Short Circuit Recovery



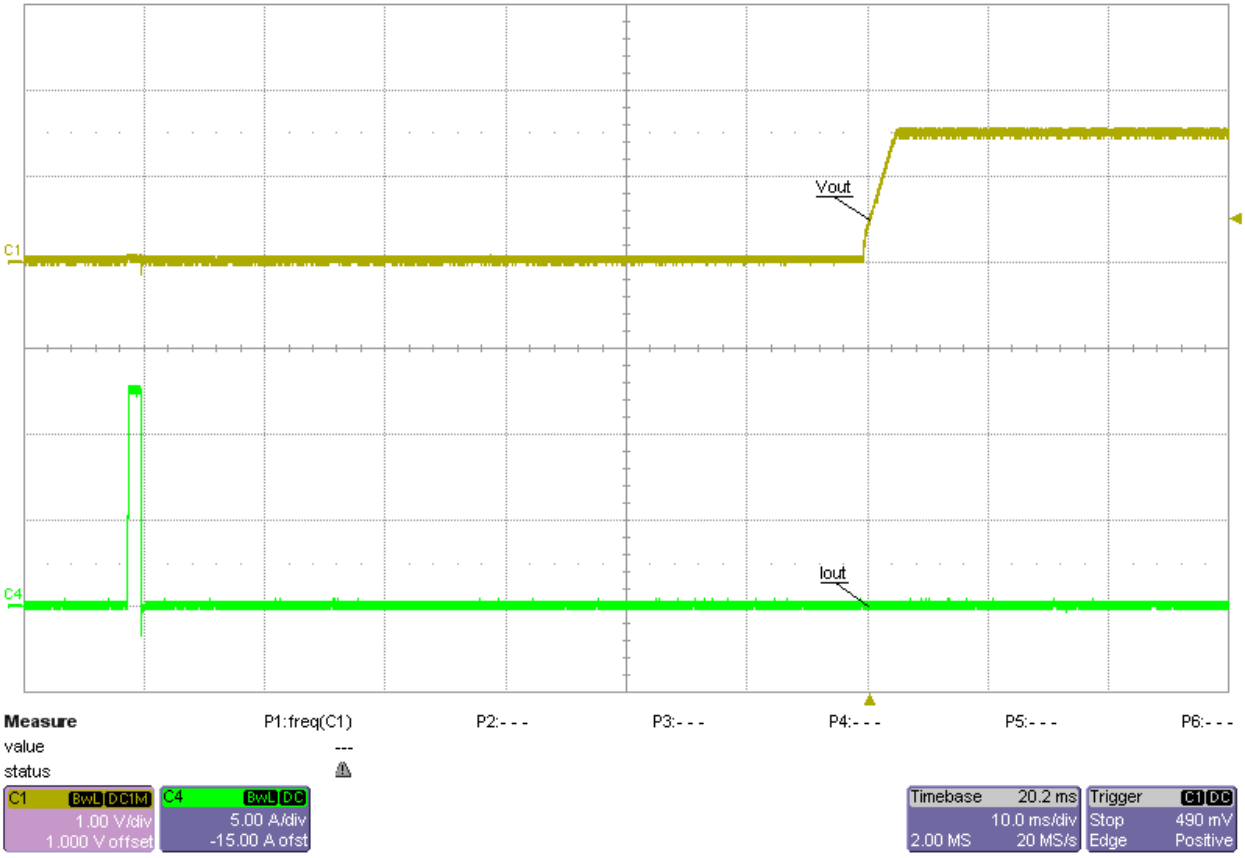
U4 CH1 (1.8V @ 2.5A) Output Short Circuit



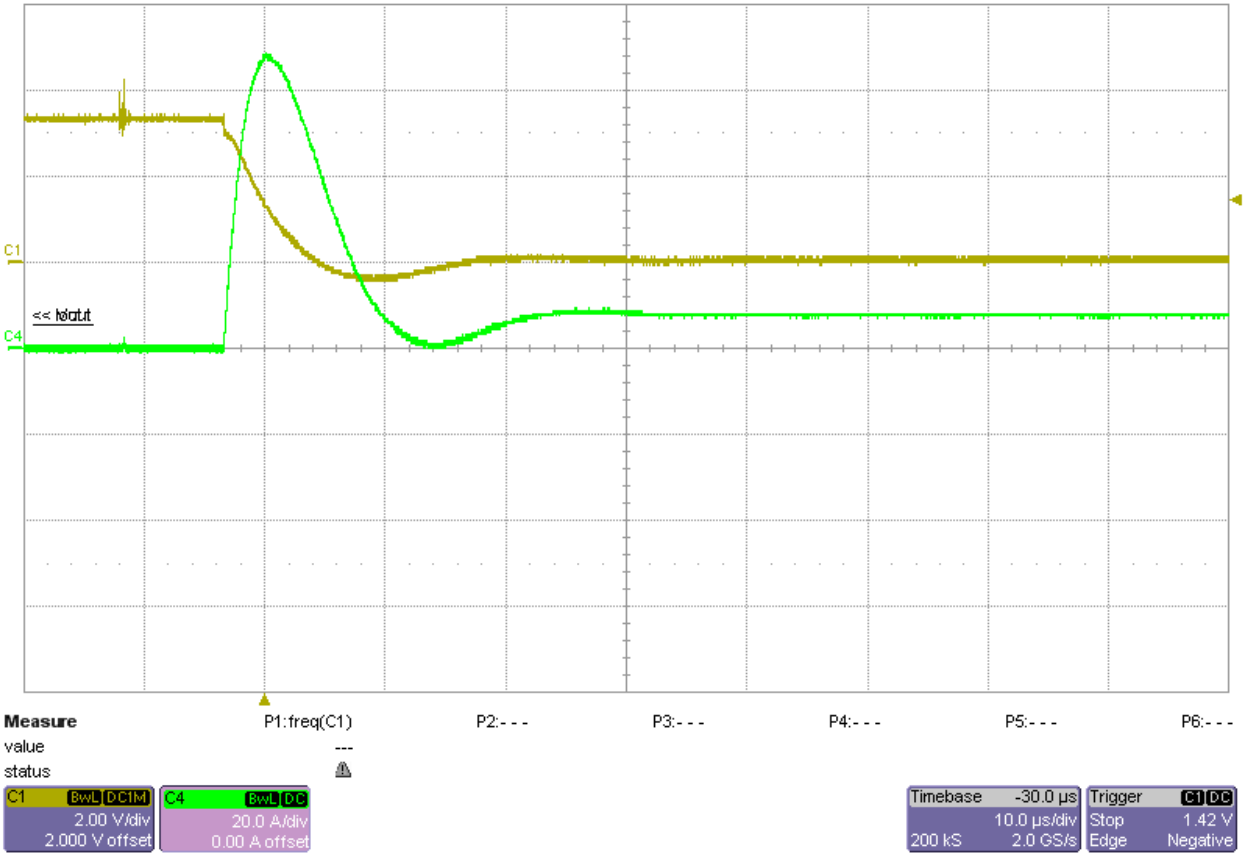
U4 CH1 (1.8V @ 2.5A) Output Short Circuit Recovery



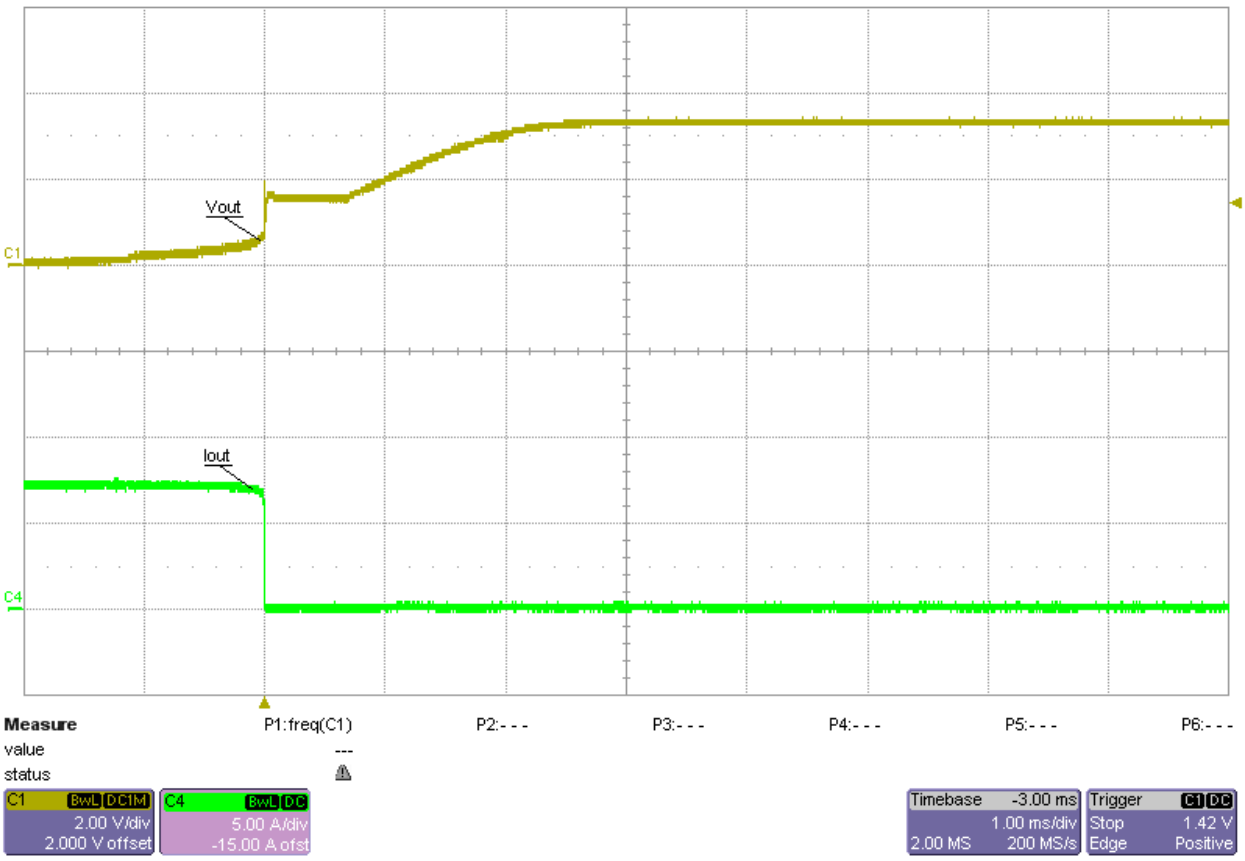
U4 CH2 (1.5V @ 6A) Output Short Circuit



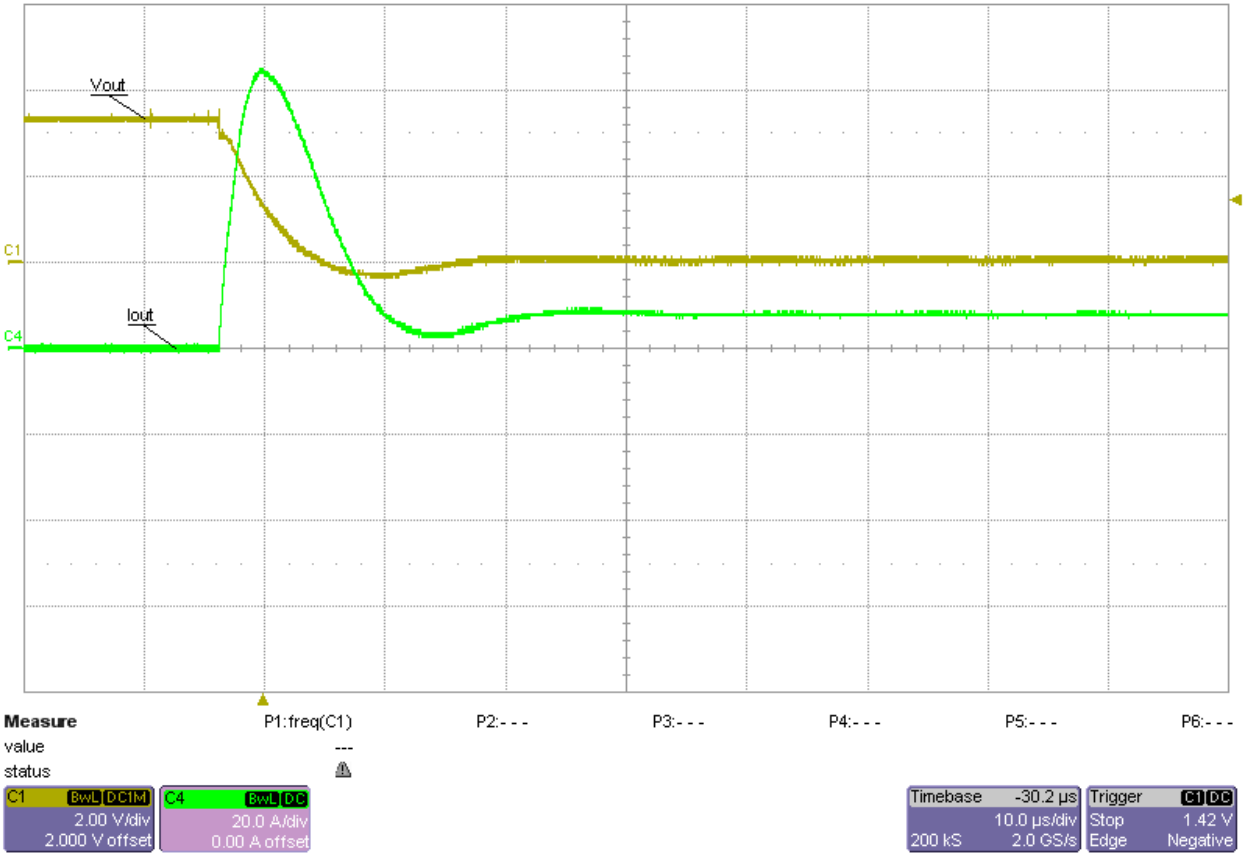
U4 CH2 (1.5V @ 6A) Output Short Circuit Recovery



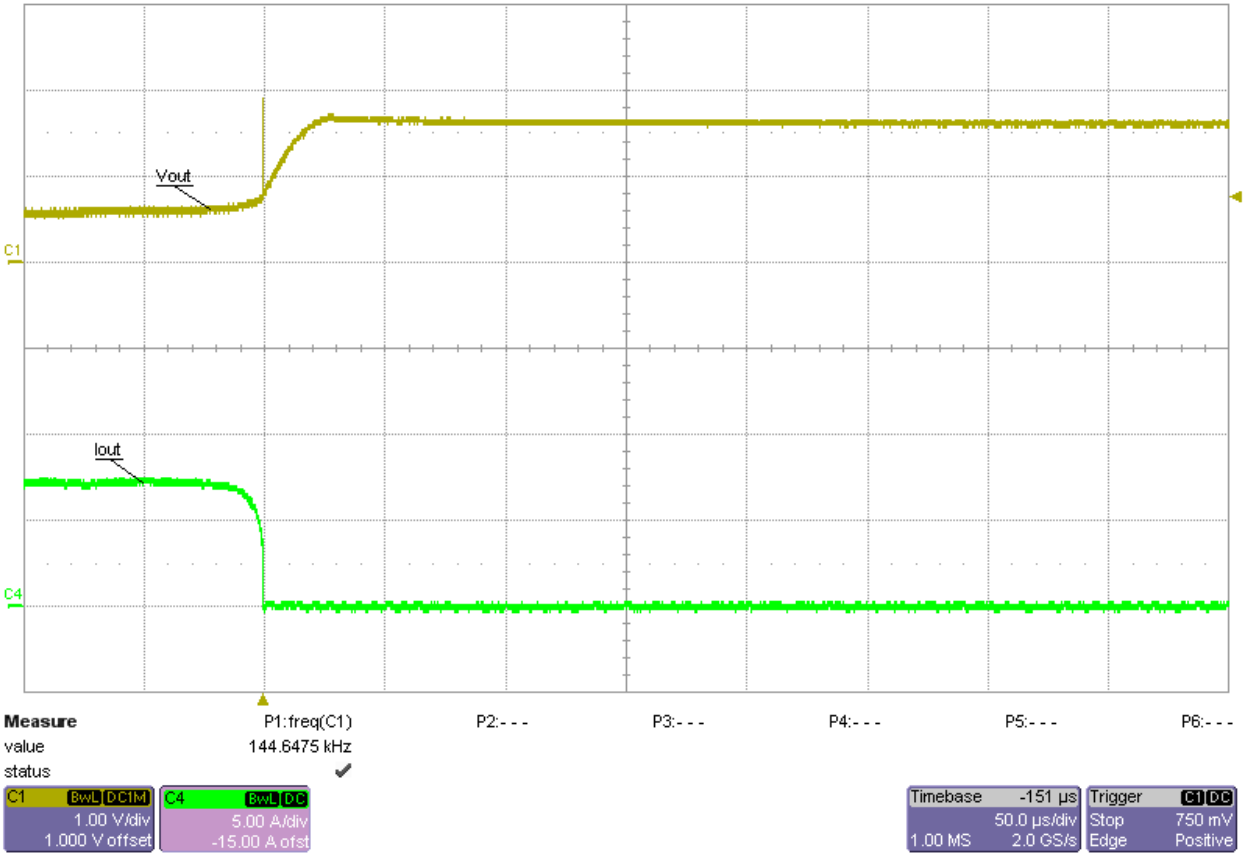
U7 (3.3V @ 5A) Output Short Circuit



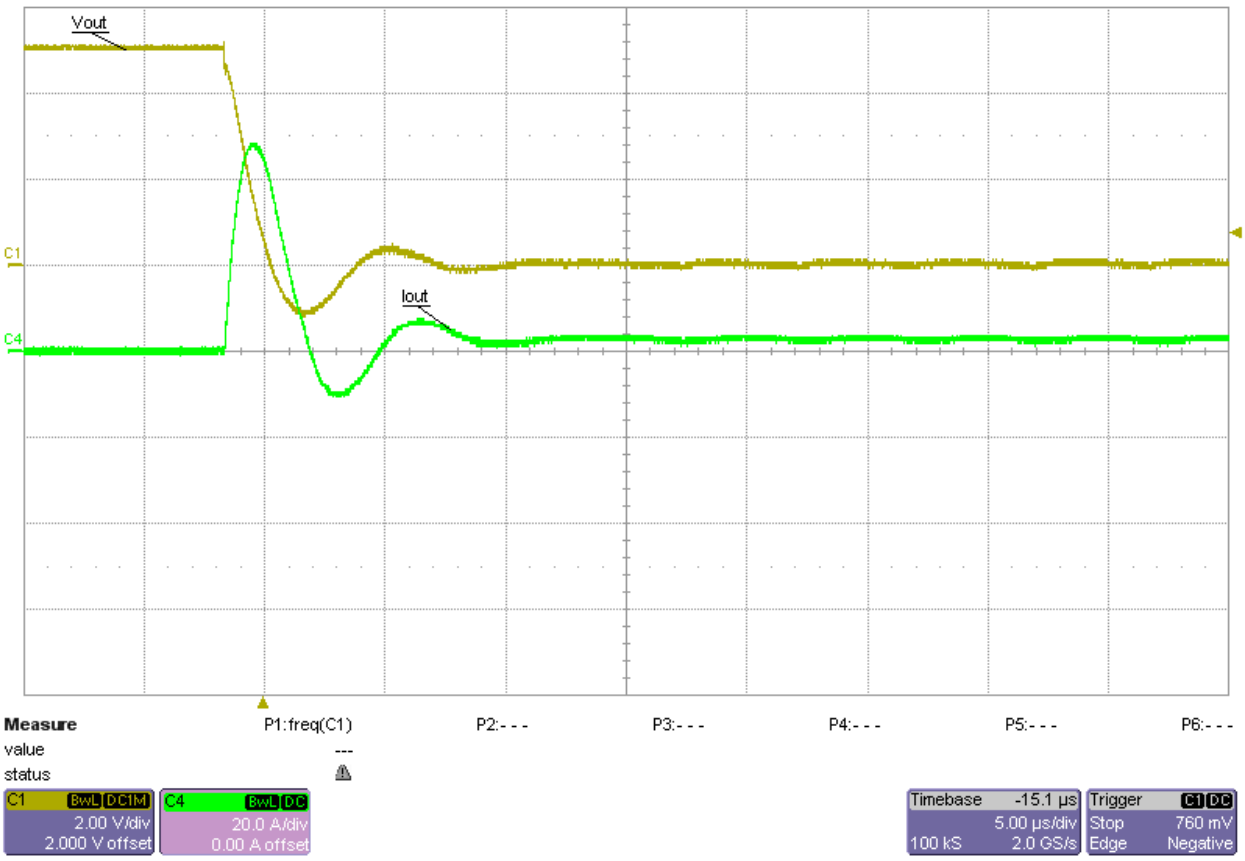
U7 (3.3V @ 5A) Output Short Circuit Recovery



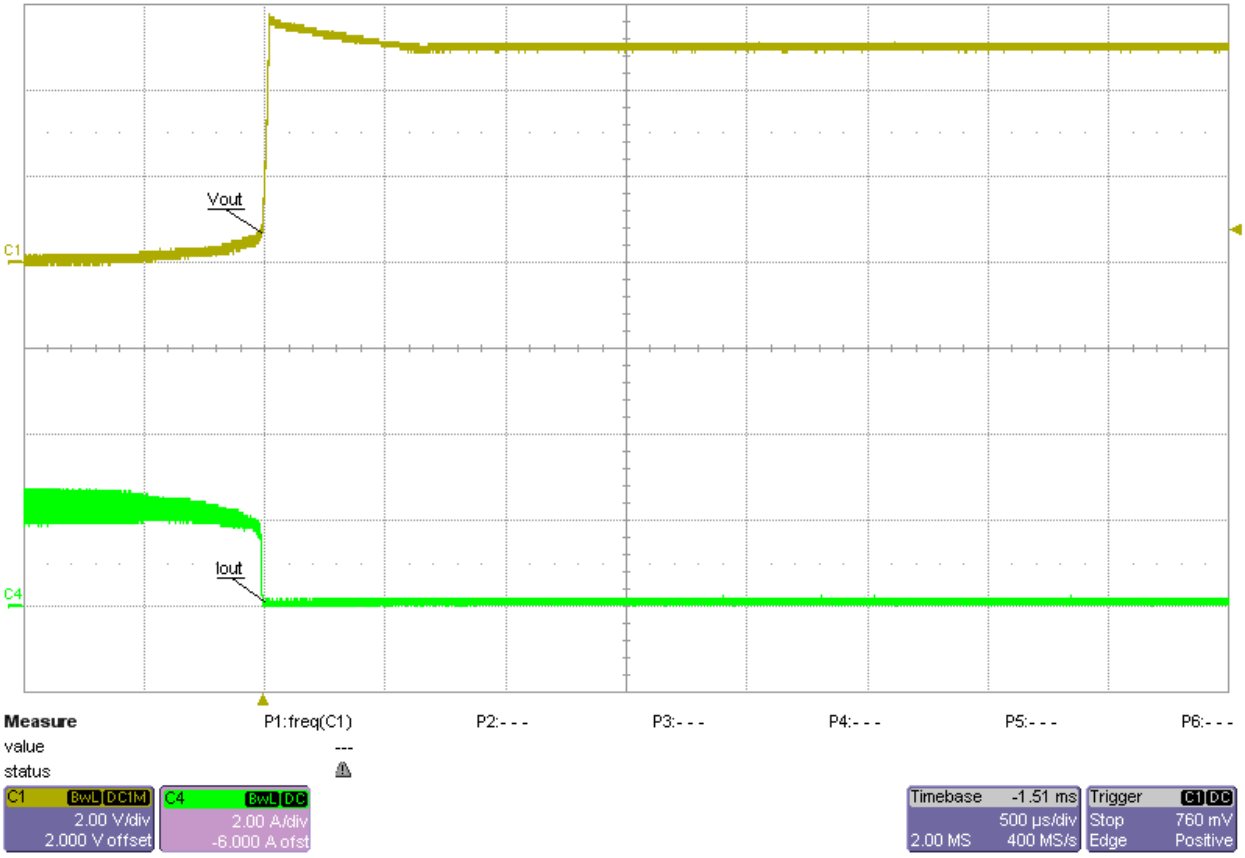
U8 (3.3V @ 5A) Output Short Circuit



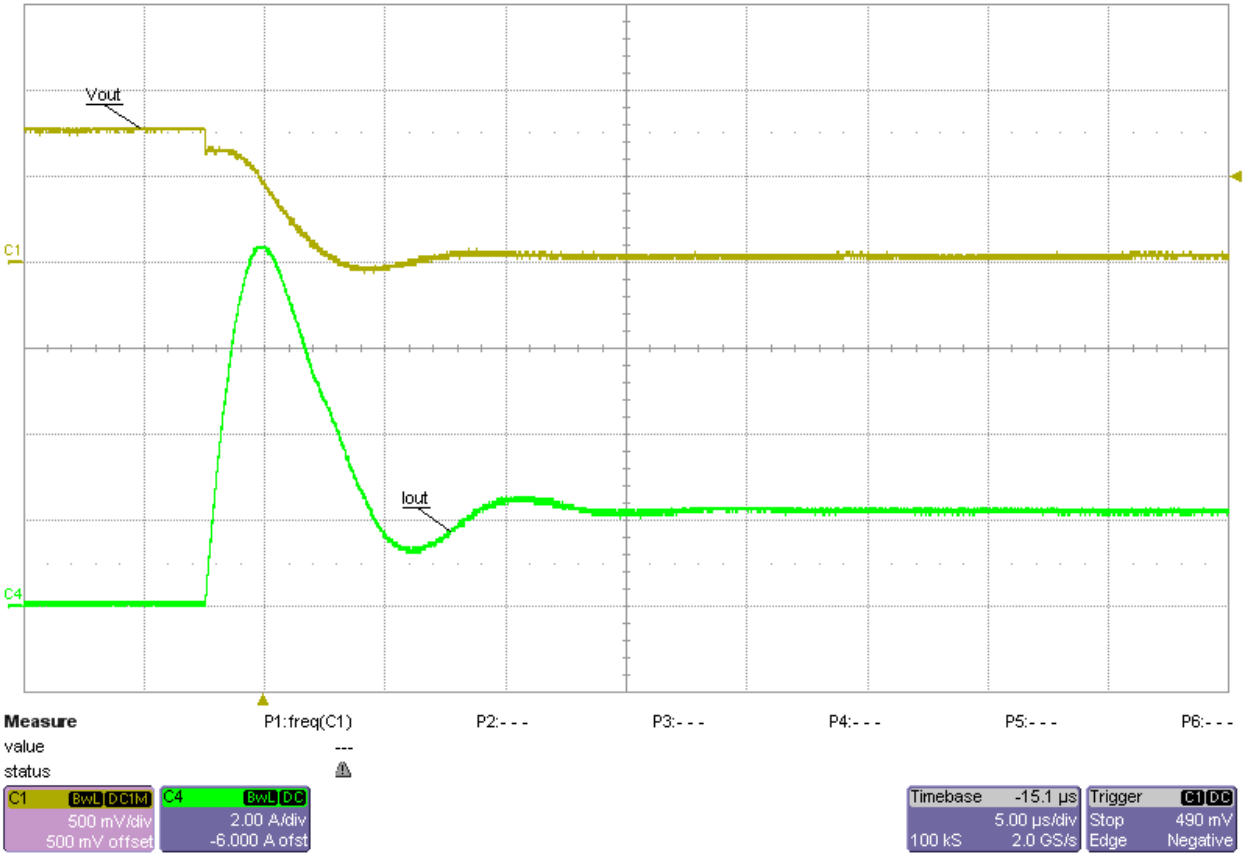
U8 (3.3V @ 5A) Output Short Circuit Recovery



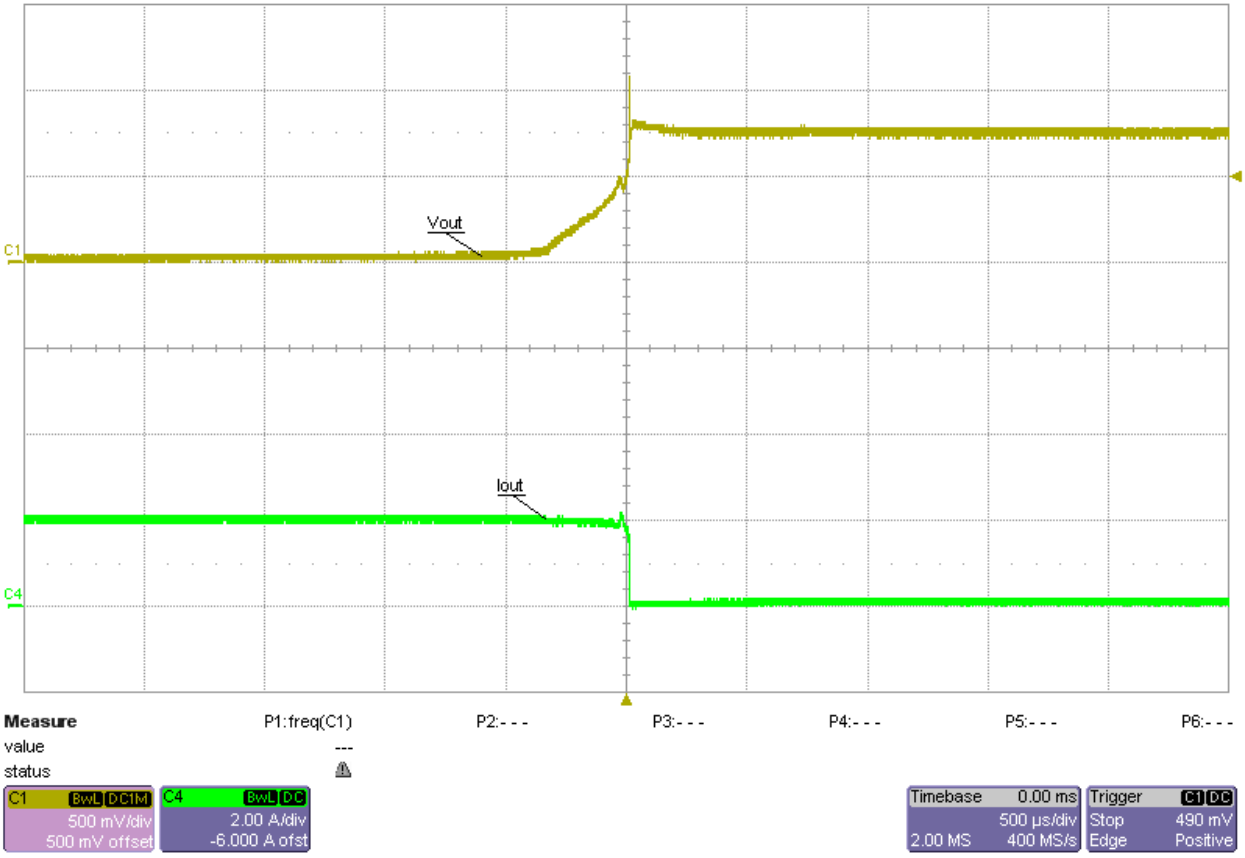
U6 (5V @ 2A) Output Short Circuit



U6 (5V @ 2A) Output Short Circuit Recovery

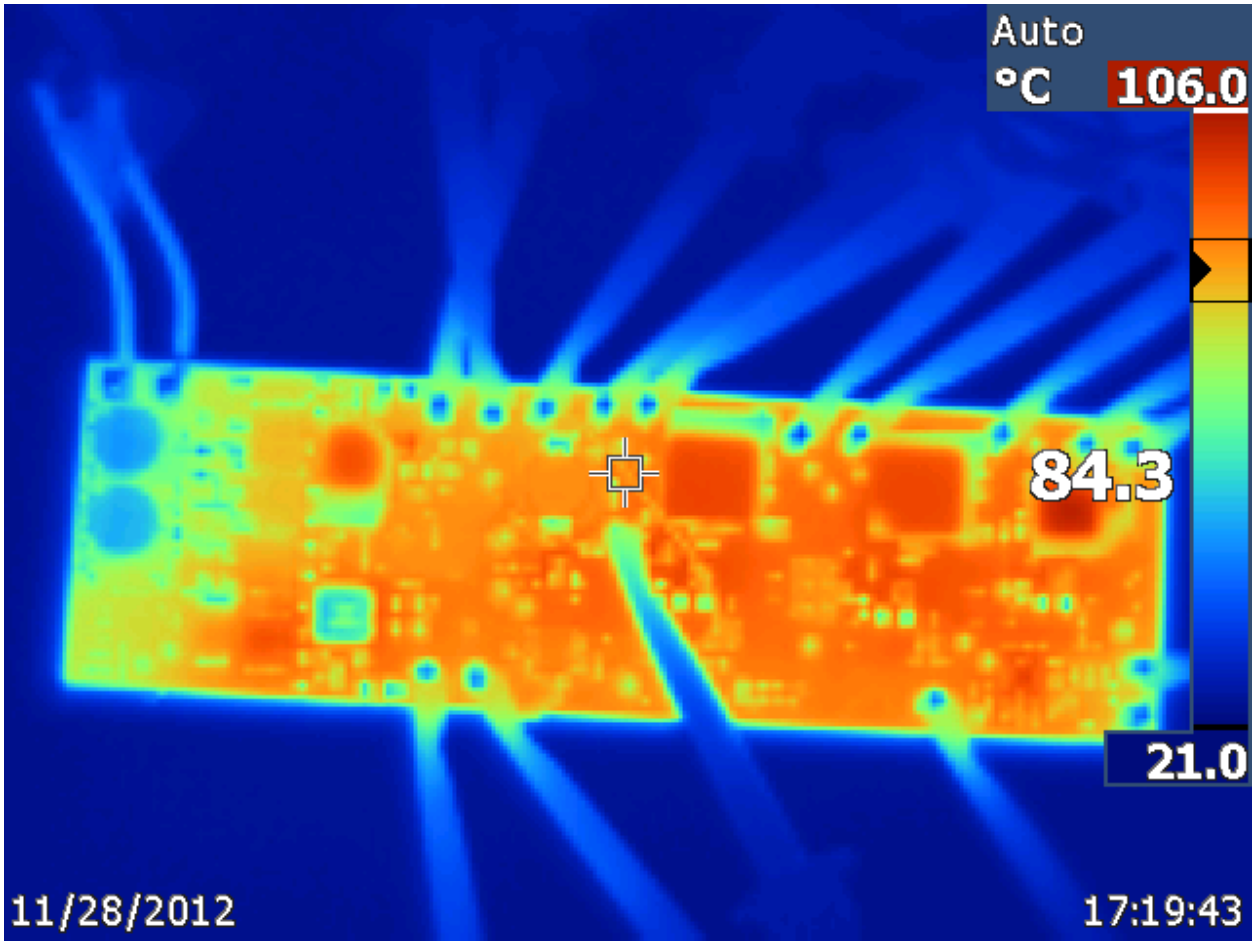


U5 (0.75V @ 1A continuous; 3A peak) Output Short Circuit

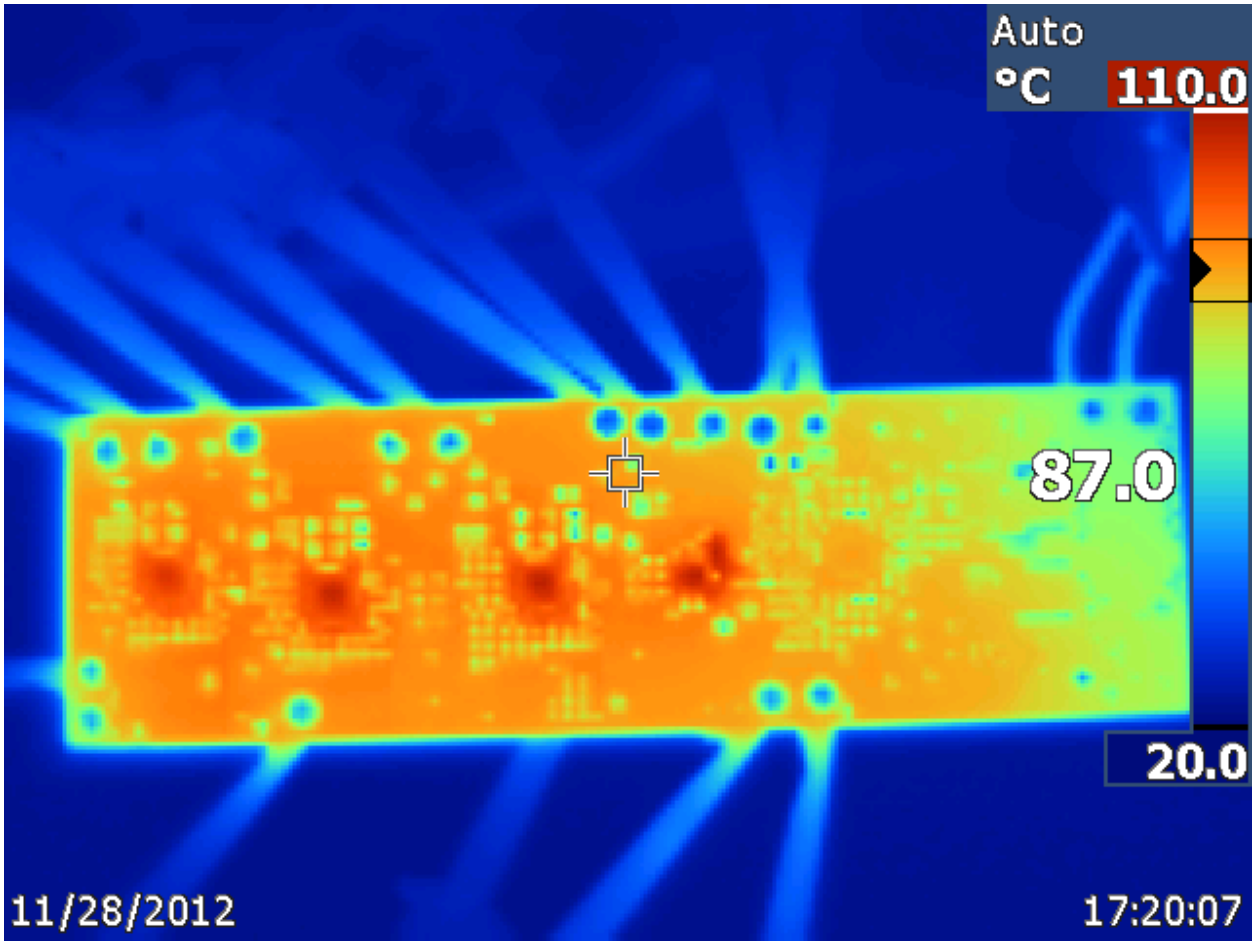


U5 (0.75V @ 1A continuous; 3A peak) Output Short Circuit Recovery

Thermal Data



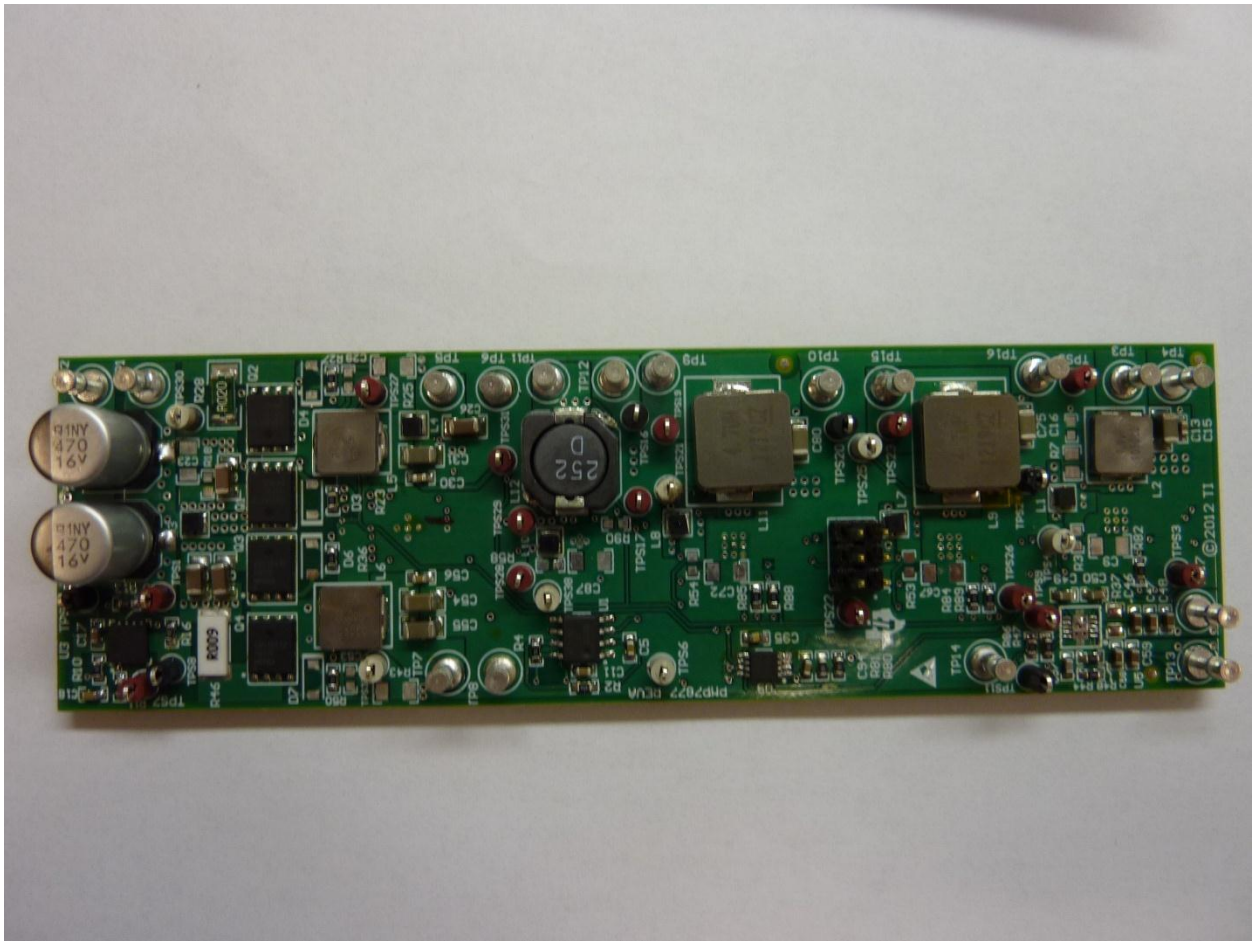
Top Side Thermal Image at Steady State (All outputs running at 100% load)



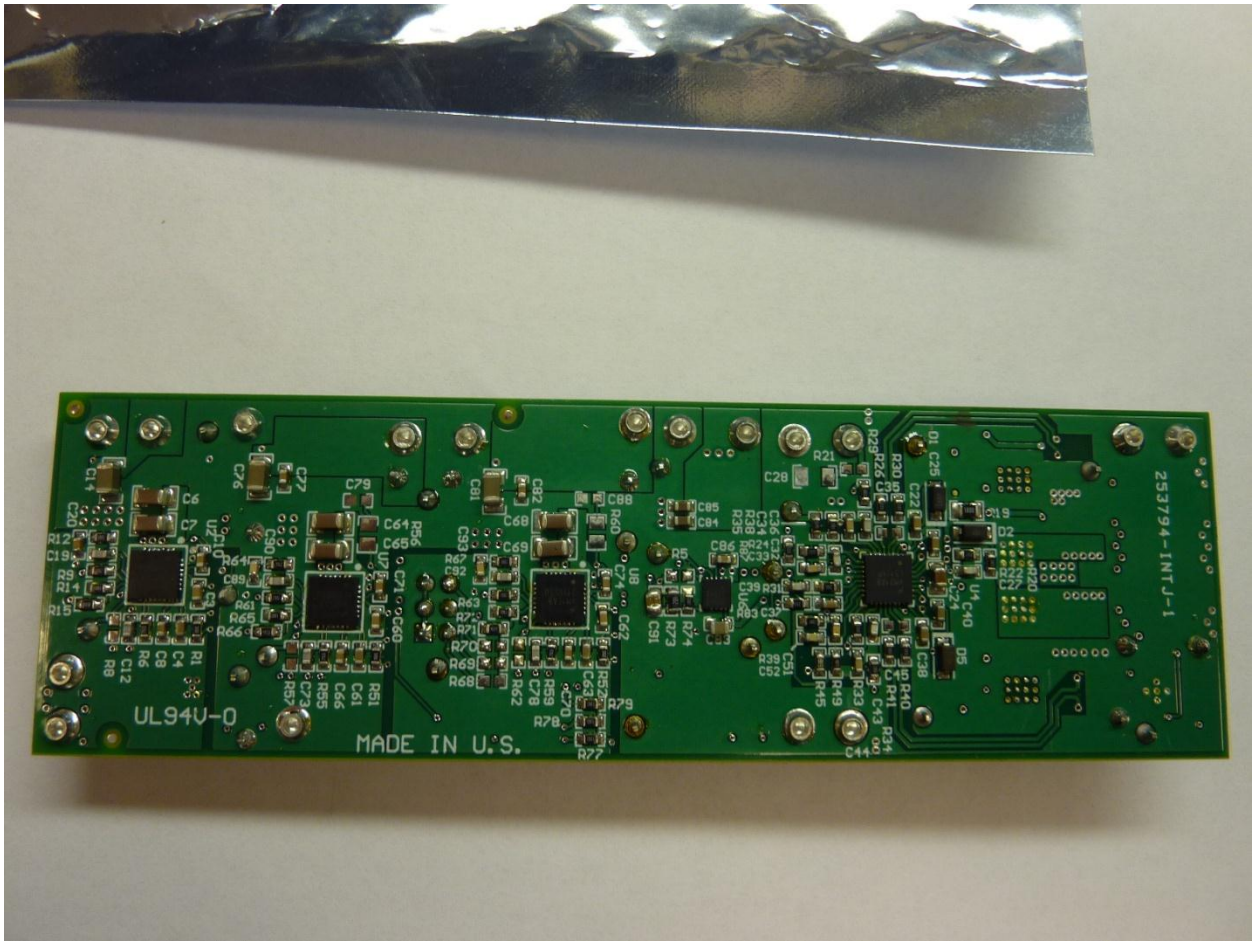
Bottom Side Thermal Image at Steady State (All outputs running at 100% load; soaked for 15 minutes)

FABRICATION

Board dimensions: 1.5” x 5”



Top Side



Bottom Side

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