Test Data
For PMP7993
08/30/2013

Power Specification

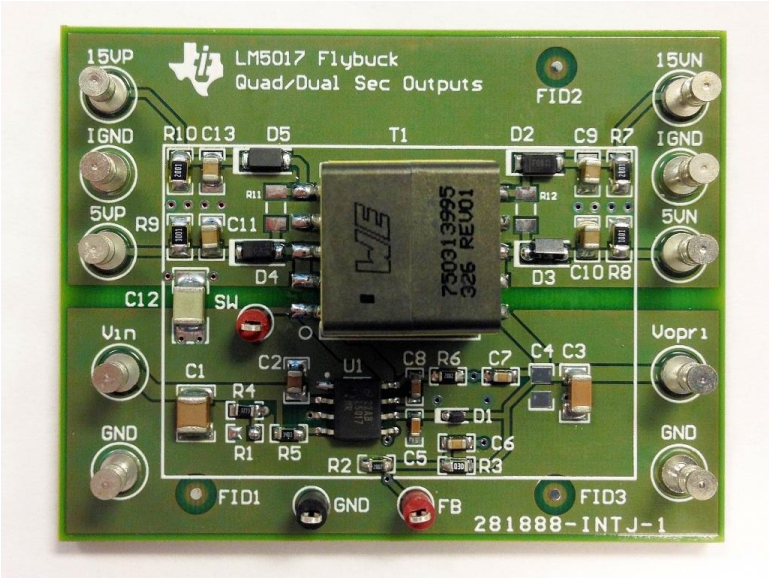
Vin range: 17V – 32V

Nominal Vin = 24V

Quad Isolated Outputs: ±15V@50mA, ±5V@100mA

Fsw = 260kHz

Board Photo

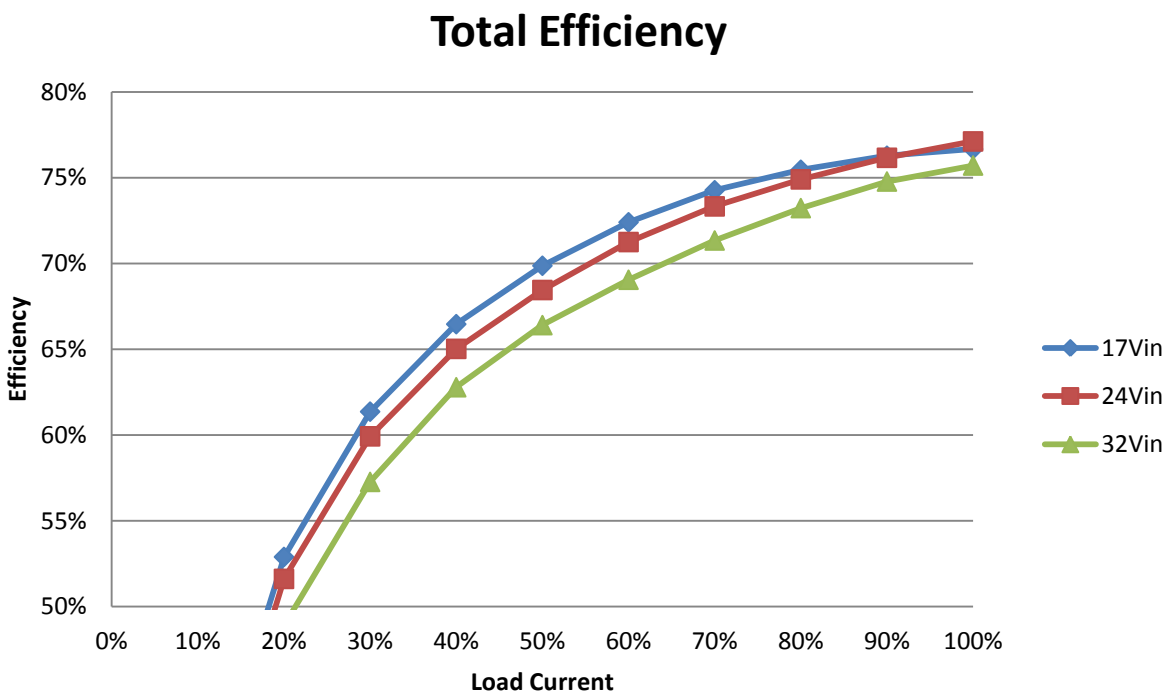


Size: 56x43mm

15VP - +15V output, 15VN – -15V output, 5VP - +5V output, 5VN – -5V output

Efficiency

The efficiency is calculated for all outputs; the load current is incremented at 10% interval.



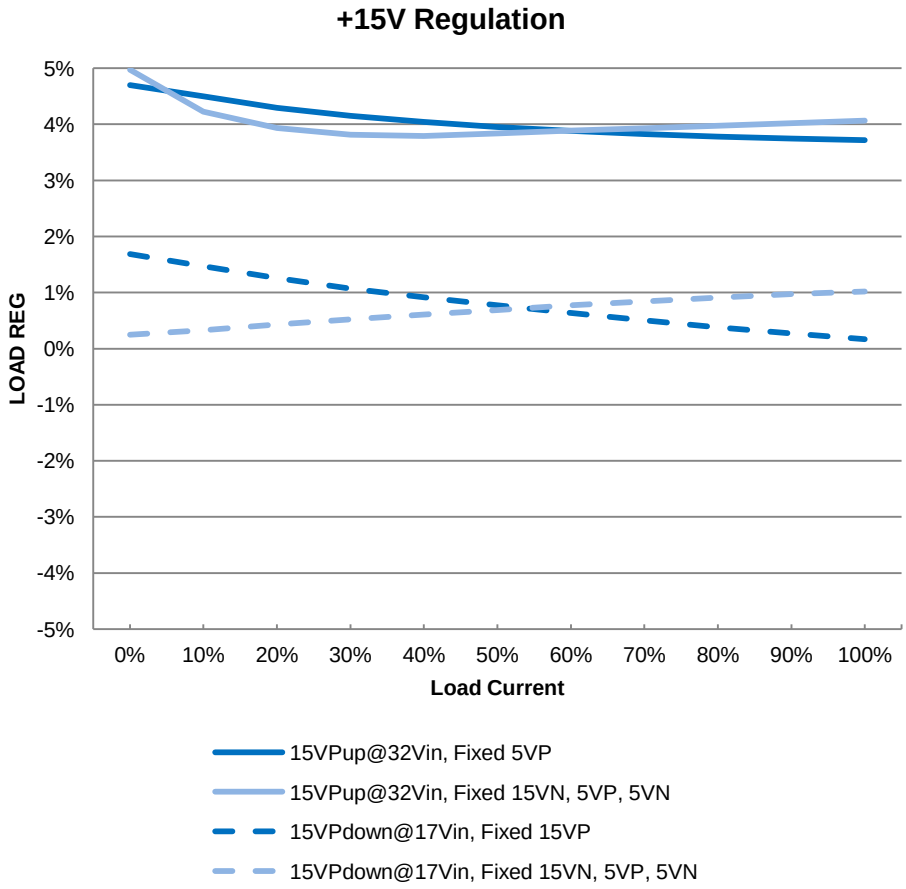
Cross Regulation

The cross regulation was tested by sweeping different load combination on four outputs. The test methodology is as follows:

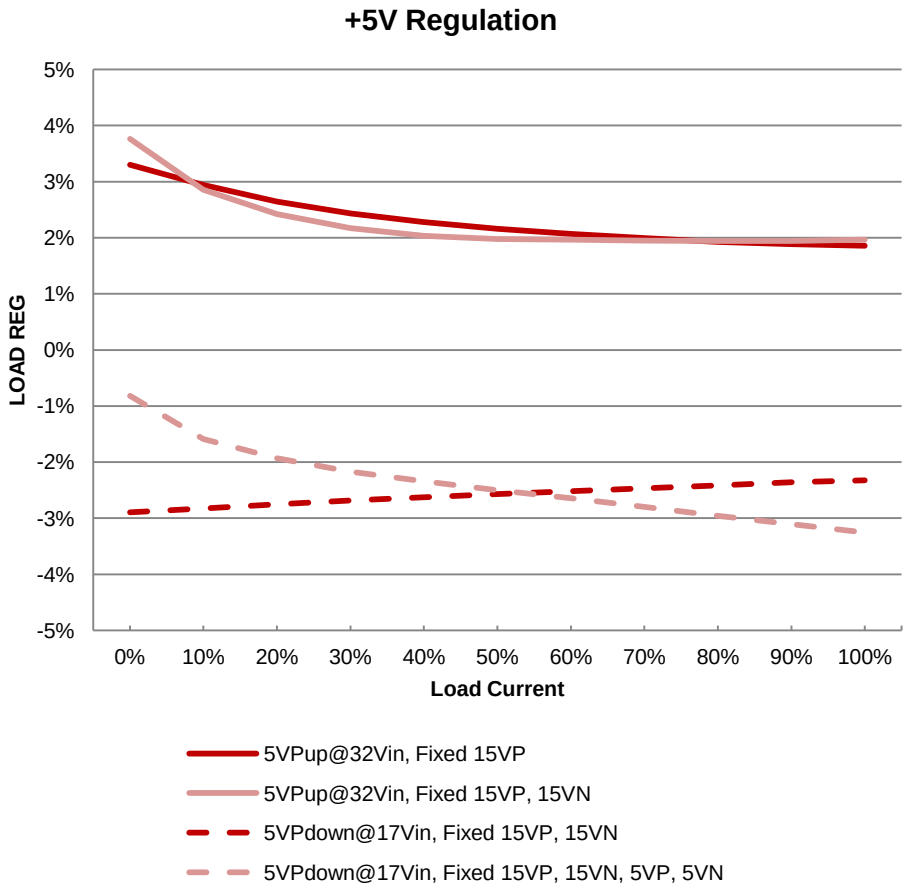
Step 1. Fix the load on one output
Step 2. Sweep other outputs' load from 0% to 100% at 10% increment
Step 3. Record the up & down max variation for all outputs
Step 4. Increase the fixed output load 10% and repeat from Step 1 until reaching 100% load
Step 5. Test different fixed output and Vin combinations and start from Step 1

Out of all the test combinations, the worst cases are summarized and plotted in the graphs below:
(Note: The line legend indicates the test condition. For example: "15VPup@32Vin, Fixed 5VP" means the curve shows the recorded upper limit of the +15V output variation in percentage under Vin=32V and fixed +5V output load condition)

1. +15V output regulation:(The ±15V regulation curves are symmetric about the 0% regulation axis)



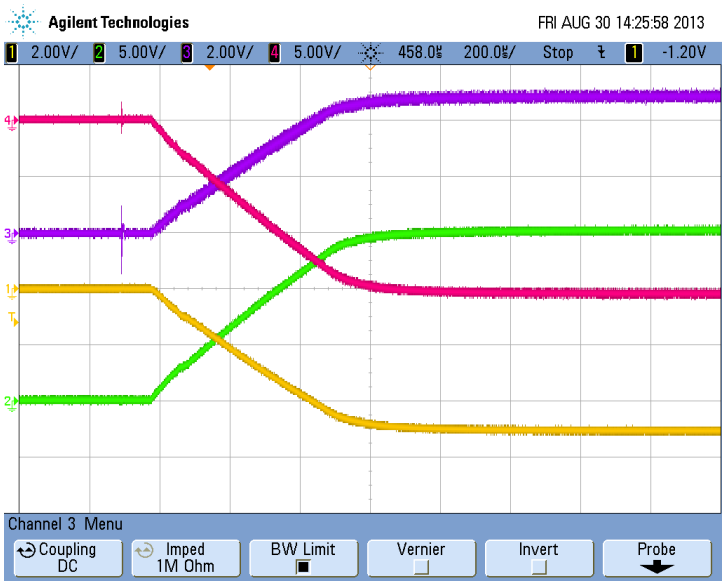
2. +5V output regulation: (The ±5V regulation curves are symmetric about the 0% regulation axis)



Start Up

Test condition: The input voltage was set at 24V, and all four outputs were set at full load.
Ch1 - Vin, Ch2 – 15VP (+15V), Ch3 – 5VP (+5V)

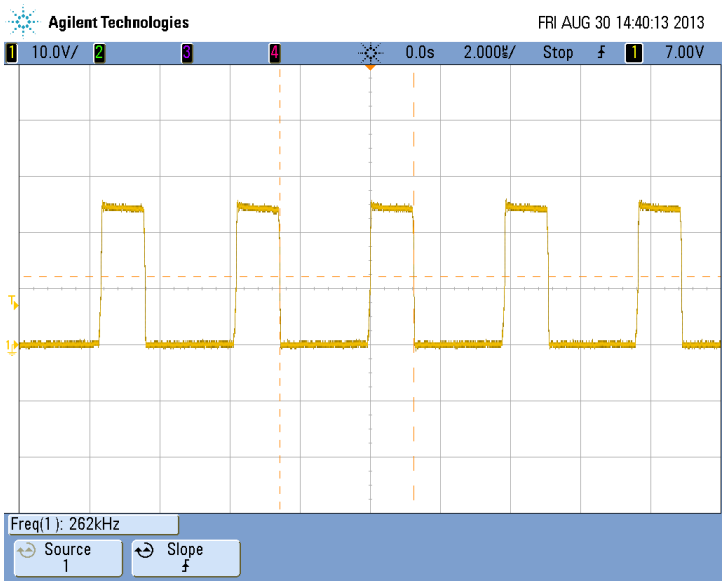
Ch1 – 5VN (-5V), Ch2 - 15VP (+15V), Ch3 - 5VP (+5V), Ch4 - 15VN (-15V)



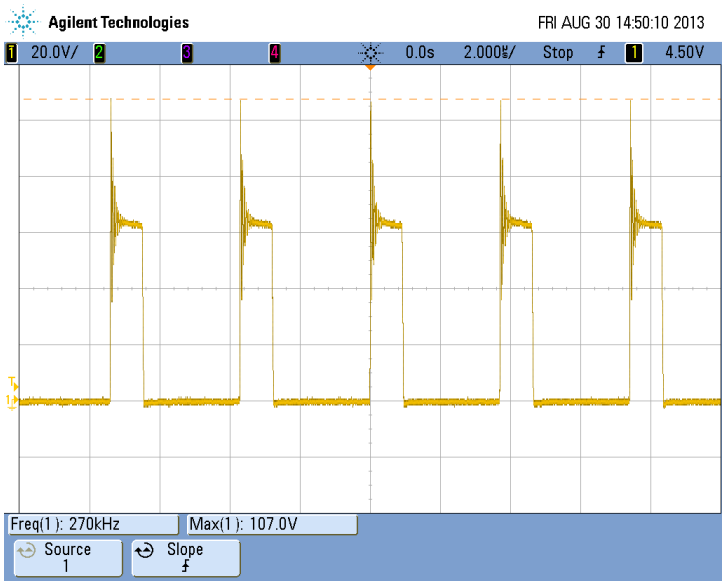
Switching Waveforms

1. Test condition: The input voltage was set at 24V, and all four outputs were set at full load.
   Ch1 – Vsw (switch node voltage)

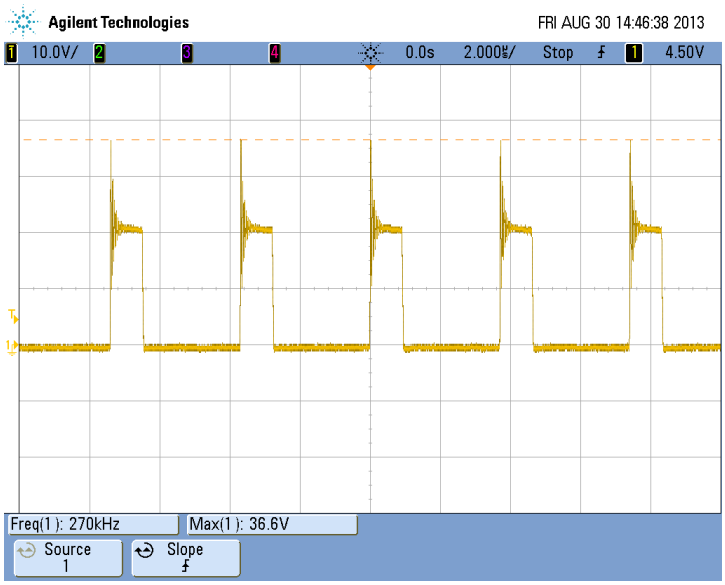
2. Test condition: The input voltage was set at 24V, and all four outputs were set at no load.
   Ch1 – Vsw (switch node voltage)



3. Test condition: The input voltage was set at 32V, and all four outputs were set at full load.
Ch1 – Vd5 (+15V output diode voltage stress from cathode (-) to anode (+), 200V rating diode)



4. Test condition: The input voltage was set at 32V, and all four outputs were set at full load.
Ch1 – Vd4 (+5V output diode voltage stress from cathode (-) to anode (+), 60V rating diode)



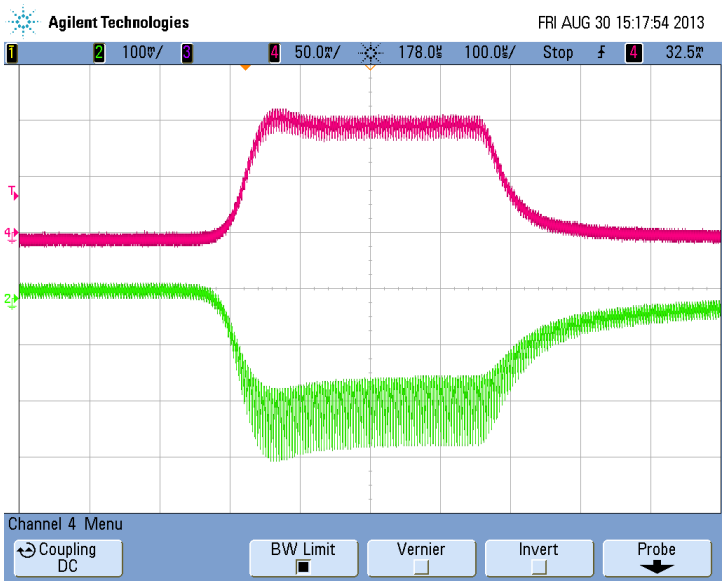
Load Transients

+15V Output Load Step

Test condition: Vin = 24V, 15VP (+15V) load from 0A to 50mA, no load on other outputs.
Ch2- 15VP (+15V) (AC mode), Ch4- +15V output current

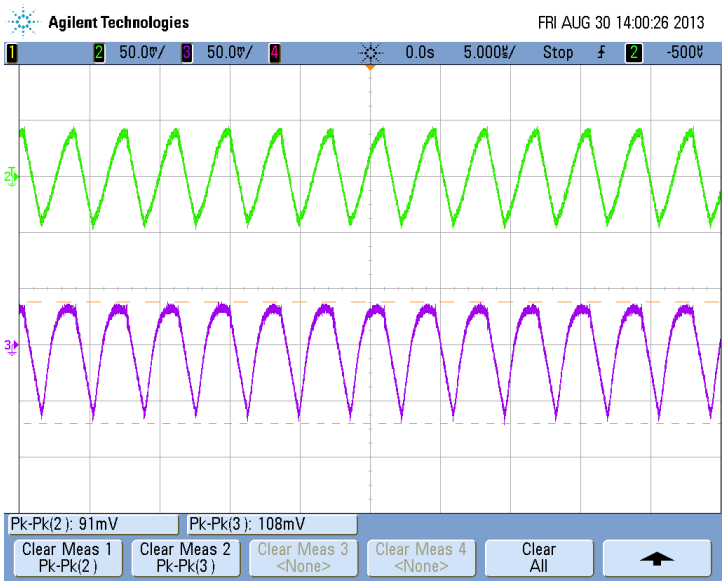
+5V Output Load Step

Test condition: Vin = 24V, 5VP (+5V) load from 0A to 100mA, no load on other outputs.
Ch2- 5VP (+5V) (AC mode), Ch4- +5V output current



Output Voltage Ripples

Test condition: The input voltage was set at 24V, and all four outputs were set at full load.
Ch2 - 15VP (+15V) (AC coupled), Ch3 - 5VP (+5V) (AC coupled)



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