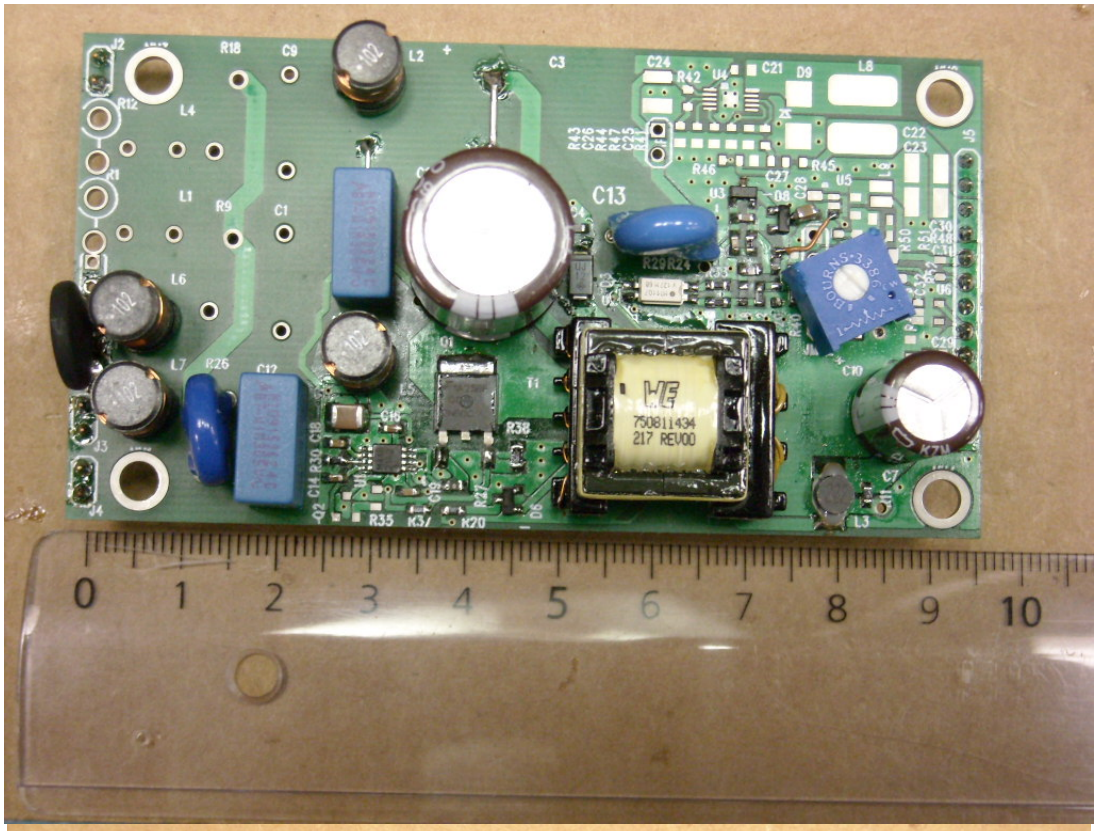
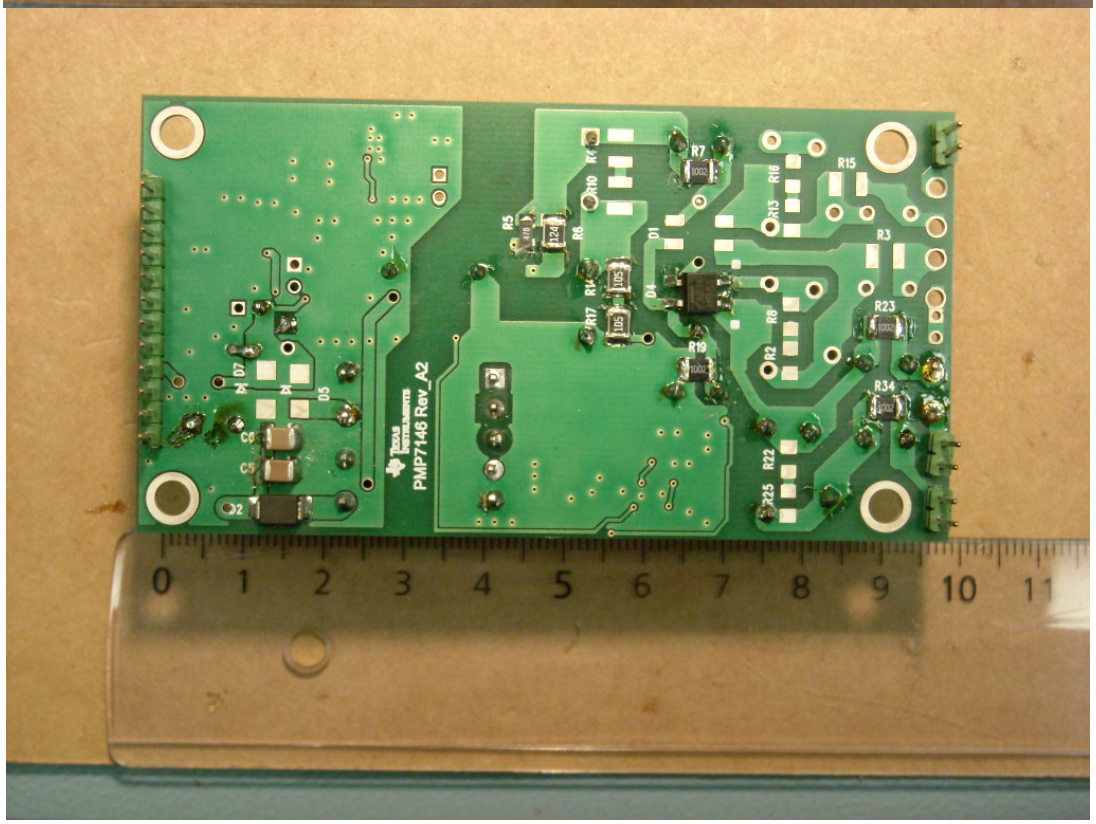
PHOTO OF THE PROTOTYPE:

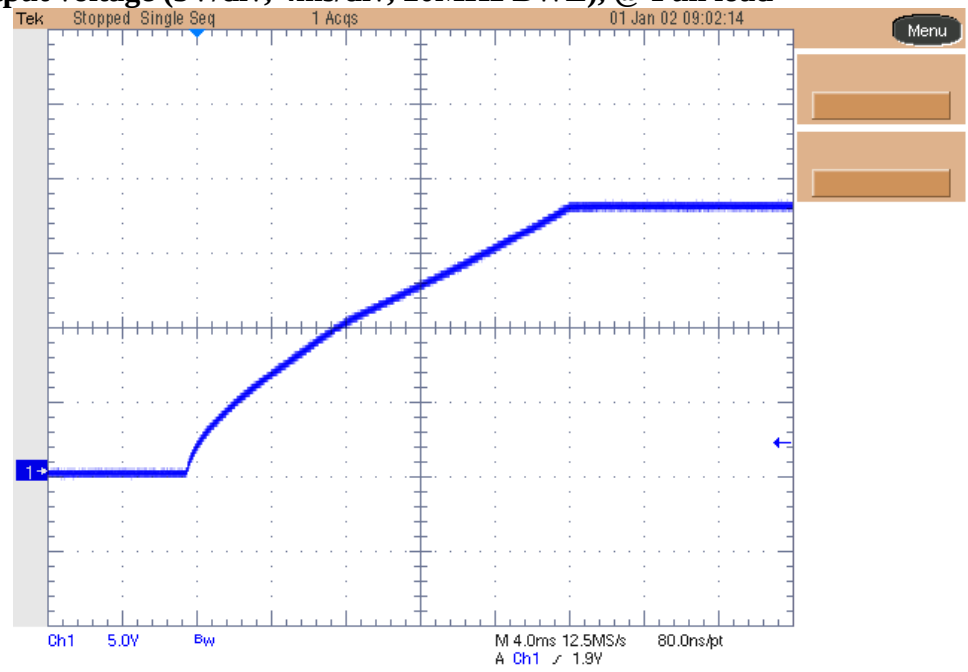




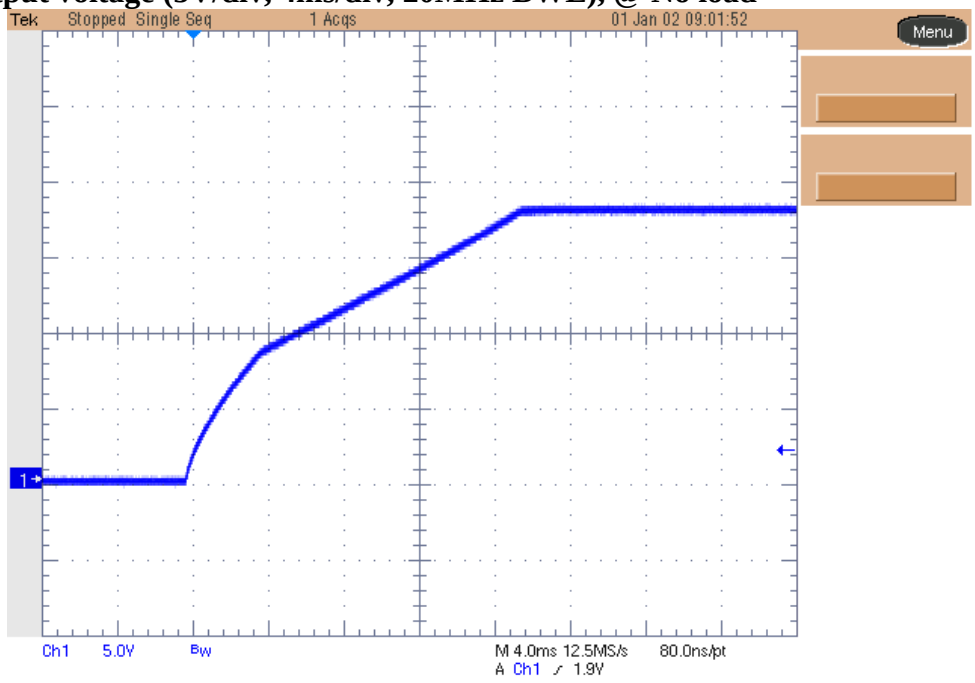
1 Startup, shut down

The output voltage behavior at startup is shown in the images below. The input voltage was set to 320Vdc. The output fully loaded for the upper picture and unloaded for the bottom one.

Ch.1: Output voltage (5V/div, 4ms/div, 20MHz BWL), @ Full load

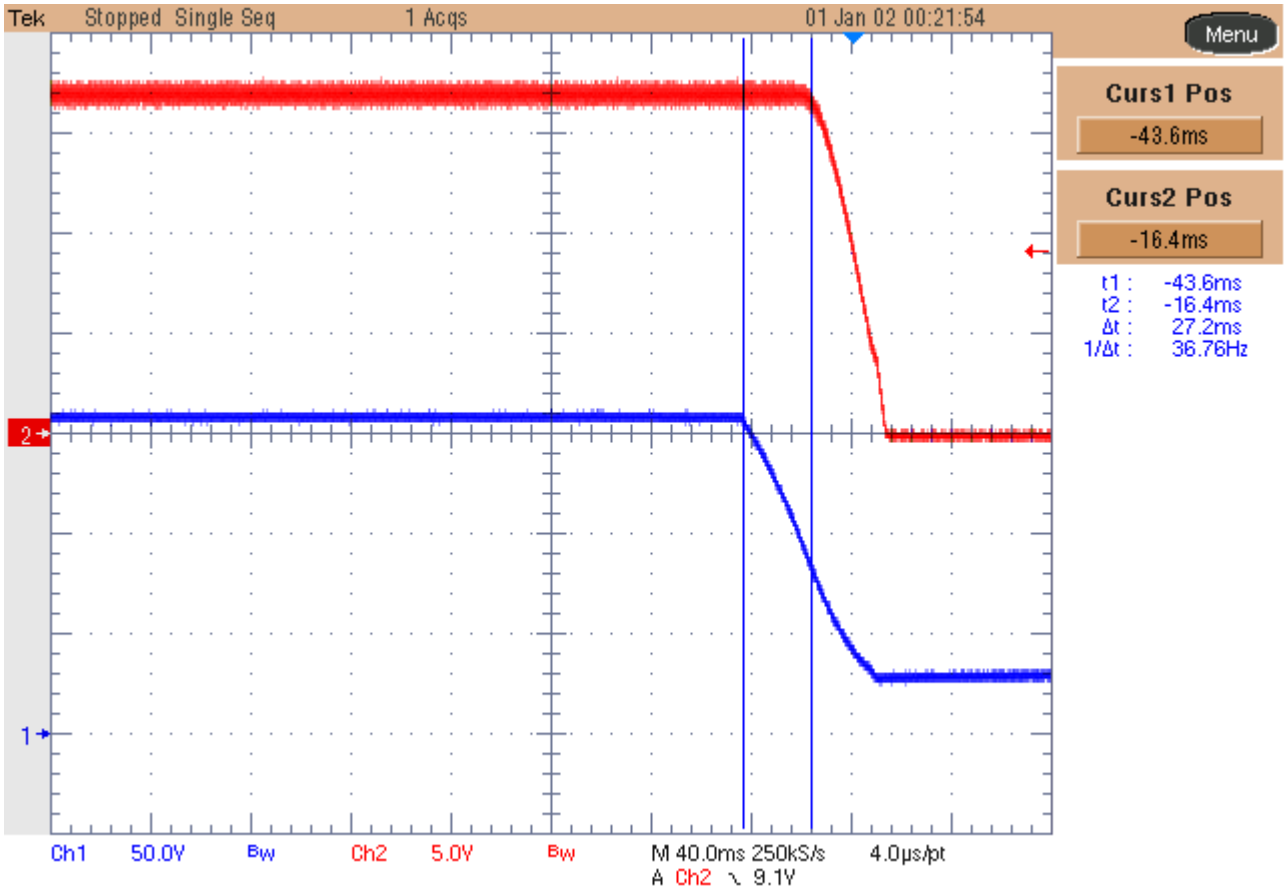


Ch.1: Output voltage (5V/div, 4ms/div, 20MHz BWL), @ No load



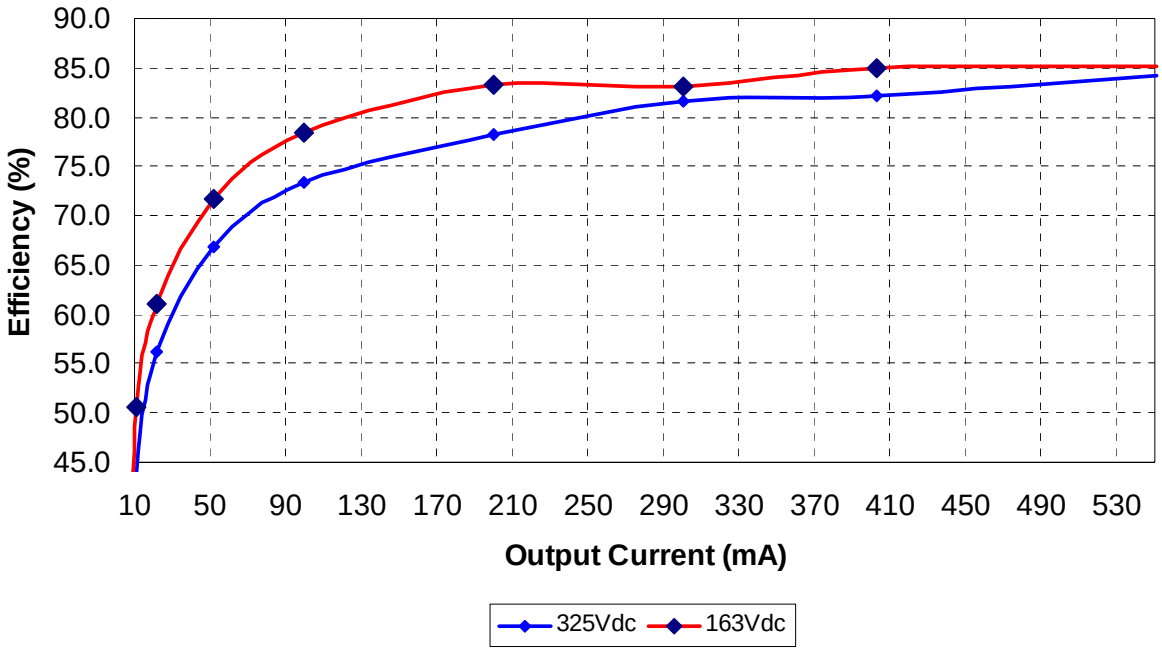
The DC source has been disconnected while the converter delivered full power. The hold-up time is shown in the image below. The input voltage has been set to the peak value of 115Vac, which is 163Vdc. The behavior of input and output voltages is shown in the image below.

Ch.1: Input voltage (50V/div, 40ms/div, 20MHz BWL)
Ch.2: Output voltage (5V/div, 20MHz BWL); **➔ Hold-up time = 27.2msec**



2 Efficiency

The efficiency data are shown in the tables and graph below. In order to get an accurate measure of the input power, a DC voltage source has been employed, set to the peak value of the two nominal input voltages: 115Vac and 230Vac (163Vdc and 325Vdc).

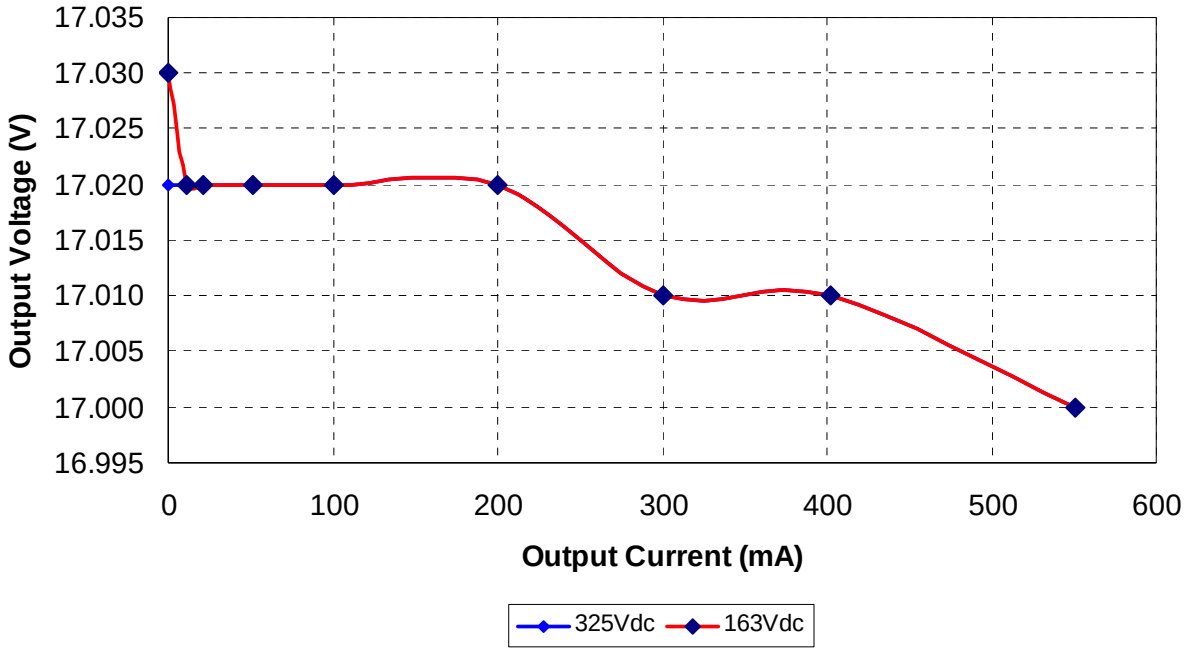


Iout (mA)	Vout (V)	Pout (W)	Iin (mA)	Vin (Vdc)	Pin (W)	Ploss (W)	Eff (%)
0.0	17.02	0.00	0.538	325.0	0.17	0.17	0.00
10.9	17.02	0.19	1.299	324.9	0.42	0.24	43.96
21.8	17.02	0.37	2.031	325.0	0.66	0.29	56.21
51.5	17.02	0.88	4.03	325.2	1.31	0.43	66.88
100.1	17.02	1.70	7.14	325.2	2.32	0.62	73.37
200.0	17.02	3.40	13.39	325.2	4.35	0.95	78.17
300.0	17.01	5.10	19.24	325.1	6.25	1.15	81.58
402.4	17.01	6.84	25.61	325.1	8.33	1.48	82.21
550.9	17.00	9.37	34.24	325.1	11.13	1.77	84.13

Iout (mA)	Vout (V)	Pout (W)	Iin (mA)	Vin (Vdc)	Pin (W)	Ploss (W)	Eff (%)
0.0	17.03	0.00	0.769	163.0	0.13	0.13	0.00
11.0	17.02	0.19	2.273	162.7	0.37	0.18	50.63
21.7	17.02	0.37	3.71	163.1	0.61	0.24	61.04
51.5	17.02	0.88	7.50	163.0	1.22	0.35	71.70
100.1	17.02	1.70	13.34	163.0	2.17	0.47	78.35
200.0	17.02	3.40	25.06	163.0	4.08	0.68	83.33
300.0	17.01	5.10	37.68	162.9	6.14	1.04	83.14
402.4	17.01	6.84	49.4	163.0	8.05	1.21	85.01
550.9	17.00	9.37	67.5	162.9	11.00	1.63	85.17

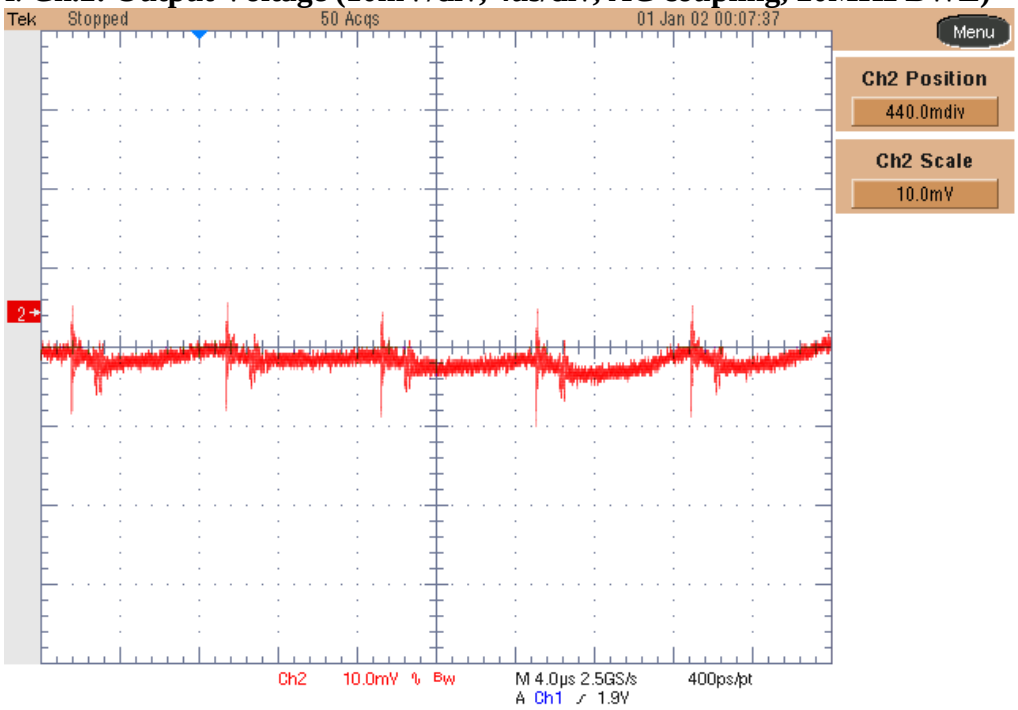
3 Output voltage regulation

The output voltage regulation versus output current is shown in the graph below. The regulation behavior is almost identical for both input voltages. Only a small difference has been measured in no-load conditions (see also values from the tables above).



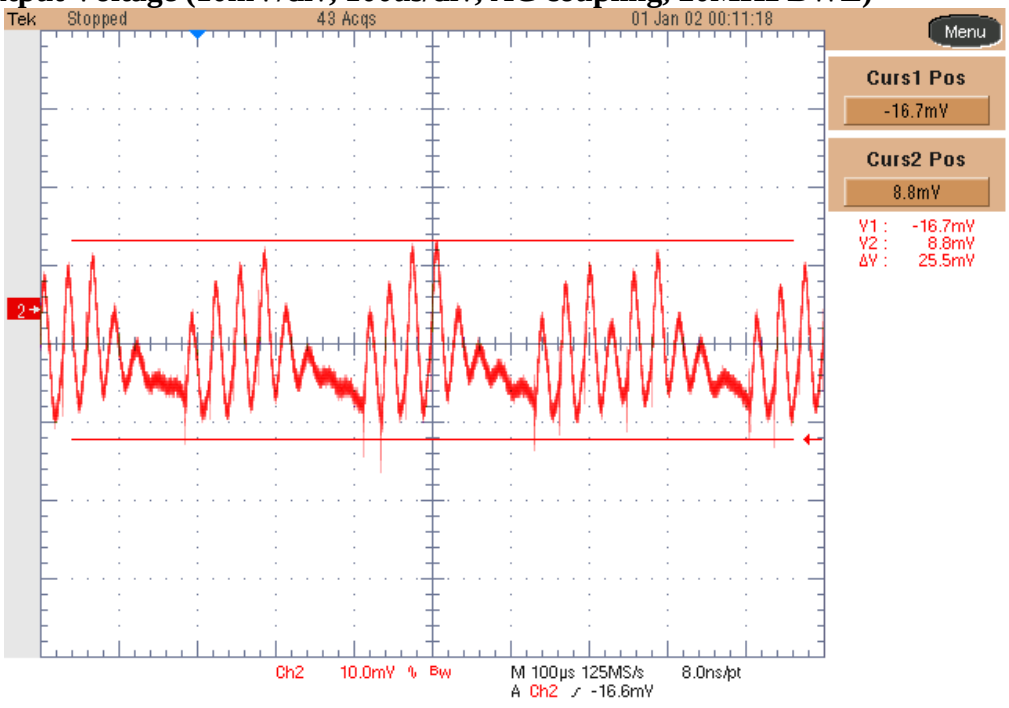
4 Output Ripple Voltage (output set to 17V)

The output ripple voltage is shown in the plot below. The input was set to 320Vdc and the output to 550mA. **Ch.2: Output Voltage (10mV/div, 4us/div, AC coupling, 20MHz BWL)**



The picture below shows how the output ripple voltage is increased during a burst mode condition. The input was unmodified and the output set to 30mA.

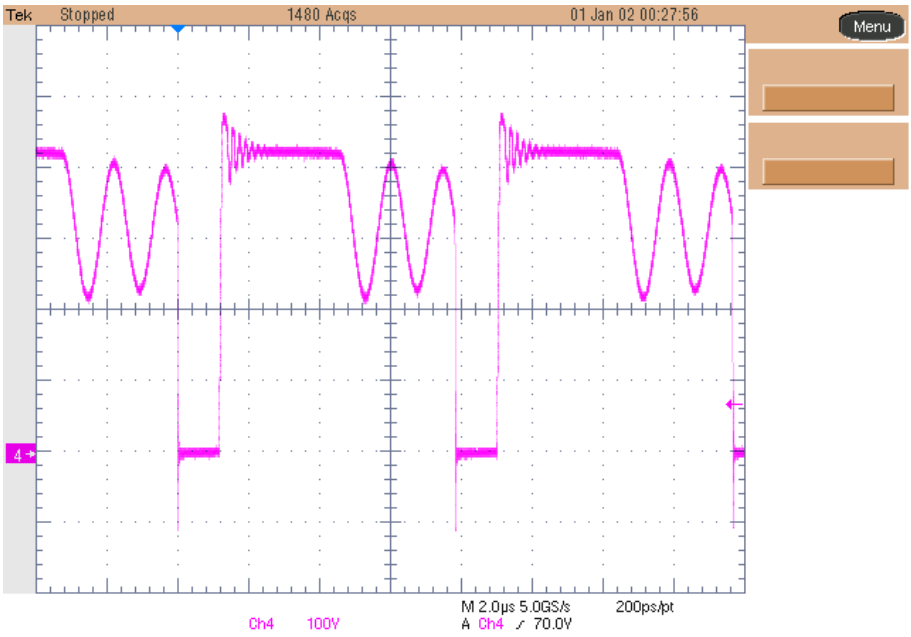
Ch.2: Output Voltage (10mV/div, 100us/div, AC coupling, 20MHz BWL)



5 Switching Node Waveform

The image below shows the peak voltage on the drain of the Mosfet Q1 with a 320Vdc input, and full load.

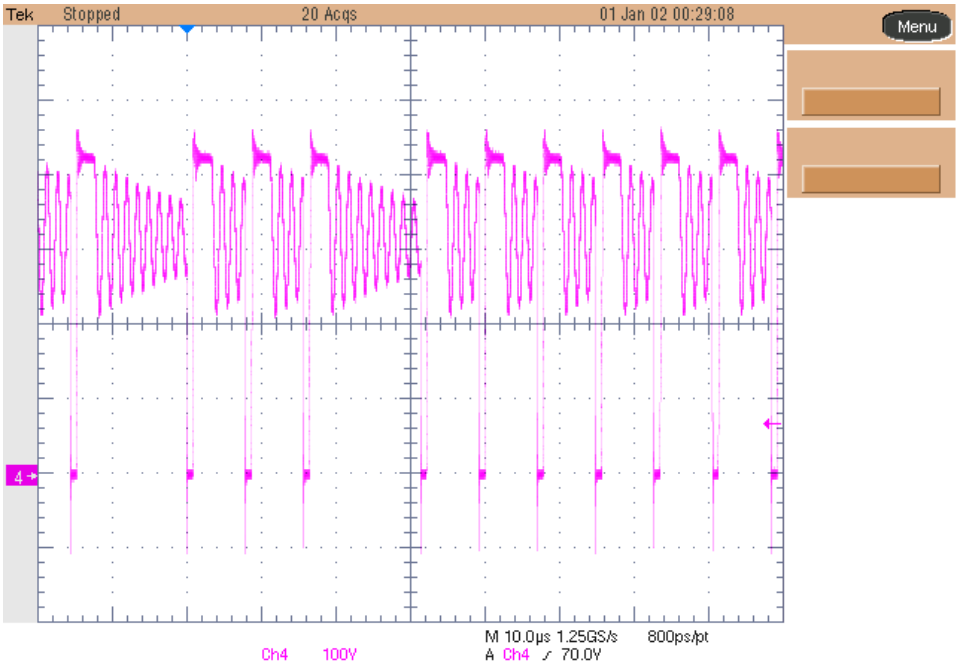
Ch4: Drain voltage (100V/div, 2us/div, No BWL).



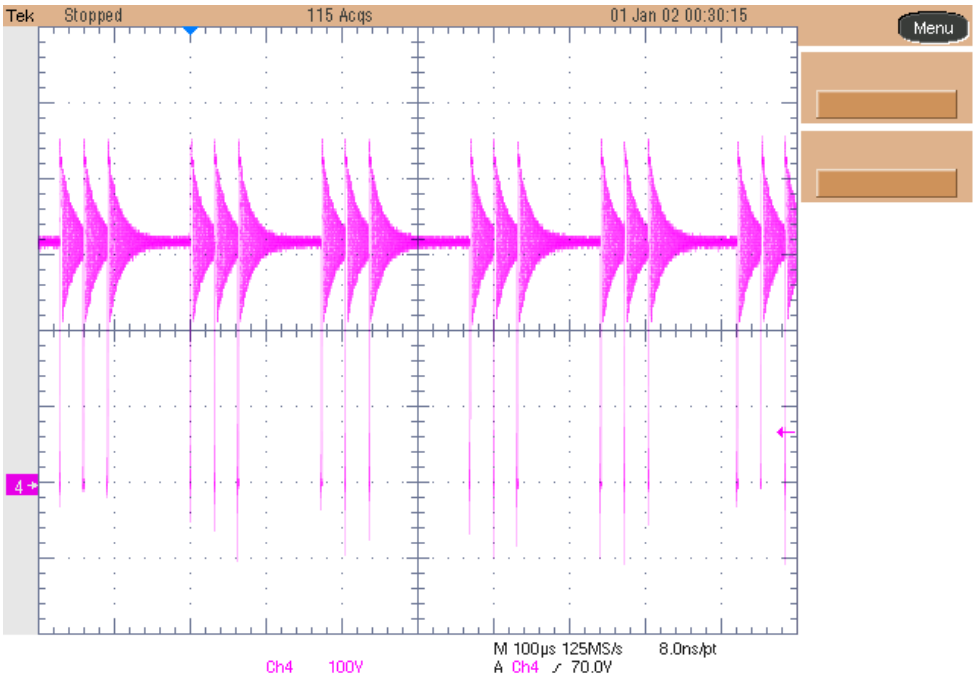
By reducing the load, the converter enters the pulse skipping mode, as shown in the picture below.

Ch4: Drain voltage (100V/div, 10us/div, No BWL).

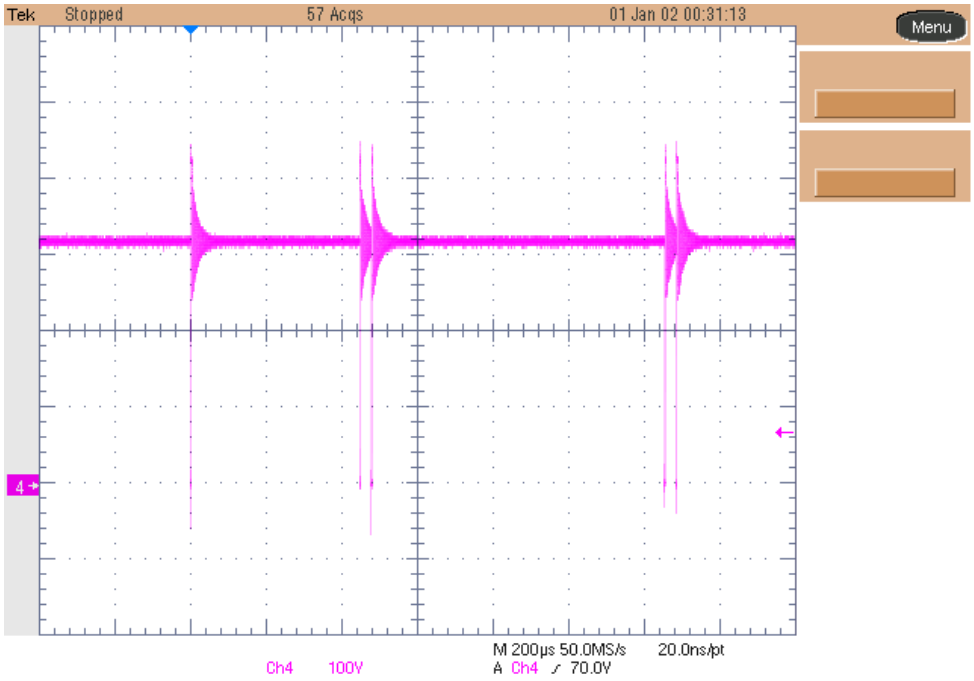
Vin = 320Vdc, Iout=200mA



Ch4: Drain voltage (100V/div, 100usec/div, No BWL).
Vin = 320Vdc, Iout=30mA



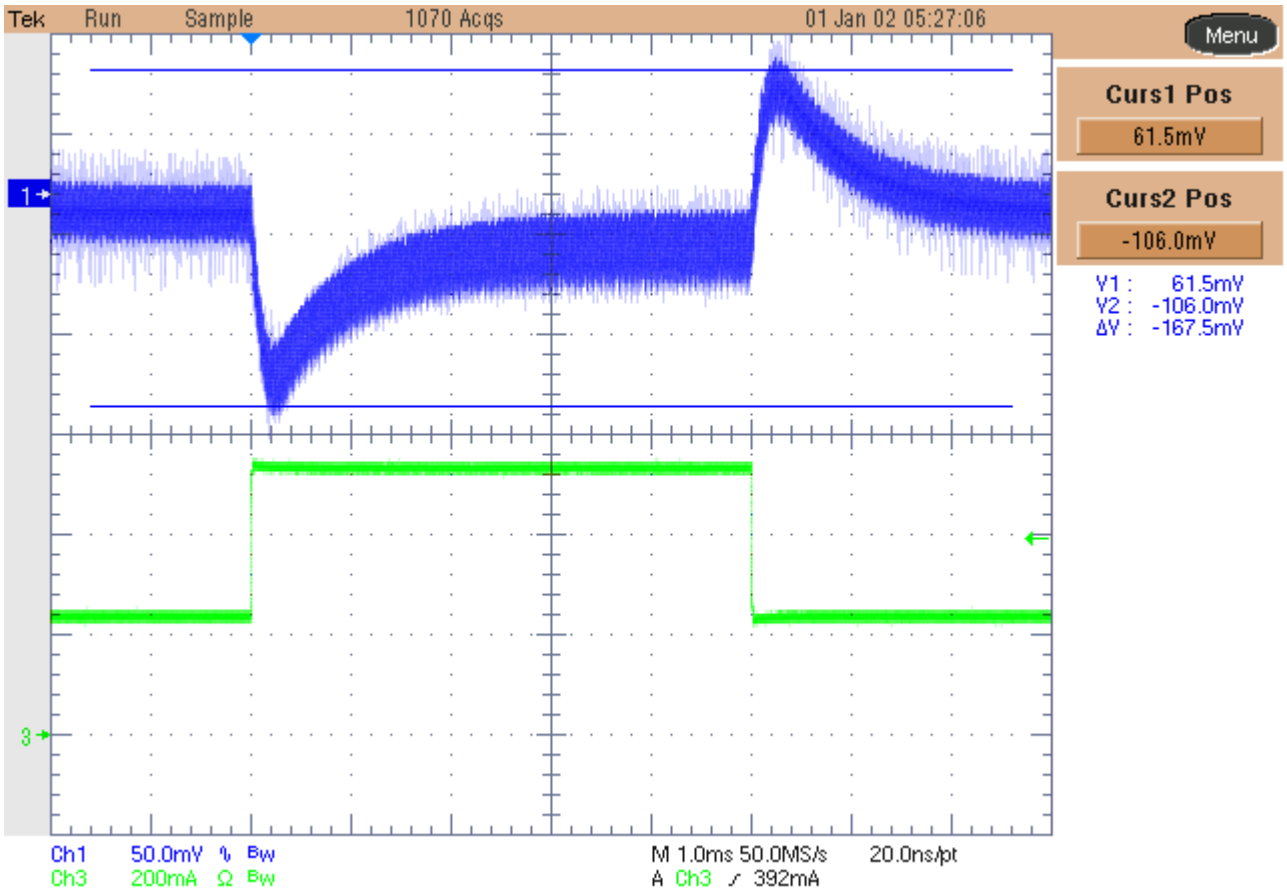
Ch4: Drain voltage (100V/div, 200usec/div, No BWL).
Vin = 320Vdc, No Load



6 Transient Response

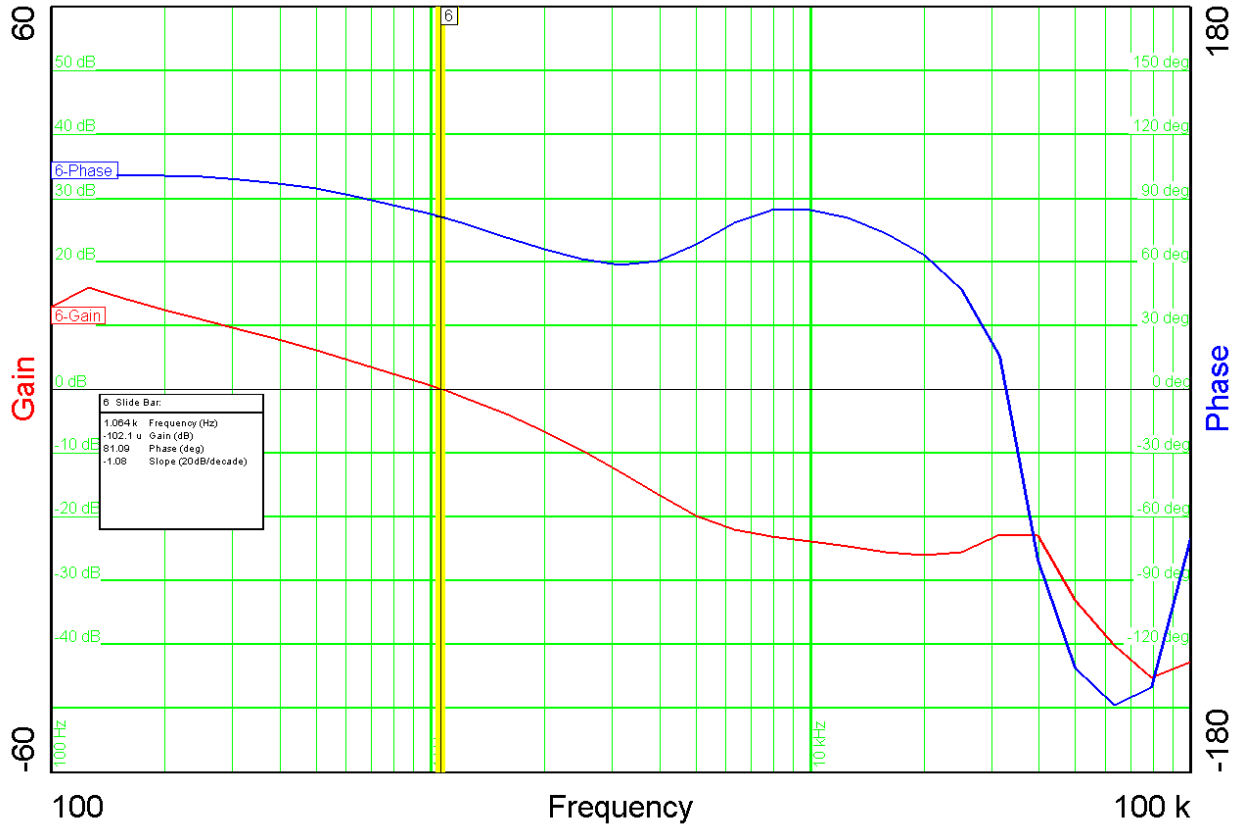
The image below shows the transient response of the output voltage when the load has been switched between 0.25A and 0.55A (45% to 100% of the nominal load). The input voltage was set to 163Vdc.

Ch3: Output Current (200mA/div, 1msec/div., DC coupled, 20MHz BWL)
Ch1: Output Voltage (50mV/div, AC coupled, 20MHz BWL)



7 Loop Response

The graph below shows the bode-plot analysis. The input voltage was set to 320Vdc, the output to 18V and the load to 550mA. The crossover frequency was 1KHz and the phase margin 81 deg., while the gain margin was 22.8dB.



8 Thermal Analysis

Below is described the thermal analysis; the picture has been taken after 30min, while the converter was fully loaded, the input voltage set to 320Vdc, the board placed horizontal on the bench in still air conditions.

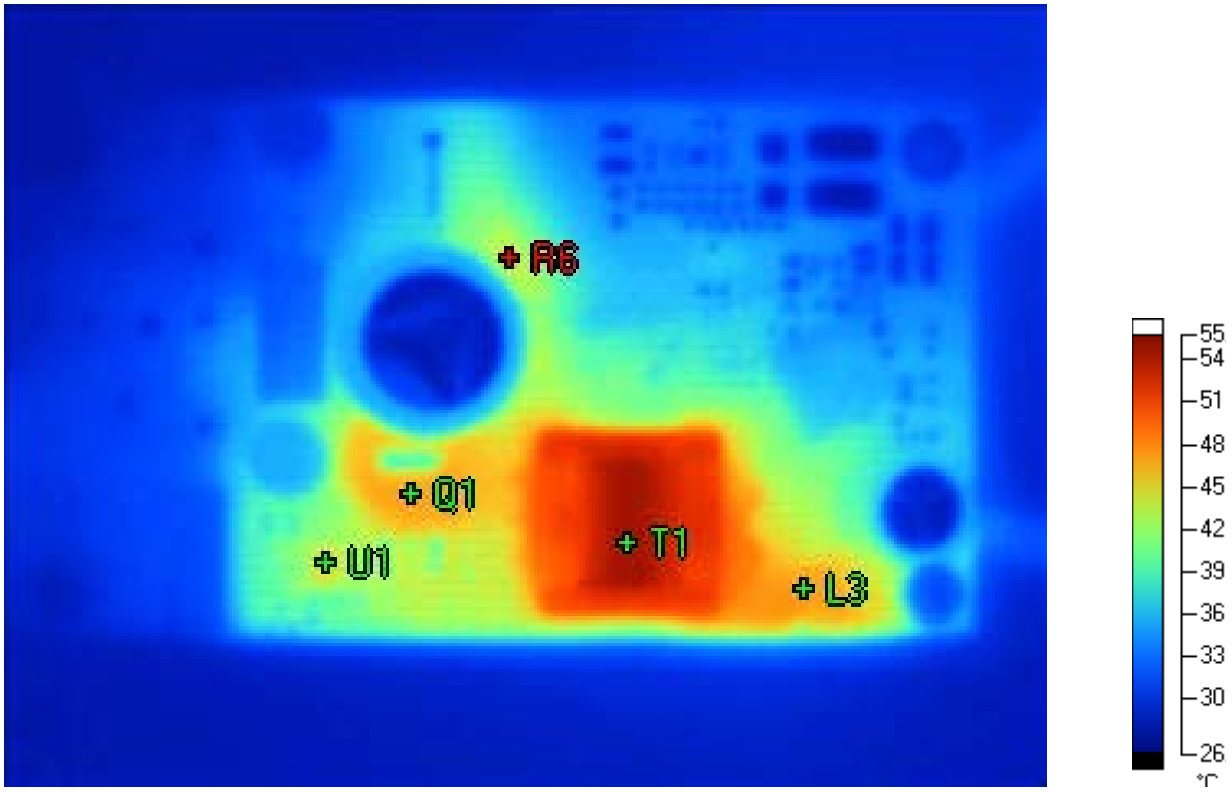


Image Info

Calibration Range	-20.0 °C to 350.0 °C
Camera Model	Ti40FT
Image Range	27.1 °C to 54.8 °C
Manufacturer	Fluke
Camera Serial Number	Ti40FT-070263

Markers

Label	Temperature	Emissivity	Background
T1	54.7 °C	0.95	24.0 °C
Q1	47.2 °C	0.95	24.0 °C
U1	45.0 °C	0.95	24.0 °C
R6	43.5 °C	0.95	24.0 °C
L3	47.1 °C	0.95	24.0 °C

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