User's Guide

LM76005QEVM User's Guide

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The Texas Instruments LM76005QEVM evaluation modules (EVM) help designers evaluate the operation and performance of the LM76005-Q1 wide-input voltage buck regulator. The output voltage for the device offers configurability from 1-V to 95% of V_{IN}, synchronous rectification, PFM, and forced PWM mode and a 200-kHz to 500-kHz adjustable frequency range with a 400-kHz default frequency. It also offers external frequency synchronization, power-good (PG) flag, and a precision enable to program undervoltage lockout (UVLO) and internal compensation. Built-in protection includes current limit, overvoltage and undervoltage protection, and thermal shutdown. The LM76005QEVM is configured for an output voltage of 3.3 V and a switching frequency of 400 kHz. Refer to the *LM76005-Q1 3.5-V to 60-V, 5-A Synchronous Step-Down Voltage Regulator Data Sheet* for additional features, detailed description, and available options.

The EVM contains one DC-DC converter (see Table 1-1).

Table 1-1. Device and Package Configurations

CONVERTER	IC	PACKAGE
U1	LM76005-Q1	(RNP) WQFN-30

Table of Contents

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2 Setup

This section describes the test points and connectors on the EVM and how to properly connect, set up, and use the LM76005QEVM. Refer to Figure 2-1 for a top view of the EVM and relative placement of the different test points and connectors.

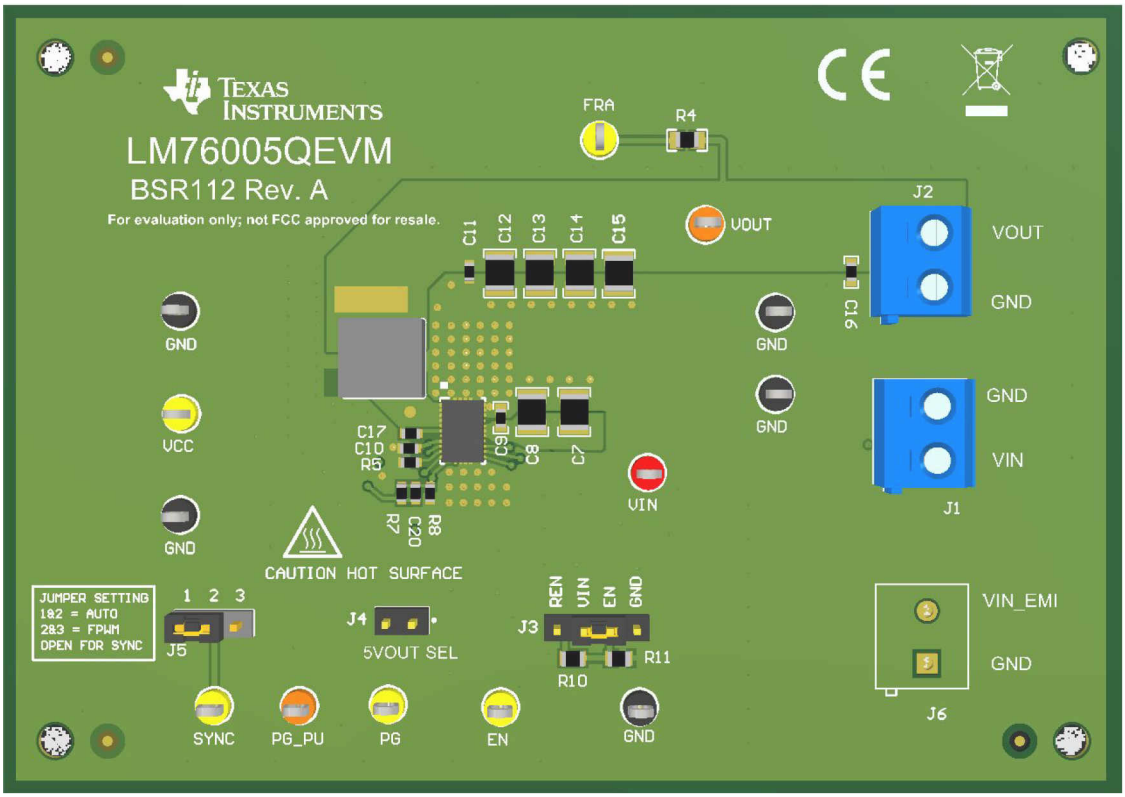


Figure 2-1. Top View of LM76005QEVM

2.1 Input/Output (I/O) Connector Description

VIN – Terminal on J1	The power input terminal for the converter
VOUT – Terminal on J2	The regulated output voltage for the converter
VIN_EMI – Terminal on J6	Used to supply the input voltage through an on board LC filter (if one is needed for conducted EMI/EMC measurement). The L1 and CBULK component pads are located on the bottom side of the EVM. Refer to Figure 3-1 for initial suggestion of component values. J6 and LC filter are not populated on this EVM.
GND – Terminal on J1, J2 and J6	The ground reference for the converter
EN – Testpoint	Used to enable the converter by supplying a voltage greater than 1.2 V (typ) or just to monitor the voltage on this pin whenever a resistor divider is in place (for precision enable applications). The regulator is enabled when V_{IN} > 3.5 V. This threshold can be calculated by:

$$\text{Enable\_Voltage} = \text{VIH\_EN} \cdot \left(1 + \frac{\text{RENT}}{\text{RENB}}\right) \quad (1)$$

PG – Testpoint	Used to monitor the power-good flag. This flag indicates whether the output voltage has reached its regulation point. This pin is an open-drain output that requires a pullup resistor to the appropriate logic voltage (any voltage less than 20 V).
PG_PU – Testpoint	The top connection of an optional 100-kΩ pullup resistor that ties directly to the open-drain PG pin. Supply an appropriate voltage to this test point, or tie it directly to the VOUT test point to observe the PG flag operation if the output voltage is set less than 20 V.
SYNC – Testpoint	The input terminal for an optional external input clock to the converter as well a mode pin for converter. If used, the external clock frequency must be between 200 kHz and 500 kHz.

2.2 Voltage Setup

Set the input voltage (V_{IN}) range for the converter between the operating voltage range of 3.5 V to 60 V. If a load is driven, it must be applied to the VOUT terminal and must not exceed the maximum load current of 5 A for LM76005-Q1.

Note

Please remove R3 and tie BIAS pin to ground if output voltage is set higher than 24 V.

2.3 Operation

For proper operation of the LM76005-Q1, VIN, GND, and VOUT must be properly configured as stated above. In this configuration, the device starts up when power is applied, and the output voltage of the regulator (V_{OUT}) comes up to the proper value. The default setting for output voltage of the LM76005-Q1 is 3.3 V. Other output voltages can be set by replacing the feedback pin resistor dividers R7 and R8; consult the data sheet for proper selection of these resistor values.

The default frequency for the LM76005QEVM is 400 kHz. If other frequencies are desired within the frequency range of 200 kHz and 500 kHz, the R_T resistor value can be changed. See the *LM76005-Q1 3.5-V to 60-V, 5-A Synchronous Step-Down Voltage Regulator Data Sheet* for proper selection of the R_T resistor. Change inductor L2 and total output capacitance for proper control loop operation.

3 Schematic

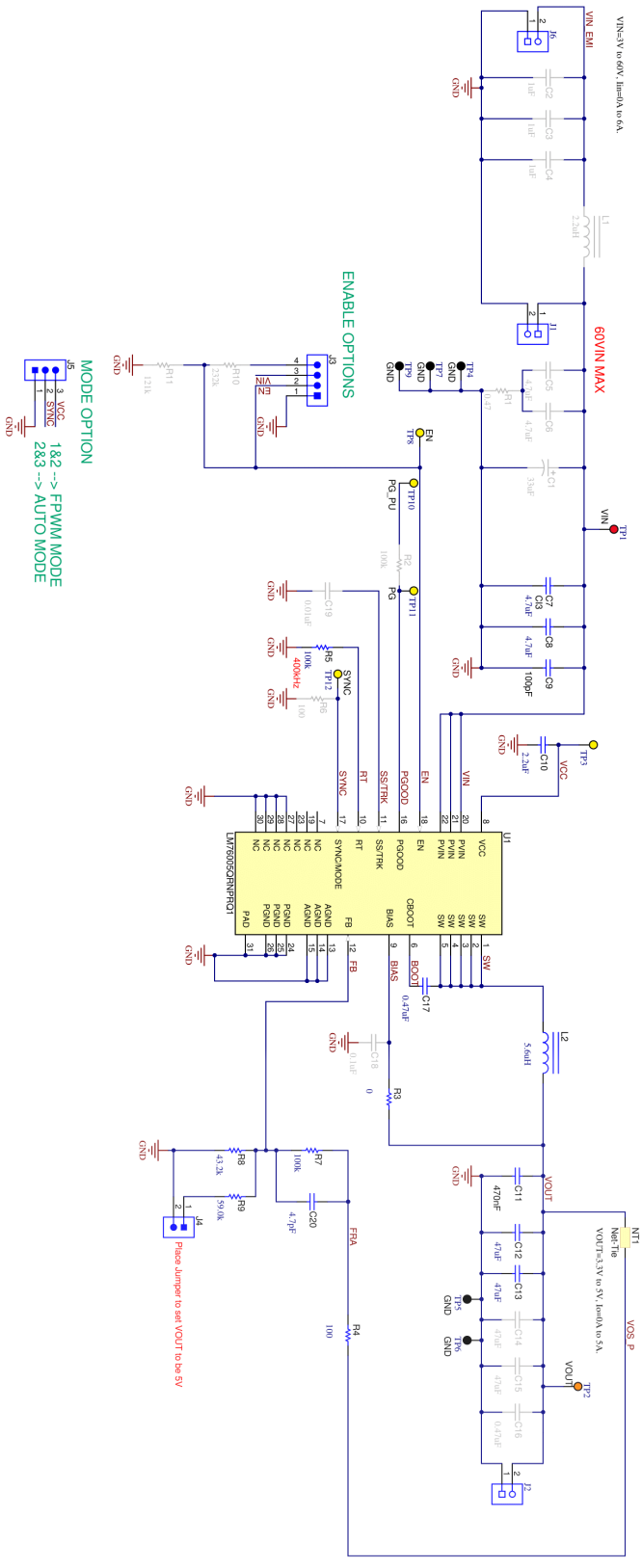


Figure 3-1. LM76005QEVM Schematic

4 Board Layout

Figure 4-1 through Figure 4-5 show the board layout for the LM76005QEVM. The EVM offers resistors, capacitors, and test points to configure the output voltage and precision enable pin, and set frequency and external clock synchronization.

The RNP WQFN-30 package offers an exposed thermal pad which must be soldered to the copper landing on the PCB for optimal thermal performance. The PCB consists of a 4-layer design. There are 2-oz copper planes on the top and bottom and 1-oz copper mid-layer planes to dissipate heat with an array of thermal vias under the thermal pad to connect to all four layers.

Test points have been provided for ease of use to connect the power supply and required load, and monitor critical signals.

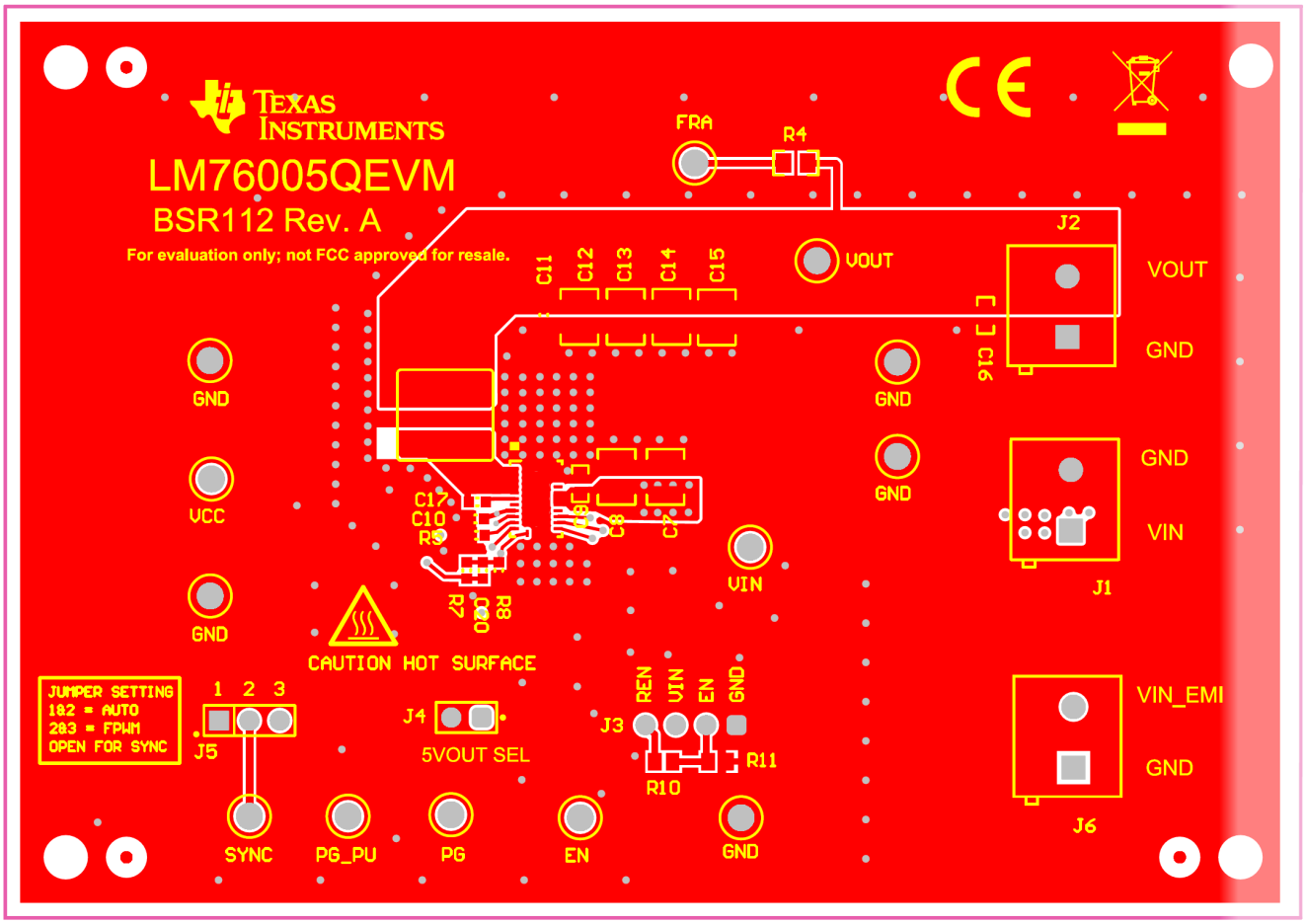


Figure 4-1. Top Silkscreen Layer

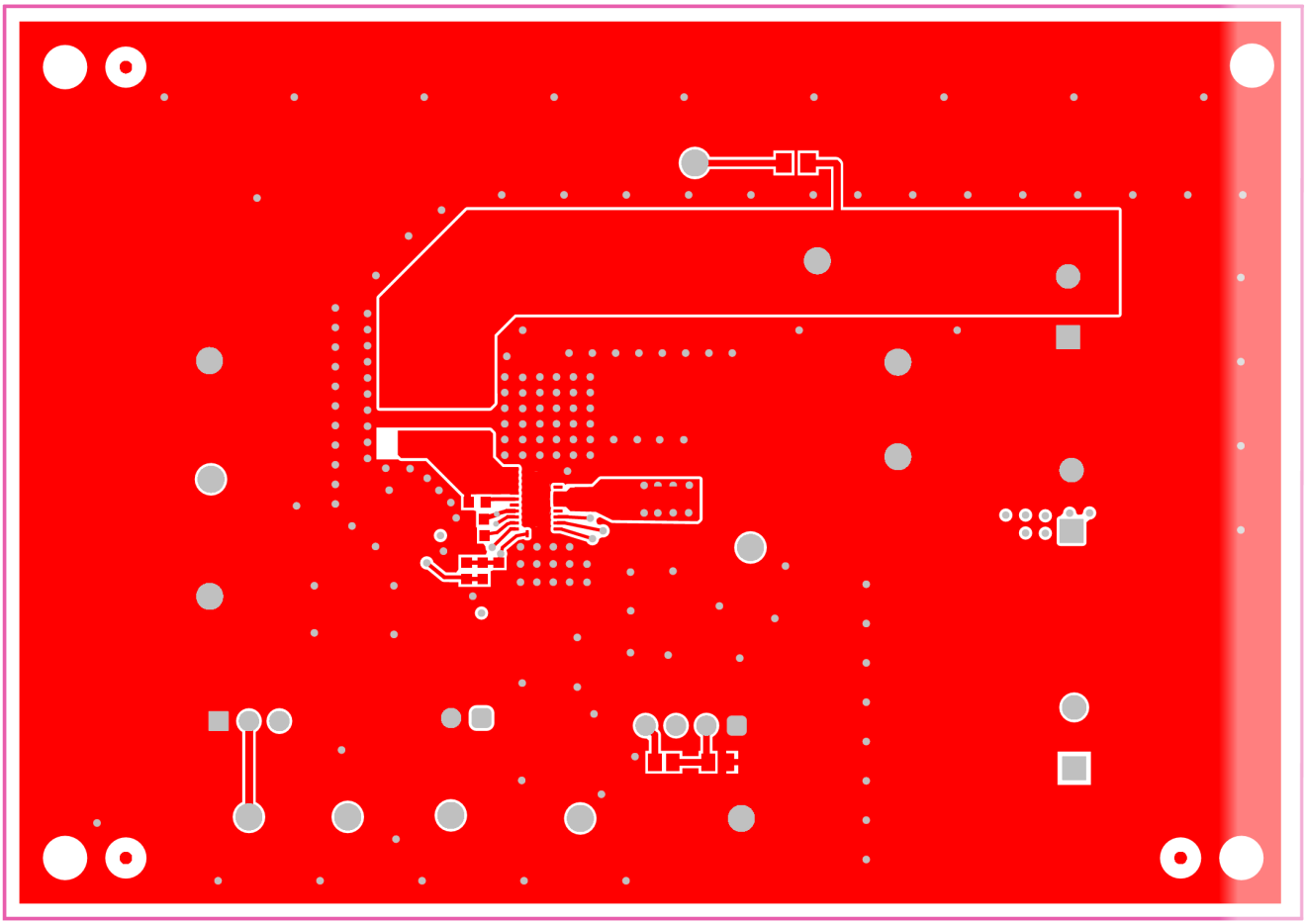


Figure 4-2. Top Layer Routing

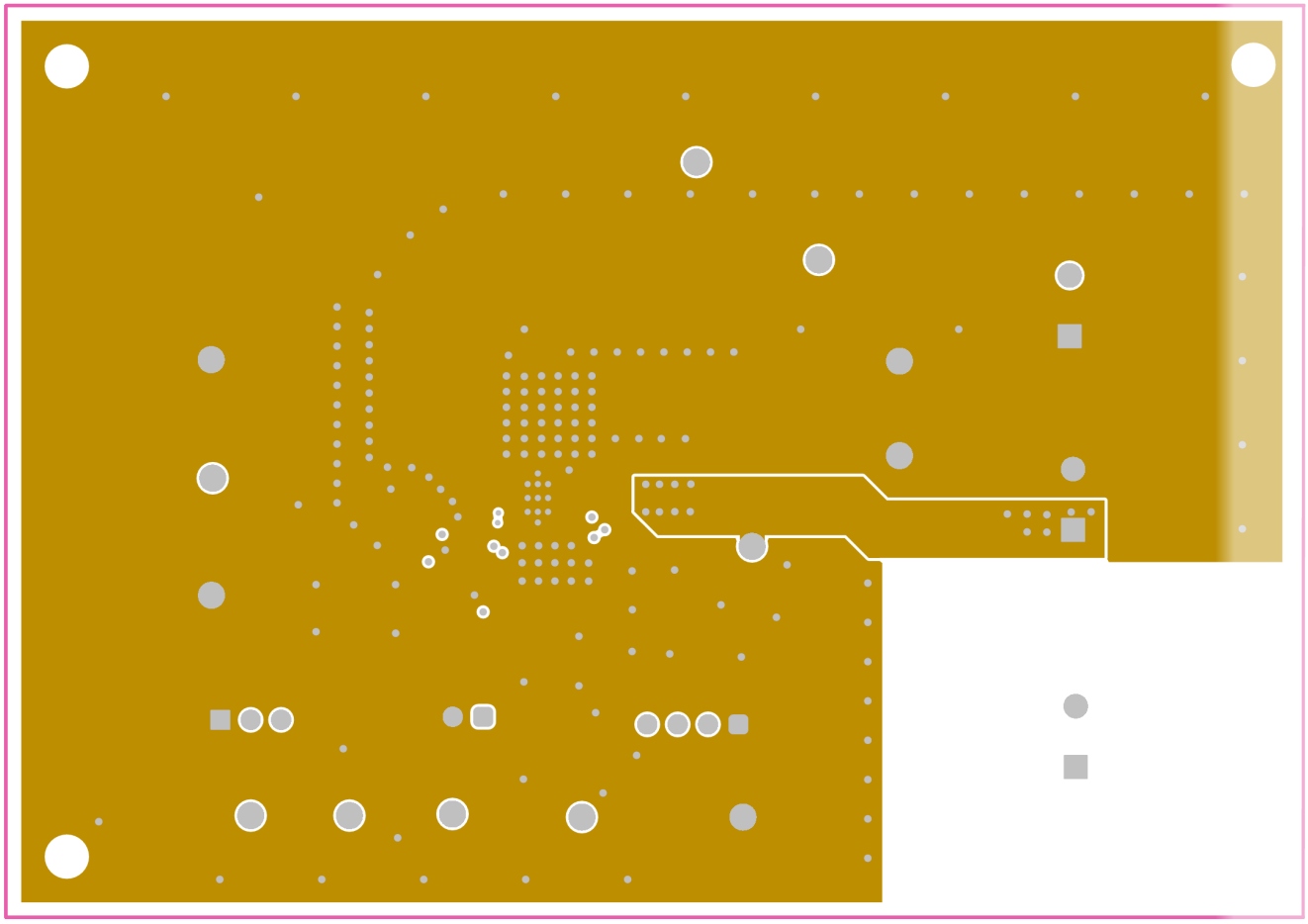


Figure 4-3. Mid Layer 1 Ground Plane

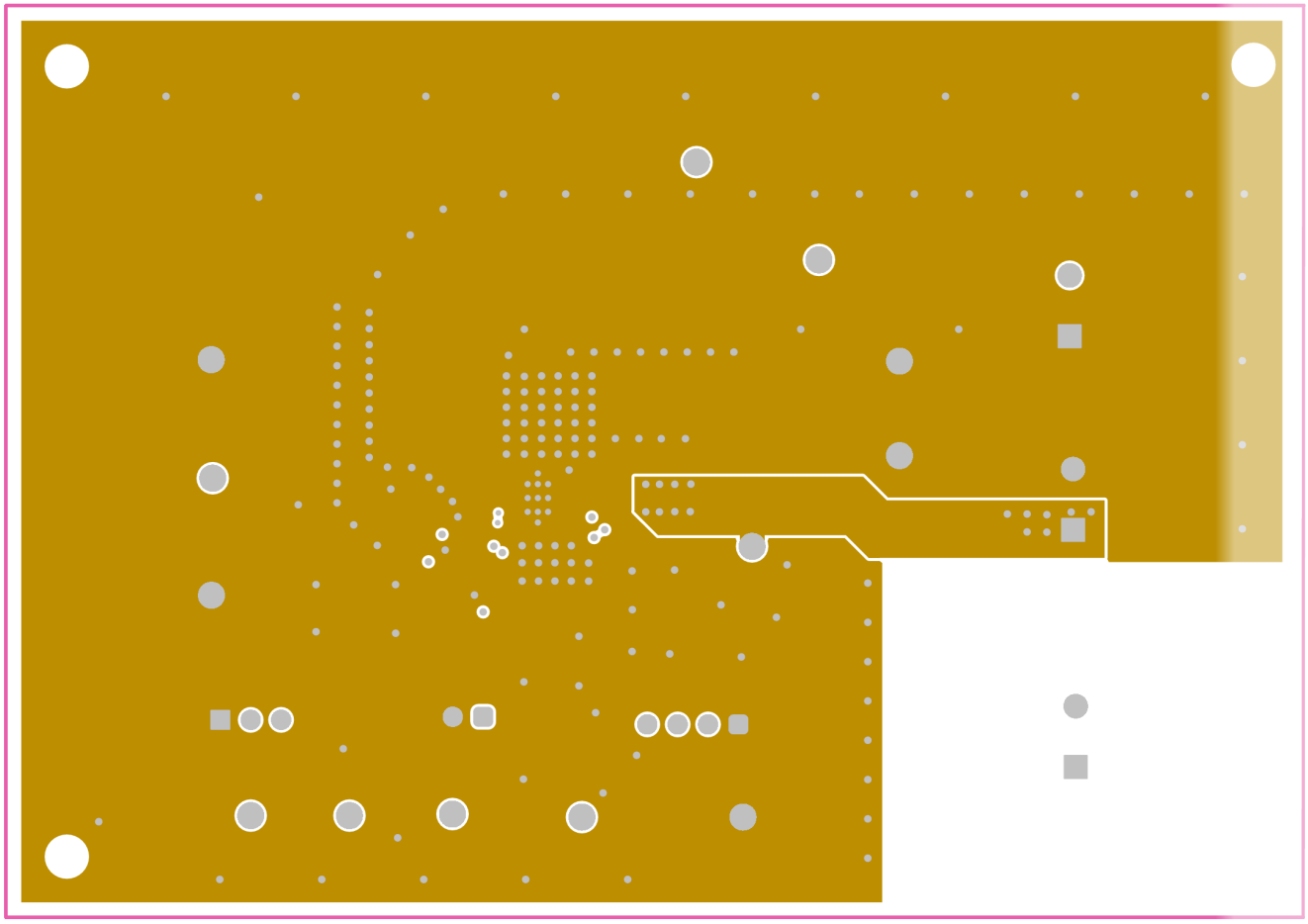


Figure 4-4. Mid Layer 2 Routing

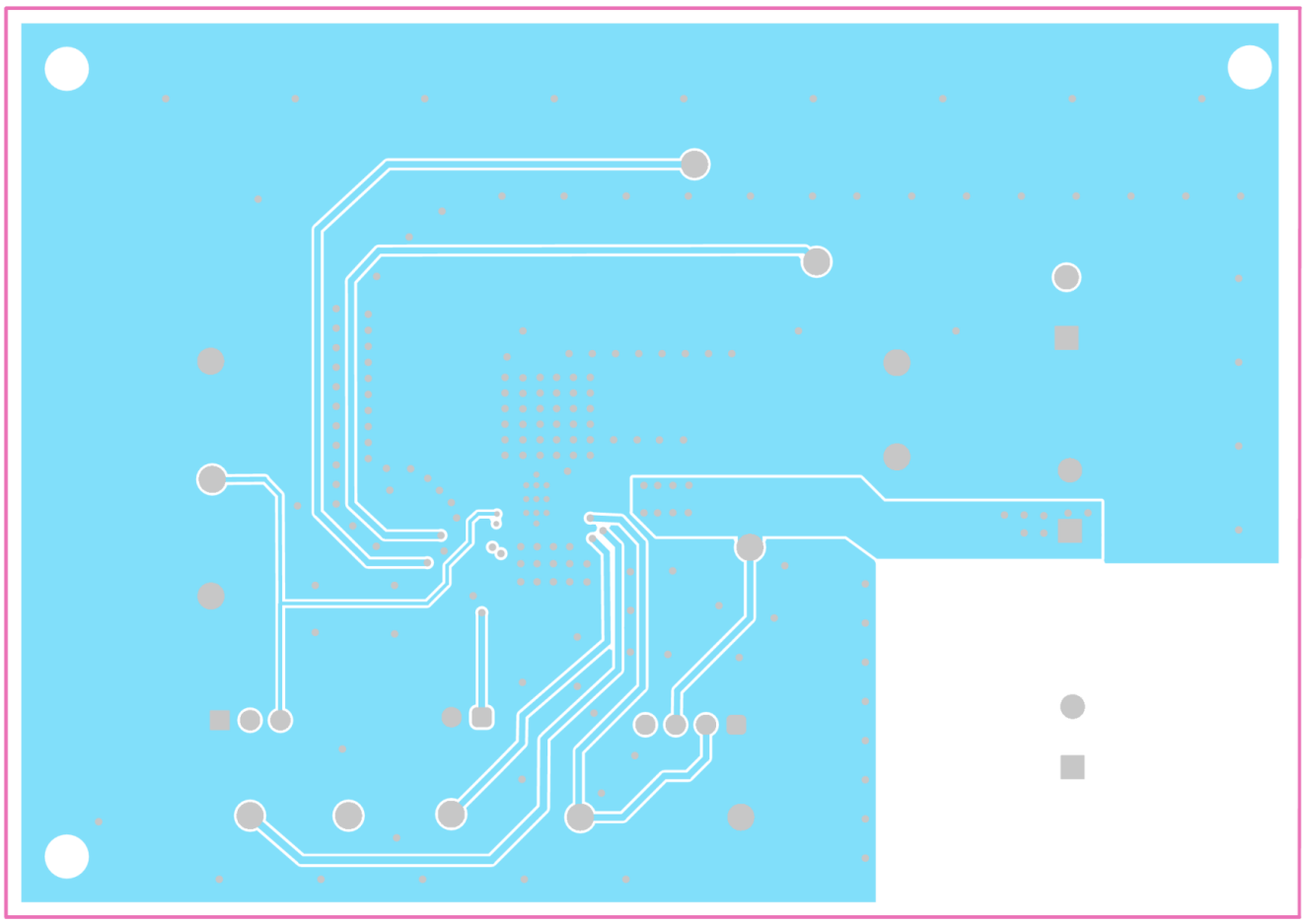


Figure 4-5. Bottom Layer Routing

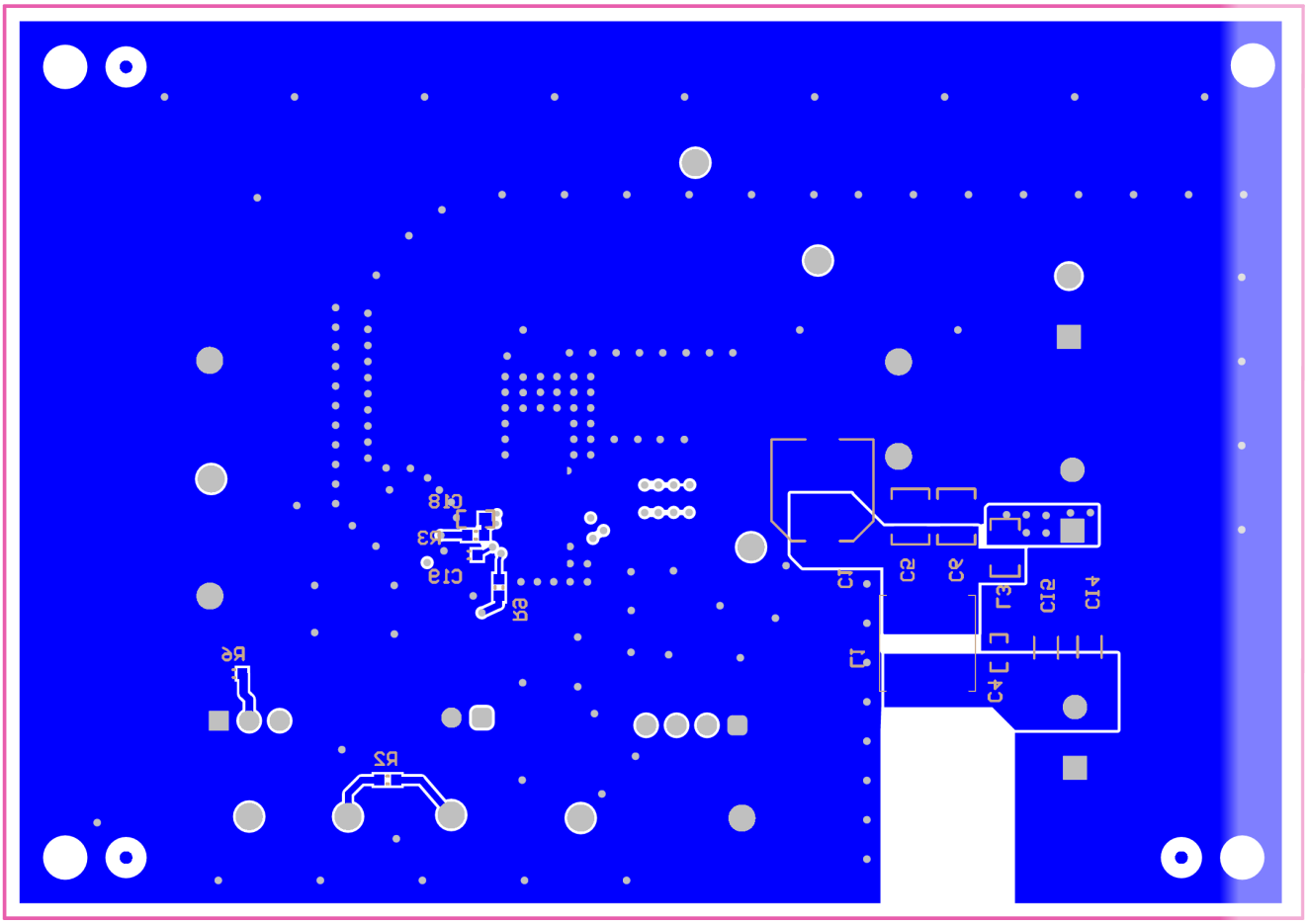


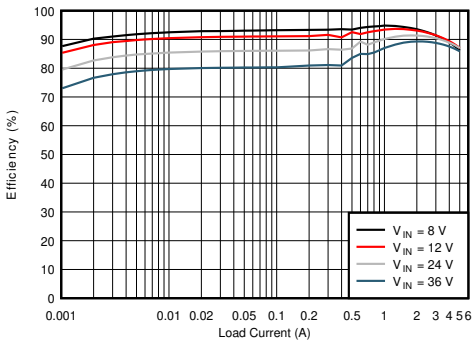
Figure 4-6. Bottom Layer Routing

5 Bill of Materials

Table 5-1. LM76005QEVM Bill of Materials (BOM) for 400-kHz Configuration

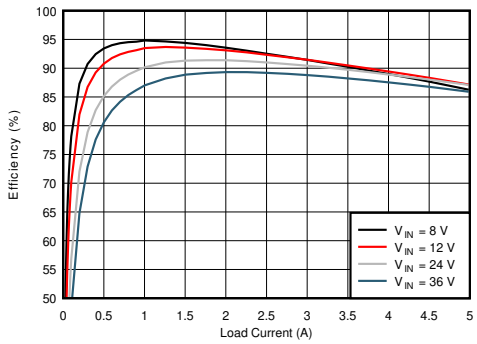
DESIGNATOR	COMMENT	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
PCB	Printed Circuit Board	Printed Circuit Board	Any	BSR112	1
C7, C8		CAP, CERM, 4.7 µF, 100 V, ±10%, X7S, 1210	TDK	C3225X7S2A475K200AB	2
C9, C16, C18		CAP, CERM, 0.1 µF, 100 V, ±10%, X7R, AEC-Q200 Grade 1, 0603	MuRata	GCJ188R72A104KA01D	3
C10	CVCC	CAP, CERM, 2.2 µF, 10 V, ±10%, X7R, 0603	TDK	C1608X7R1A225K080AC	1
C11	CO1	CAP, CERM, 0.47 µF, 50 V, ±10%, X7R, 0603	TDK	C1608X7R1H474K080AC	1
C12, C13, C14, C15		CAP, CERM, 47 µF, 10 V, ±10%, X7R, 1210	MuRata	GRM32ER71A476KE15L	4
C17	CBOOT	CAP, CERM, 0.47 µF, 25 V, ±10%, X5R, 0603	MuRata	GRM188R61E474KA12D	1
C20	CFF	CAP, CERM, 4.7 pF, 50 V, ±5%, C0G/NP0, 0603	AVX	06035A4R7CAT2A	1
J1, J2	VIN, VOUT connector	Terminal Block, 5.08 mm, 2x1, Brass, TH	On-Shore Technology	ED120/2DS	2
J3		Header, 100 mil, 4x1, Gold, TH	Samtec	TSW-104-07-G-S	1
J4		Header, 100 mil, 2x1, Gold, TH	Samtec	TSW-102-07-G-S	1
J5		Header, 100 mil, 3x1, Gold, TH	Samtec	HTSW-103-07-G-S	1
L2		Inductor, Shielded, Composite, 5.6 µH, 11.4 A, 0.01 Ω, SMD	Coilcraft	XAL7070-562MEB	1
R3	RBIAS	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06030000Z0EA	1
R4	RINJ	RES, 100, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	Vishay-Dale	CRCW0805100RFKEA	1
R2, R5, R7		RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100KFKEA	3
R8		RES, 43.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060343K2FKEA	1
R9		RES, 59.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060359K0FKEA	1
R10		RES, 232 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	Vishay-Dale	CRCW0805232KFKEA	1
R11		RES, 121 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	Vishay-Dale	CRCW0805121KFKEA	1
SH-J1, SH-J2	Shunt	Shunt, 100 mil, Gold plated, Black	Samtec	SNT-100-BK-G	2
TP1	VIN	Test Point, Multipurpose, Red, TH	Keystone	5010	1
TP2, TP10	VOUT, PG_PU	Test Point, Multipurpose, Orange, TH	Keystone	5013	2
TP3, TP8, TP11, TP12, TP13	VCC, EN, PG, SYNC, FRA	Test Point, Multipurpose, Yellow, TH	Keystone	5014	5
TP4, TP5, TP6, TP7, TP9	GND	Test Point, Multipurpose, Black, TH	Keystone	5011	5
U1	LM76005QRNPRQ1	3.5-V to 60-V 5-A Synchronous Step-Down Voltage Regulator, RNP0030A (WQFN-30)	Texas Instruments	LM76005QRNPRQ1	1
C1		CAP, AL, 33 µF, 63 V, ±20%, SMD	Chemi-Con	EMVE630ADA330MHA0G	0
C2, C3		CAP, CERM, 1 µF, 100 V, ±10%, X7R, 1206	TDK	C3216X7R2A105K160AA	0
C4		CAP, CERM, 0.1 µF, 100 V, ±10%, X7R, AEC-Q200 Grade 1, 0603	MuRata	C3225X7S2A475K200AB	0
C5, C6		CAP, CERM, 4.7 µF, 100 V, ±10%, X7S, 1210	TDK	C3225X7S2A475K200AB	0
FID1, FID2, FID3, FID4, FID5, FID6	Fiducial	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	0
J6	VIN_EMI connector	Terminal block, 5.08 mm, 2x1, Brass, TH	On-Shore Technology	ED120/2DS	0
L1		Inductor, Shielded, Composite, 2.2 µH, 12.9 A, 0.0137 Ω, SMD	Coilcraft	XAL7030-222MEB	0
L3		Ferrite Bead, 110 Ω @ 100 MHz, 5.4 A, 1206	Wurth Elektronik	74279221111	0
R6		RES, 100, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100RFKEA	0

6 Application Curves



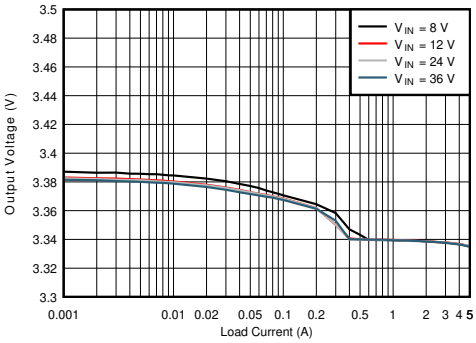
V_{OUT} = 3.3 V f_{SW} = 400 kHz Auto Mode

Figure 6-1. LM76005-Q1 Efficiency



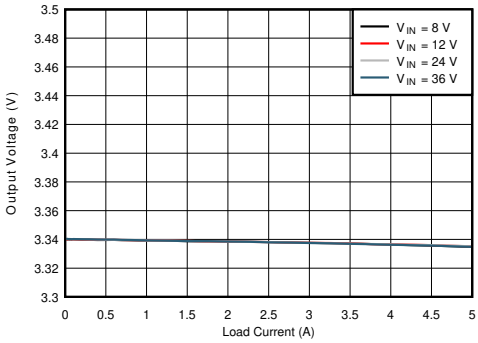
V_{OUT} = 3.3 V f_{SW} = 400 kHz FPWM Mode

Figure 6-2. LM76005-Q1 Efficiency



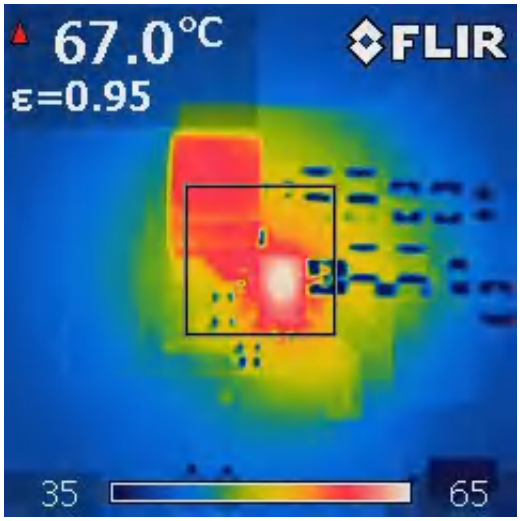
V_{OUT} = 3.3 V f_{SW} = 400 kHz Auto Mode

Figure 6-3. LM76005-Q1 Load and Line Regulation



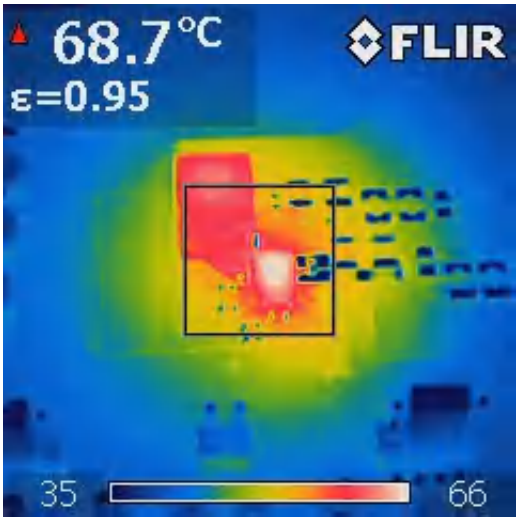
V_{OUT} = 3.3 V f_{SW} = 400 kHz FPWM Mode

Figure 6-4. LM76005-Q1 Load and Line Regulation



V_{IN} = 12 V V_{OUT} = 3.3 V f_{SW} = 400 kHz
5-A Load

Figure 6-5. LM76005-Q1 Thermal Picture



V_{IN} = 24 V V_{OUT} = 3.3 V f_{SW} = 400 kHz
5-A Load

Figure 6-6. LM76005-Q1 Thermal Picture

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 11, 2020 to September 7, 2020 (from Revision * (February 2020) to Revision A (July 2020)) **Page**

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