Technical Reference Manual

LP87564T-Q1 Technical Reference Manual

ABSTRACT

This document provides the default register bit values for the one-time programmable (OTP) bits of the orderable part number LP87564TRNFRQ1.

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Trademarks

1 Introduction

This technical reference manual can be used as a reference for the LP87564T-Q1 default register bits after power up. This technical reference manual does not provide information about the electrical characteristics, external components, package, or the functionality of the device. For this information and the full register map, refer to the datasheet.

Table 1-1 provides the quick overview of each regulator default OTP settings. Sequencing provides an overview of default power up and power down sequence. Table 3-1 lists all the default OTP settings after power up.

Table 1-1. Main OTP Settings for regulators

Description		Bit Name	Value
Device identification	OTP configuration	OTP_ID	89h
BUCK0	Output voltage	BUCK0_VSET	1100 mV
	Enable (ENx pin or I^2C register write)	EN_BUCK0, EN_PIN_CTRL0, BUCK0_EN_PIN_SELECT	EN_BUCK0 bit
	Startup delay	BUCK0_STARTUP_DELAY	0 ms
	Shutdown delay	BUCK0_SHUTDOWN_DELAY	0 ms
	Force PWM	BUCK0_FPWM	Forced PWM
	Peak current limit	ILIM0	5.0 A
	Maximum load current	N/A	4 A
	Slew rate	SLEW_RATE0	1.9 mV/us

Table 1-1. Main OTP Settings for regulators (continued)

Description		Bit Name	Value
BUCK1	Output voltage	BUCK1_VSET	1100 mV
	Enable (ENx pin or I²C register write)	EN_BUCK1, EN_PIN_CTRL1, BUCK1_EN_PIN_SELECT	EN_BUCK1 bit
	Startup delay	BUCK1_STARTUP_DELAY	0 ms
	Shutdown delay	BUCK1_SHUTDOWN_DELAY	0 ms
	Force PWM	BUCK1_FPWM	Forced PWM
	Peak current limit	ILIM1	5.0 A
	Maximum load current	N/A	4 A
	Slew rate	SLEW_RATE1	1.9 mV/us
BUCK2	Output voltage	BUCK2_VSET	1000 mV
	Enable (ENx pin or I²C register write)	EN_BUCK2, EN_PIN_CTRL2, BUCK2_EN_PIN_SELECT	EN1 pin
	Startup delay	BUCK2_STARTUP_DELAY	0 ms
	Shutdown delay	BUCK2_SHUTDOWN_DELAY	0 ms
	Force PWM	BUCK2_FPWM	Forced PWM
	Peak current limit	ILIM2	5.0 A
	Maximum load current	N/A	4 A
	Slew rate	SLEW_RATE2	1.9 mV/us
BUCK3	Output voltage	BUCK3_VSET	1100 mV
	Enable (ENx pin or I²C register write)	EN_BUCK3, EN_PIN_CTRL3, BUCK3_EN_PIN_SELECT	EN_BUCK3 bit
	Startup delay	BUCK3_STARTUP_DELAY	0 ms
	Shutdown delay	BUCK3_SHUTDOWN_DELAY	0 ms
	Force PWM	BUCK3_FPWM	Forced PWM
	Peak current limit	ILIM3	5.0 A
	Maximum load current	N/A	4 A
	Slew rate	SLEW_RATE3	1.9 mV/us
Spread spectrum		EN_SPREAD_SPEC	Enabled
Switching frequency		N/A	2 MHz
I²C address		N/A	65h

2 Sequencing

Figure 2-1 shows the generic power up and power down timing diagram. Startup delay is the delay from the rising edge of ENABLE signal. Shutdown delay is the delay from the falling edge of ENABLE signal. Note that the ENABLE pin assignment/control method and exact power up and power down sequencing depends on the timing values defined in the OTP and specified in Table 2-1.

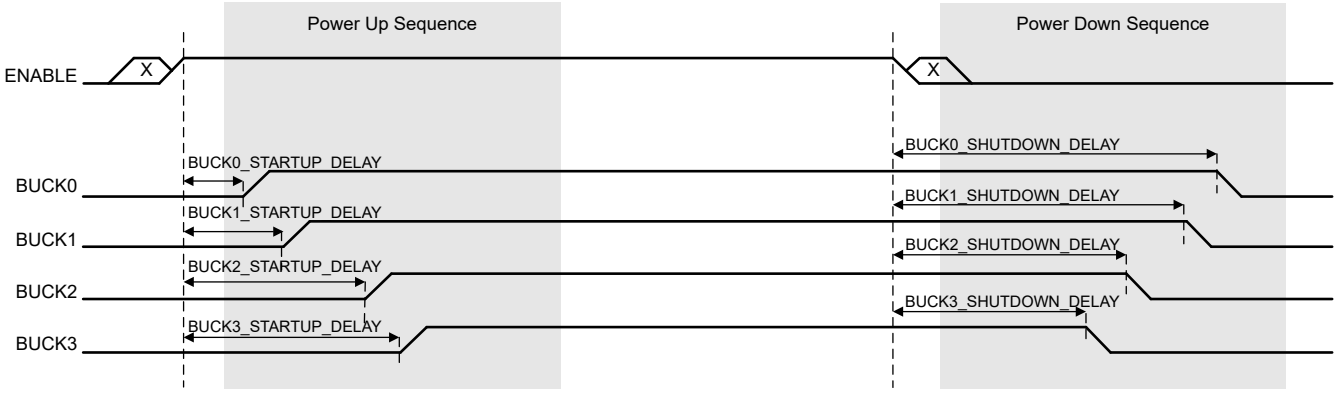

Figure 2-1. Generic Startup and Shutdown Sequences of the Regulators

Table 2-1. Startup and Shutdown Sequencing for LP87564T-Q1

	BUCK0	BUCK1	BUCK2	BUCK3
Control	EN_BUCK0 bit	EN_BUCK1 bit	EN1 pin	EN_BUCK3 bit
Startup delay	0 ms	0 ms	0 ms	0 ms
Shutdown delay	0 ms	0 ms	0 ms	0 ms

3 Register Bits Loaded From OTP Memory

Table 3-1 lists all the default register bit values loaded from the OTP memory during device start-up.

Table 3-1. Summary of Register Values

Address	Register Name	Bit	Value	Description
0x01	OTP_REV	OTP_ID[7:0]	89h	89h
0x02	BUCK0_CTRL1	EN_BUCK0	00h	Disabled
0x02	BUCK0_CTRL1	EN_PIN_CTRL0	00h	EN_BUCK0 bit
0x02	BUCK0_CTRL1	BUCK0_EN_PIN_SELECT[1:0]	00h	EN_BUCK0 bit AND EN1 pin
0x02	BUCK0_CTRL1	BUCK0_FPWM	01h	Forced PWM
0x02	BUCK0_CTRL1	BUCK0_FPWM_MP	00h	Automatic phase adding and shedding
0x03	BUCK0_CTRL2	ILIM0[2:0]	07h	5.0 A
0x03	BUCK0_CTRL2	SLEW_RATE0[2:0]	05h	1.9 mV/us
0x04	BUCK1_CTRL1	EN_BUCK1	00h	Disabled
0x04	BUCK1_CTRL1	EN_PIN_CTRL1	00h	EN_BUCK1 bit
0x04	BUCK1_CTRL1	BUCK1_EN_PIN_SELECT[1:0]	00h	EN_BUCK1 bit AND EN1 pin
0x04	BUCK1_CTRL1	BUCK1_FPWM	01h	Forced PWM
0x05	BUCK1_CTRL2	ILIM1[2:0]	07h	5.0 A
0x05	BUCK1_CTRL2	SLEW_RATE1[2:0]	05h	1.9 mV/us
0x06	BUCK2_CTRL1	EN_BUCK2	01h	Enabled
0x06	BUCK2_CTRL1	EN_PIN_CTRL2	01h	EN1 pin
0x06	BUCK2_CTRL1	BUCK2_EN_PIN_SELECT[1:0]	00h	EN_BUCK2 bit AND EN1 pin
0x06	BUCK2_CTRL1	BUCK2_FPWM	01h	Forced PWM
0x06	BUCK2_CTRL1	BUCK2_FPWM_MP	00h	Automatic phase adding and shedding
0x07	BUCK2_CTRL2	ILIM2[2:0]	07h	5.0 A
0x07	BUCK2_CTRL2	SLEW_RATE2[2:0]	05h	1.9 mV/us
0x08	BUCK3_CTRL1	EN_BUCK3	00h	Disabled
0x08	BUCK3_CTRL1	EN_PIN_CTRL3	00h	EN_BUCK3 bit
0x08	BUCK3_CTRL1	BUCK3_EN_PIN_SELECT[1:0]	00h	EN_BUCK3 bit AND EN1 pin
0x08	BUCK3_CTRL1	BUCK3_FPWM	01h	Forced PWM
0x09	BUCK3_CTRL2	ILIM3[2:0]	07h	5.0 A
0x09	BUCK3_CTRL2	SLEW_RATE3[2:0]	05h	1.9 mV/us
0x0A	BUCK0_VOUT	BUCK0_VSET[7:0]	61h	1100 mV
0x0C	BUCK1_VOUT	BUCK1_VSET[7:0]	61h	1100 mV
0x0E	BUCK2_VOUT	BUCK2_VSET[7:0]	4Dh	1000 mV
0x10	BUCK3_VOUT	BUCK3_VSET[7:0]	61h	1100 mV
0x12	BUCK0_DELAY	BUCK0_SHUTDOWN_DELAY[3:0]	00h	0 ms
0x12	BUCK0_DELAY	BUCK0_STARTUP_DELAY[3:0]	00h	0 ms
0x13	BUCK1_DELAY	BUCK1_SHUTDOWN_DELAY[3:0]	00h	0 ms
0x13	BUCK1_DELAY	BUCK1_STARTUP_DELAY[3:0]	00h	0 ms
0x14	BUCK2_DELAY	BUCK2_SHUTDOWN_DELAY[3:0]	00h	0 ms
0x14	BUCK2_DELAY	BUCK2_STARTUP_DELAY[3:0]	00h	0 ms
0x15	BUCK3_DELAY	BUCK3_SHUTDOWN_DELAY[3:0]	00h	0 ms
0x15	BUCK3_DELAY	BUCK3_STARTUP_DELAY[3:0]	00h	0 ms
0x16	GPIO2_DELAY	GPIO2_SHUTDOWN_DELAY[3:0]	00h	0 ms
0x16	GPIO2_DELAY	GPIO2_STARTUP_DELAY[3:0]	00h	0 ms
0x17	GPIO3_DELAY	GPIO3_SHUTDOWN_DELAY[3:0]	00h	0 ms
0x17	GPIO3_DELAY	GPIO3_STARTUP_DELAY[3:0]	00h	0 ms
0x19	CONFIG	DOUBLE_DELAY	00h	0-4.8 ms with 0.32 ms steps

Table 3-1. Summary of Register Values (continued)

Address	Register Name	Bit	Value	Description
0x19	CONFIG	CLKIN_PD	01h	Enabled
0x19	CONFIG	EN4_PD	00h	Disabled
0x19	CONFIG	EN3_PD	01h	Enabled
0x19	CONFIG	TDIE_WARN_LEVEL	01h	137C
0x19	CONFIG	EN2_PD	01h	Enabled
0x19	CONFIG	EN1_PD	01h	Enabled
0x21	TOP_MASK1	GPIO_MASK	01h	Masked
0x21	TOP_MASK1	SYNC_CLK_MASK	01h	Masked
0x21	TOP_MASK1	TDIE_WARN_MASK	00h	Unmasked
0x21	TOP_MASK1	I_LOAD_READY_MASK	01h	Masked
0x22	TOP_MASK2	RESET_REG_MASK	01h	Masked
0x23	BUCK_0_1_MASK	BUCK1_PG_MASK	01h	Masked
0x23	BUCK_0_1_MASK	BUCK1_ILIM_MASK	01h	Masked
0x23	BUCK_0_1_MASK	BUCK0_PG_MASK	01h	Masked
0x23	BUCK_0_1_MASK	BUCK0_ILIM_MASK	01h	Masked
0x24	BUCK_2_3_MASK	BUCK3_PG_MASK	01h	Masked
0x24	BUCK_2_3_MASK	BUCK3_ILIM_MASK	01h	Masked
0x24	BUCK_2_3_MASK	BUCK2_PG_MASK	01h	Masked
0x24	BUCK_2_3_MASK	BUCK2_ILIM_MASK	01h	Masked
0x28	PGOOD_CTRL1	PG3_SEL[1:0]	00h	Masked
0x28	PGOOD_CTRL1	PG2_SEL[1:0]	01h	Power-Good-threshold voltage
0x28	PGOOD_CTRL1	PG1_SEL[1:0]	00h	Masked
0x28	PGOOD_CTRL1	PG0_SEL[1:0]	00h	Masked
0x29	PGOOD_CTRL2	HALF_DELAY	01h	0-4.8 ms with 0.32 ms steps
0x29	PGOOD_CTRL2	EN_PG0_NINT	00h	PGOOD signal NOT included to nINT signal
0x29	PGOOD_CTRL2	PGOOD_SET_DELAY	00h	4-10 us
0x29	PGOOD_CTRL2	EN_PGFLT_STAT	00h	Live status of monitored voltage outputs
0x29	PGOOD_CTRL2	PGOOD_WINDOW	01h	Overvoltage and undervoltage monitoring
0x29	PGOOD_CTRL2	PGOOD_OD	01h	Open-drain output
0x29	PGOOD_CTRL2	PGOOD_POL	00h	HIGH
0x2B	PLL_CTRL	PLL_MODE[1:0]	00h	PLL disabled, internal RC oscillator
0x2B	PLL_CTRL	EXT_CLK_FREQ[4:0]	01h	2 MHz
0x2C	PIN_FUNCTION	EN_SPREAD_SPEC	01h	Enabled
0x2C	PIN_FUNCTION	EN_PIN_CTRL_GPIO3	01h	GPIO3_OUT bit AND ENx pin
0x2C	PIN_FUNCTION	EN_PIN_SELECT_GPIO3	00h	GPIO3_SEL bit AND EN1 pin
0x2C	PIN_FUNCTION	EN_PIN_CTRL_GPIO2	01h	GPIO2_OUT bit AND ENx pin
0x2C	PIN_FUNCTION	EN_PIN_SELECT_GPIO2	00h	GPIO2_SEL bit AND EN1 pin
0x2C	PIN_FUNCTION	GPIO3_SEL	01h	GPIO3
0x2C	PIN_FUNCTION	GPIO2_SEL	01h	GPIO2
0x2C	PIN_FUNCTION	GPIO1_SEL	00h	EN1
0x2D	GPIO_CONFIG	GPIO3_OD	01h	Open-drain output
0x2D	GPIO_CONFIG	GPIO2_OD	01h	Open-drain output
0x2D	GPIO_CONFIG	GPIO1_OD	00h	Push-pull output
0x2D	GPIO_CONFIG	GPIO3_DIR	00h	Input
0x2D	GPIO_CONFIG	GPIO2_DIR	00h	Input
0x2D	GPIO_CONFIG	GPIO1_DIR	00h	Input
0x2F	GPIO_OUT	GPIO3_OUT	01h	Logic high level

Table 3-1. Summary of Register Values (continued)

Address	Register Name	Bit	Value	Description
0x2F	GPIO_OUT	GPIO2_OUT	01h	Logic high level

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