User's Guide

LM5171 Evaluaton Module

ABSTRACT

The LM5171EVM-BIDIR Evaluation Module (EVM) is designed to showcase the LM5171 high performance dual-channel bidirectional controller, which is an excellent choice for, but not limited to, the automotive 48-V to 12-V dual battery system applications.

The EVM can be configured as a bidirectional power converter in the form of either a current source or voltage source. The direction of power flow can be controlled either by an external command signal or by the on-board jumper. Through the onboard interface headers, the EVM can be operated by a DSP, an FPGA, an MCU, or other digital controllers. Two EVMs can be paralleled to make a 3 or 4 phases interleaved converter for higher power. More EVMs can be paralleled for greater number of phases. Many convenient jumper headers are also included for versatile configurations of the EVM.

Refer to the *LM5171 Multiphase Bidirectional Current Controller Data Sheet* (SNVSCM3) for detailed technical information of the LM5171 device.

CAUTION

Read the user's guide before use.

CAUTION

Hot surface! Contact can cause burns. Do not touch!

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Trademarks

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1 Features and Electrical Performance

The EVM supports the following features and performance capabilities:

- Input operating voltage ranges
  - The 48VDC-port 6 V to 70 V, in the buck mode
  - The 12VDC-port 6 V to 48 V, in the boost mode
- Output voltage regulation (with the onboard outer voltage regulation activated)
  - 14.5-V output voltage at the 12VDC-port, in the buck mode
  - 50.5-V output voltage at the 48VDC-port, in the boost mode
- Operating current
  - 60-Adc maximum from or into the 12VDC-port
  - Typical 1% current regulation accuracy
  - Typical 1% current monitor accuracy
- Switching frequency:
  - Standalone Fsw = 100 kHz
  - Able to synchronize to an external clock from 80 kHz to 120 kHz
- Maximum efficiency: >97%
- OVP threshold
  - 75 V at the 48VDC-port
  - 24 V at the 12VDC-port
- Other convenient features
  - Optional onboard SEPIC converter providing +10V supply
  - Onboard 5 V bias voltages and 3.5V voltage reference
  - Onboard LM26LV Temperature Sensors Monitoring Local Temperatures of Power MOSFETs, with optional over temperature shutdown and LED indicator
  - LED indicators of buck and boost operating modes
  - Optional channel current shunt AC filters for accurate Digital Voltmeter (DVM) Reading
  - Onboard two stage RC Filter for PWM input to ISET (J33)
  - ISET voltage clamp input (J43)
  - Square wave input for dithering (J14)
  - I^2C interface for monitoring and diagnose (J31)
  - Output voltage tracking input (J37)

The electrical performance of the EVM is show in Table 1-1. Figure 2-1 shows the simplified EVM schematic.

Table 1-1. Electrical Performance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
48VDC-Port	Buck mode operation (DIR > 2 V)	6	48	70	V
12VDC-Port	Boost mode operation (DIR < 1 V)	6	12	48	V
OUTPUT CHARACTERISTICS					
Current delivery	12VDC-Port input or output current (dual-channel enabled)	0		60	A
Current regulation accuracy	12VDC-Port current vs ISETA command voltage		1%		
Channel current monitor accuracy	When onboard IOUT1 and IOUT2 termination filter activated		1%		
48VDC-Port	Boost mode operation (DIR < 1 V, onboard analog output voltage loop closed)		50.5		V
12VDC-Port	Buck mode operation (DIR > 2 V, onboard analog output voltage loop closed)		14.5		V
SYSTEM CHARACTERISTICS					
Switching frequency			100		kHz
External clock synchronization		80		120	kHz
Full load efficiency			97%		
Junction temperature, T_J		–40		150	°C

2 Setup

2.1 EVM Configurations

Figure 2-2 shows the EVM board top view and circuit layout partitions. The EVM has the following ports:

- 48VDC-Port: Connected to 48-V battery rail
- 12VDC-Port: Connected to 12-V battery rail
- J17 (60-Pin Header): Interfacing the external control commands or MCU
- J18 (60-Pin Header): Interfacing J17 of the secondary EVM in a 4-phase system consisting of two EVMs
- Channel Current Setting: Analog programming at J17-pin 11, and digital programming at J17-pin 13
- I^2C interface for diagnosis and monitory functions at J45.

Table 2-1 through Table 2-4 list the functions of the EVM jumpers and headers. The EVM jumpers and headers offer flexible configurability and programmability of the EVM for various use cases including but not limited to the following:

- A unidirectional or bidirectional voltage source
- A unidirectional or bidirectional current source
- Dynamic phase adding and shedding in a 4-phase system consisting of two EVMs
- Dynamic MOSFETs dead time adjustment
- Individual channel current monitoring or total current monitoring
- Synchronization to external clock
- External shutdown command through DT/nSD pin (J17-pin45)

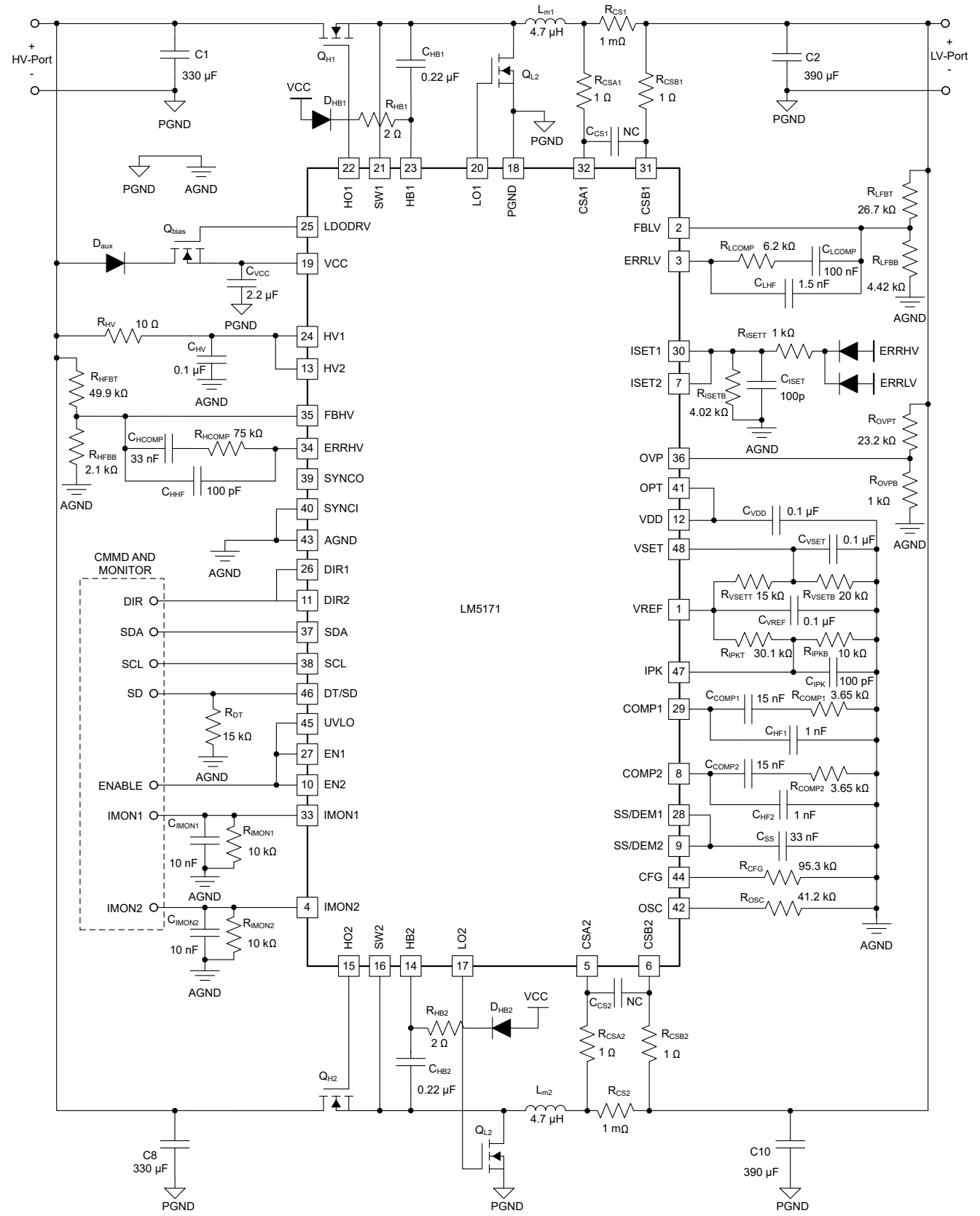

Figure 2-1. Simplified EVM Schematic

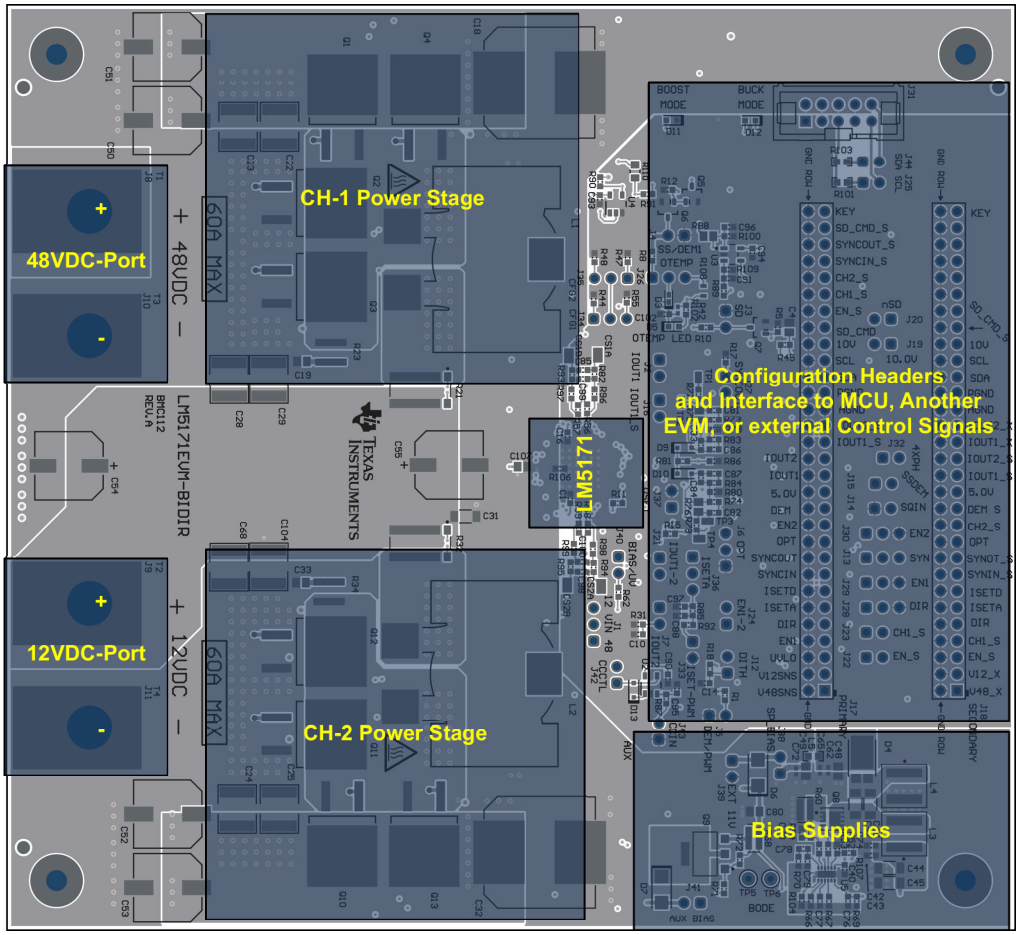

Figure 2-2. EVM Board Top View and Layout Partitions

Table 2-1. Three-Pin Header Settings

HEADER	SIGNAL	PINS	FUNCTION DESCRIPTION	DEFAULT
J1	UVLO	--(1)	External UVLO command through J17	
		(1,2)(2)	48VDC-Port UVLO Control	Y
		(2,3)(3)	12VDC-Port UVLO Control	
J6	OPT	--	External interleaving control through J17	
		(1,2)	CH-2 240 degree delay from CH-1	
		(2,3)	CH-2 180 degree delay from CH-1	Y
J13	SYNC	--	Secondary EVM not sync to main EVM	Y
		(1,2)	Secondary EVM sync to main EVM	
		(2,3)	Secondary EVM sync to external clock	
J26	OTEMP	--	Onboard Over temperature protection inactive	Y
		(1,2)	Over temperature protection in hiccup mode	
		(2,3)	Over temperature protection in latched shutdown	
J28	DIR	--	External DIR control through J17	
		(1,2)	Onboard DIR command for buck operation	Y
		(2,3)	Onboard DIR command for boost operation	
J29	EN1	--	External CH-1 enable control through J17	
		(1,2)	Onboard CH-1 enable	Y
		(2,3)	Onboard CH-1 inactive	
J30	EN2	--	External CH-2 enable control through J17, overridden by J24.	Y
		(1,2)	Onboard CH-2 enable	
		(2,3)	Onboard CH-2 inactive	
J34	CFG	--	I^2C address set to 0x0 is not selected	
		(1,2)	I^2C address set to 0x0, and select inductor current monitor	Y
		(2,3)	I^2C address set to 0x0, and select output current monitor	
J35	CFG	--	I^2C address set to 0x1 is not selected	Y
		(1,2)	I^2C address set to 0x1, and select inductor current monitor	
		(2,3)	I^2C address set to 0x1, and select output current monitor	
J36	ISET	--	External ISET control through J17	
		(1,2)	Onboard voltage loop	Y
		(2,3)	External digital voltage loop	

(1) – = All jumper pins open.
(2) (1,2) = Pins 1 and 2 closed.
(3) (2,3) = Pins 2 and 3 closed.

Table 2-2. Two-Pin Header Settings

HEADER	SIGNAL	PINS	FUNCTION DESCRIPTION	DEFAULT
J2	IMON1	C(1)	IMON1 filter connected	Y
		O(2)	IMON1 filter disconnected	
J3	nSD	C	Shutdown	
		O	External shutdown via J17	Y
J4	SS/DEM1	C	CH-1 set to DEM	Y
		O	CH-1 set to FPWM	
J5	SS/DEM2	C	CH-2 set to DEM	Y
		O	CH-2 set to FPWM	
J7	IMON2	C	IMON2 filter connected	Y
		O	IMON2 filter disconnected	
J12	Dithering	C	dithering control allowed	
		O	dithering control not allowed	Y
J14	SQIN	C	Not allowed	
		O	square wave input for dithering control	Y
J15	SS/DEM1 & SS/DEM2	C	SS/DEM1 & SS/DEM2 are connected	Y
		O	SS/DEM1 & SS/DEM2 are independent	
J16	Main & Secondary EVM IMON1	C	Main EVM & Secondary EVM IMON1 signal merged	
		O	Main EVM & Secondary EVM IMON1 signal not merged	Y
J19	Main & Secondary EVM 10 V VCC	C	Main EVM & Secondary EVM 10 V VCC connected	
		O	Main EVM & Secondary EVM 10 V VCC not connected	Y
J20	Main & Secondary EVM SD_CMD	C	Main EVM & Secondary EVM SD_CMD connected for simultaneous shutdown	
		O	Main EVM & Secondary EVM SD_CMD not connected for independent shutdown	Y
J21	IMON1 & IMON2	C	Combined channel current monitors	
		O	Independent dual-channel current monitor	Y
J22	Main & Secondary EVM UVLO	C	Main EVM & Secondary EVM UVLO connected	
		O	Main EVM & Secondary EVM UVLO not connected	Y
J23	Main & Secondary EVM EN1	C	Main EVM & Secondary EVM EN1 connected	
		O	Main EVM & Secondary EVM EN1 not connected	Y
J24	EN1 & EN2	C	Combined channel enable	Y
		O	Independent dual-channel enable	
J25	USB2ANY pullup for SCL	C	Pullup by USB2ANY board	
		O	Pullup by external signal source through J17	Y
J32	OPT/ EN2_secondary	C	3- and 4-phase auto transition	
		O	3- and 4-phases auto transition inactive	Y
J33	PWM input for ISET	C	Not allowed	
		O	External PWM input for ISET	Y
J37	VSET input	C	Not allowed	
		O	Output voltage tracking input	Y
J38	Onboard bias supply output connection	C	VCC supplied by onboard VCC.	Y
		O	Onboard bias supply output disconnected from VCC.	
J39	External VCC supply input	C	Not allowed	
		O	External 10-12V input port for VCC	Y
J40	Onboard bias supply enable	C	Onboard bias supply enabled	Y
		O	Onboard bias supply inactive	
J41	Onboard bias supply input connection	C	Sepic input is energized by 48V-port	Y
		O	Sepic input is disconnected and not energized	
J42	CC Control	C	CC control allowed	
		O	CC control inactive	Y

Table 2-2. Two-Pin Header Settings (continued)

HEADER	SIGNAL	PINS	FUNCTION DESCRIPTION	DEFAULT
J43	CC Control Input	C	Not allowed	
		O	CC control input port	Y
J44	USB2ANY pullup for SDA	C	Pullup by USB2ANY board	
		O	Pullup by external signal source through J17	Y

(1) Jumper pins closed.
(2) Jumper pins open.

Table 2-3. J17 60-Pin Header Description(1)

PIN	SIGNAL	I/O	DESCRIPTION
1	V48SN	O(2)	48V-port voltage sense during operation
3	V12SN	O	12V-port voltage sense during operation
5	UVLO	I(3)	Main EVM enable (connect to the UVLO pin of the IC)
7	EN1	I	CH-1 control (connect to the EN1 pin of the IC)
9	DIR	I	Direction command
11	ISETA	I	Analog command for ISET
13	ISETD	I	Digital PWM command for ISET
15	SYNCIN	I	Input of the external clock to be synchronized to
17	SYNCOUT	O	Clock output signal
19	OPT	I	Interleave angle setting
21	EN2	I	CH-2 control (connect to the EN2 pin of the IC)
23	DEM	O	FPWM/DEM selection
25	+5V	O	Onboard 5 V bias supply
27	IMON1	O	CH-1 monitor
29	IMON2	O	CH-2 current monitor
31	IMON1_S	O	Secondary EVM CH-1 monitor in 3 or 4 phases
33	IMON2_S	O	Secondary EVM CH-2 current monitor in 3 or 4 phases
35	AGND	I/O	Reference GND for control signals
37	PGND	O	Power ground of the DC-DC converter
39	SDA	I	SDA of I^2C
41	SCL	I	SCL of I^2C
43	+10 V	I/O	+10V bias supply
45	nSD	I/O	External shut down command input pin
47	ENABLE_S	I	Secondary EVM enable (connect to the UVLO pin of the secondary IC)
49	CH1_S	I	Secondary EVM CH-1 control (connect to the EN1 pin of the secondary IC)
51	CH2_S	I	Secondary EVM CH-2 control (connect to the EN2 pin of the secondary IC)
53	SYNCIN_S	I	Input of the external clock for the secondary EVM to be synchronized to
55	SYNCOUT_S	O	Secondary EVM clock output signal
57	nSD_S	I/O	Secondary EVM external shut down command input pin
59	KEY	—	No Connect
All even number pins	AGND	I/O	All signals' return

(1) J17 is the interface connector to MCU, or external digital controller, or to J18 of the main EVM if the host EVM serves as a secondary EVM in the multiphase configuration.
(2) I = input pin
(3) O = output pin

Table 2-4. J18 60-Pin Header Description(1)

PIN	SIGNAL	I/O	DESCRIPTION
1	V48_X	—	No Connect
3	V12_X	—	No Connect
5	ENABLE_S	I(2)	Secondary EVM enable (connect to the UVLO pin of the secondary IC)
7	CH1_S	I	Secondary EVM CH-1 control (connect to the EN1 pin of the IC)
9	DIR	I	Direction command
11	ISETA	I	Analog command for ISET
13	ISETD	I	Digital PWM command for ISET
15	SYNCIN_S	I	The external clock input for the secondary
17	SYNCOUT_S	O(3)	Secondary EVM clock output signal
19	OPT	I	Interleave angle setting
21	CH2_S	I	Secondary EVM CH-2 control (connect to the EN1 pin of the IC)
23	DEM_S	I	FPWM/DEM selection
25	+5 V	I	Onboard 5 V bias supply
27	IMON1_S	O	Secondary EVM CH-1 monitor in 3 or 4 phases
29	IMON2_S	O	Secondary EVM CH-2 current monitor in 3 or 4 phases
31	IMON1_X	—	Not used
33	IMON2_X	—	Not used
35	AGND	I/O	Reference GND for control signals
37	PGND	O	Power ground of the DC-DC converter
39	SDA	I	SDA of I^2C
41	SCL	—	SCL of I^2C
43	+10 V	I	Onboard +10-V bias supply
45	nSD_S	I/O	Secondary EVM external shut down command input pin
47	UVLO_X	—	No Connect
49	CH1_X	—	No Connect
51	CH2_X	—	No Connect
53	SYNCIN_X	—	No Connect
55	SYNCOUT_X	—	No Connect
57	SD_X	—	No Connect
59	KEY	—	No Connect
All even number pins	AGND	I/O	All signals' return

(1) J18 is the interface connector to the secondary EVM in the multiphase configuration if the host EVM serves as the main. All control commands and control signals are sent through J18 to J17 of the secondary EVM.
(2) I = input pin
(3) O = output pin

2.2 Bench Setup

For buck mode or boost mode operation, one Power Supply (PS) and one Electronic Load (E-Load) are enough to perform the test as shown in Jumper Settings for Typical Operation Modes.

For bidirectional operation, Figure 2-3 shows the typical bench setup to operate the EVM in the bidirectional power system environment. The combination of the E-Load and bench PS emulates a battery capable of both sourcing and sinking current. A relatively Higher Voltage Power Supply (HV-PS) and E-Load (HV-E-Load) are needed for the 48VDC-port, and a Lower Voltage Power Supply (LV-PS) and E-Load (LV-E-Load) are needed for the 12VDC-port.

The user can externally provide the dashed line signals, or use the onboard jumpers to set these signals, when operating the EVM.

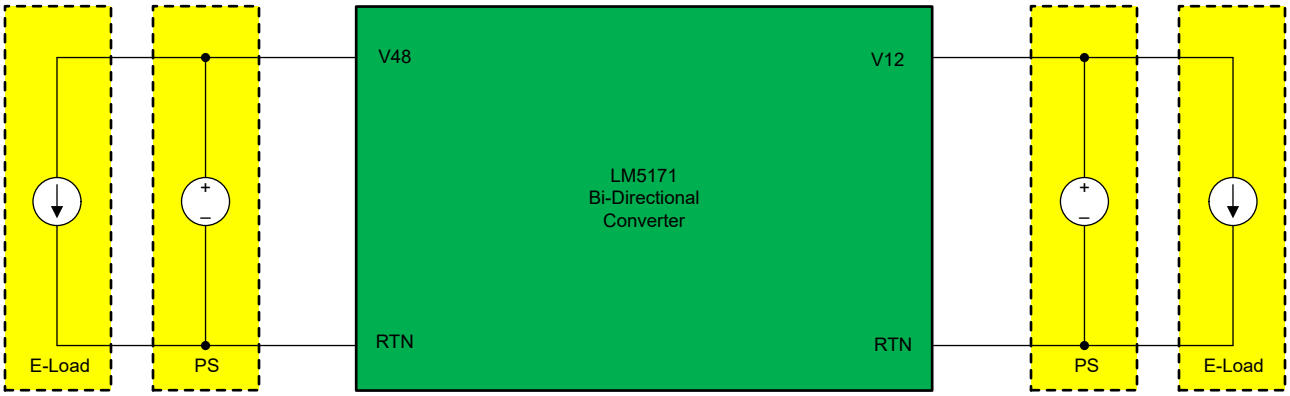

Figure 2-3. Bidirectional Converter Bench Setup

To operate the EVM to full power, follow the guidelines below for initial setup:

- Set the LV-E-Load to Constant Current (CC) of 62 A
- Set the LV-PS voltage at 12 V, and the current limit at 63 A
- Set the HV-E-Load to CC of 14 A
- Set the HV-PS voltage at 48 V, and the current limit at 15 A

2.3 Test Equipment

Power Supplies: HV-PS needs to be capable of 80 V/20 A, and LV-PS 40 V/80 A. To operate 2 EVMs in 4 phase configuration, double the capabilities of the HV-PS and LV-PS. Bench power supplies to generate UVLO, ISETA, DIR, and EN1 and EN2 signals need to be capable of 5 V/0.1A.

Electronic Loads: The HV-E-Load needs to be capable of 80 V/20 A, and LV-E-Load 40 V/80 A. To operate 2 EVMs in 4 phase configuration, double the capability of the E-Load.

Meters: Because most current meters are rated only to 10 A, shunts are recommended to measure the current using a DVM.

Oscilloscope: An oscilloscope and 10x probes with at least 20-MHz bandwidth is required. Current probe capable of 50 A is required to monitor the inductor current via a wire loop inserted to the non-switching side of the inductor.

2.4 Jumper Settings for Typical Operation Modes

Refer to the following sections for EVM jumper settings for some typical operation modes.

- Buck Mode with Voltage Regulation
- Boost Mode with Voltage Regulation
- Buck Mode with Current Regulation
- Boost Mode with Current Regulation
- 2-EVM Daisy-Chain for 3 or 4-Phase Operation

The jumper connections are shown as small red rectangular box, which indicating the short of the enclosed two pins of the jumper header.

2.4.1 Buck Mode with Voltage Regulation

Jumper Settings in Buck Mode with Voltage Regulation shows the jumper settings of buck mode with voltage regulation. This is the default jumper setting of the EVM.

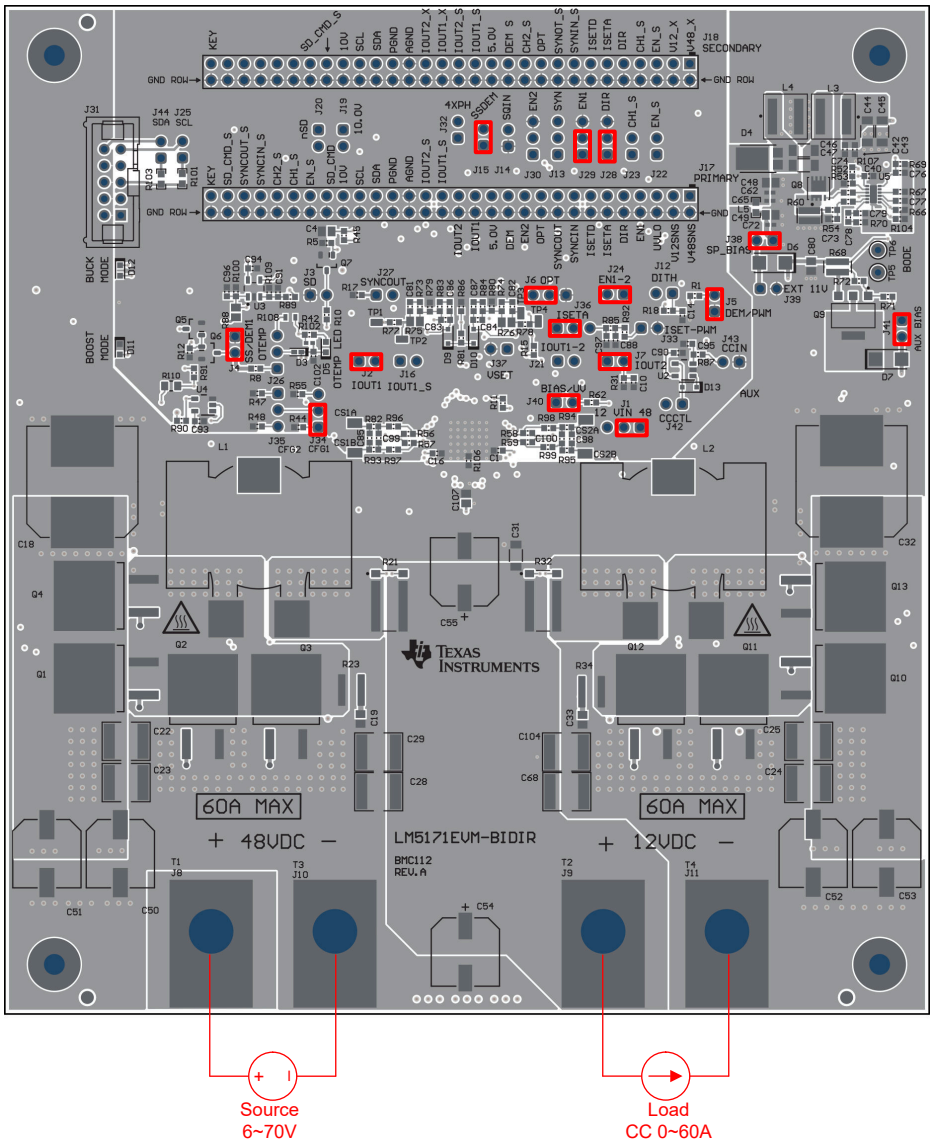

Figure 2-4. Jumper Settings in Buck Mode with Voltage Regulation

The status of the EVM is as follows:

- UVLO: 48 V via J1
- Phase interleaving angle: 180° via J6
- DIR: Buck mode via J28
- EN1: Enable via J29
- CFG: I^2C address set to 0x0 & inductor current monitor via J34
- Voltage loop: Closed via J36
- IMON1: Filter connected via J2
- IMON2: Filter connected via J7
- SS/DEM1: DEM mode via J4
- SS/DEM1: DEM mode via J5
- SS/DEM2 connected to SS/DEM1 via J15
- EN2: Select EN2=EN1 via J24
- VCC supply: Select onboard bias power via J38
- Onboard bias power: Enabled via J40
- Onboard bias power input: 48 V via J41

Note the load needs to be set to CC mode.

2.4.2 Boost Mode with Voltage Regulation

Jumper Settings in Boost Mode with Voltage Regulation shows the jumper settings of boost mode with voltage regulation.

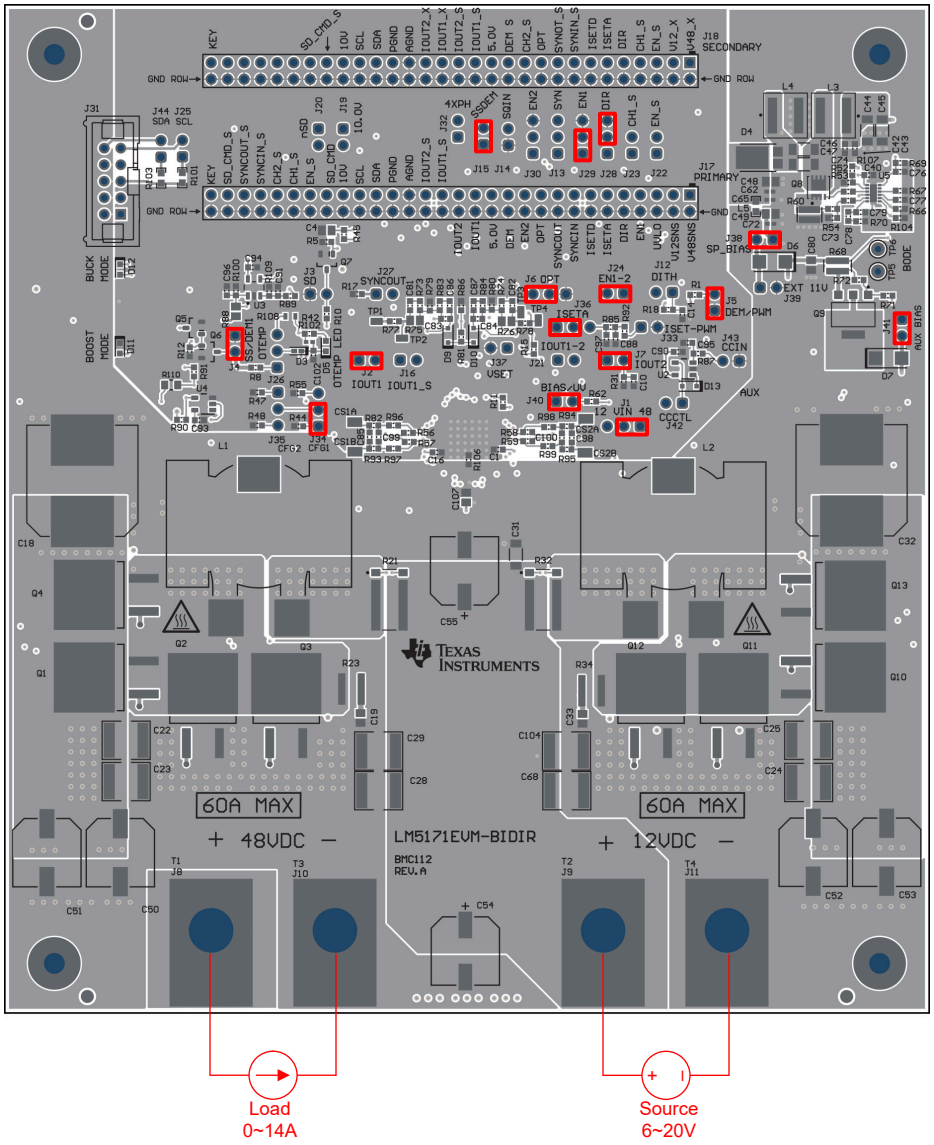

Figure 2-5. Jumper Settings in Boost Mode with Voltage Regulation

Compared to Buck Mode with Voltage Regulation, J28-pin 2,3 is closed for boost mode. Also note the source and load are exchanged from that of buck mode.

2.4.3 Buck Mode with Current Regulation

Figure 2-6 shows the jumper settings of buck mode with current regulation.

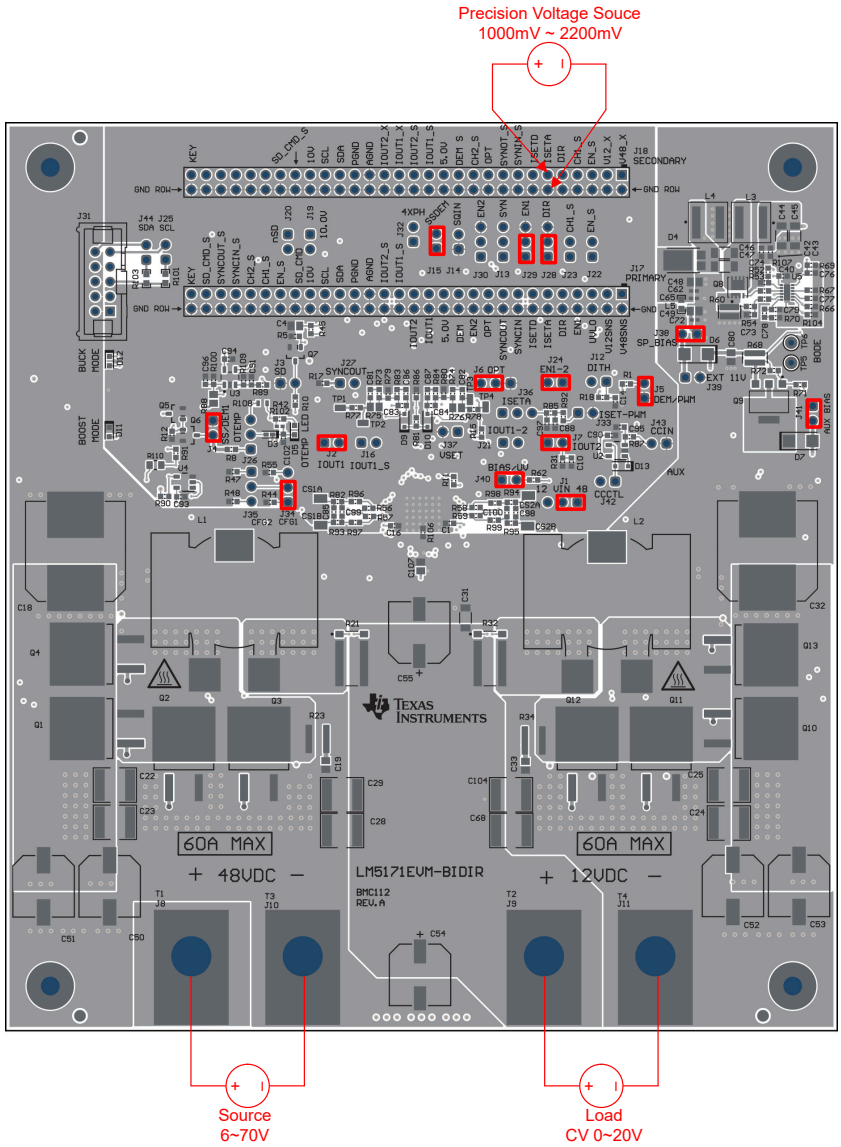

Figure 2-6. Jumper Settings in Buck Mode with Current Regulation

Compared to Buck Mode with Voltage Regulation, J36 is open and ISET is set from external precision voltage source . Also note the load needs to be set to CV mode.

2.4.4 Boost Mode with Current Regulation

Figure 2-7 shows the jumper settings of boost mode with current regulation.

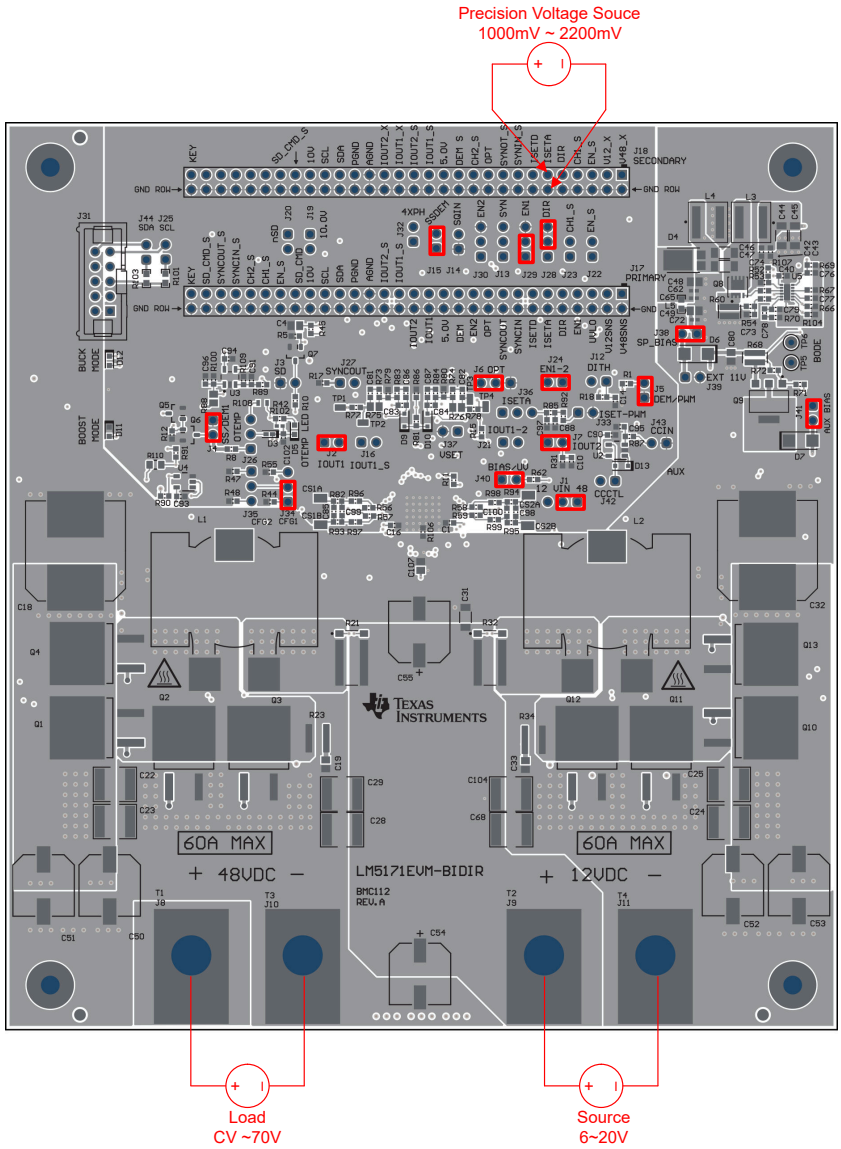

Figure 2-7. Jumper Settings in Boost Mode with Current Regulation

Compared to Buck Mode with Current Regulation, J28-pin 2,3 is closed for boost mode. Also note the source and load are exchanged from that of buck mode.

2.4.5 2-EVM Daisy-Chain for 3 or 4-Phase Operation

Figure 2-8 shows the jumper settings for 2-EVM Daisy-Chain.

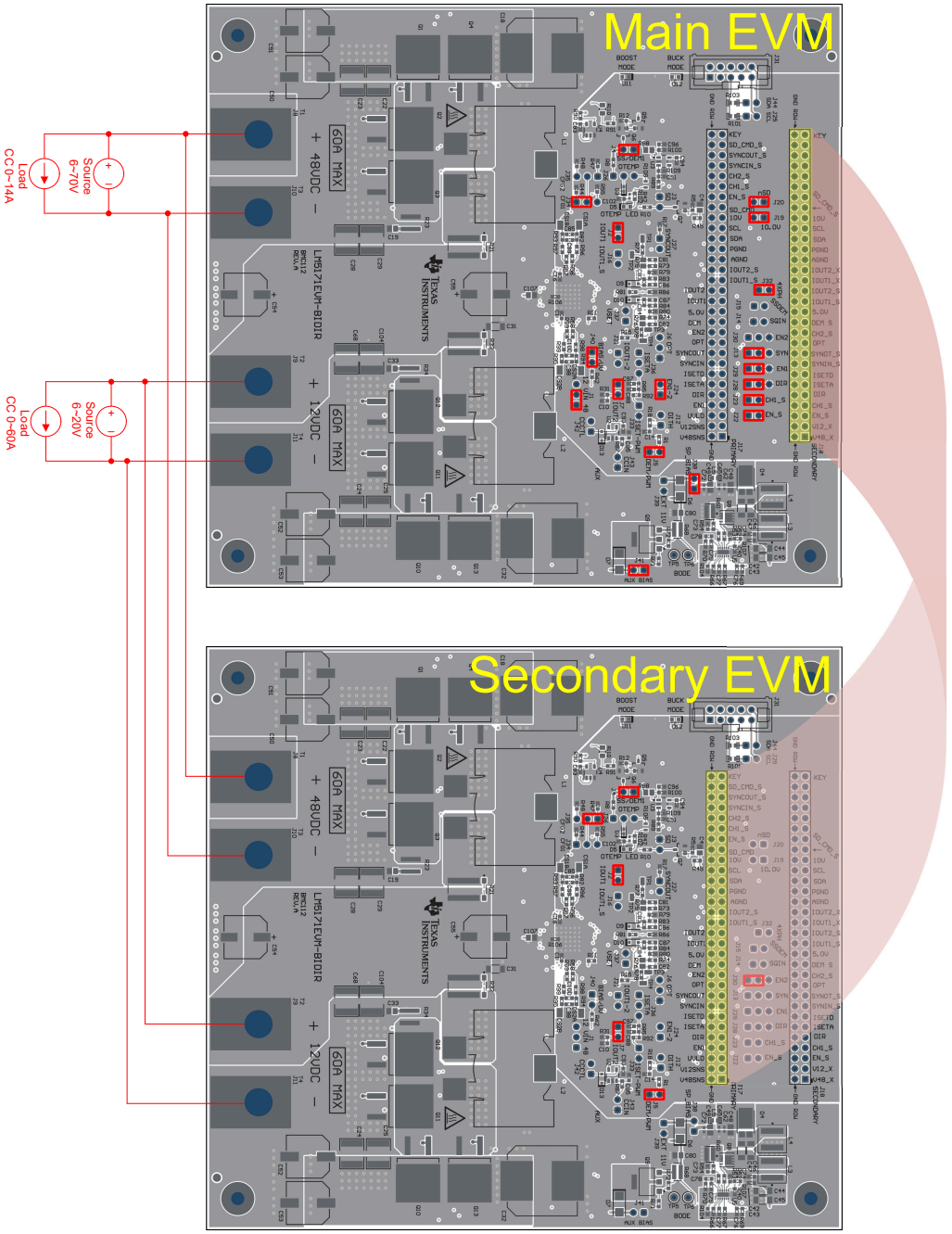

Figure 2-8. Jumper Settings in 2-EVM Daisy-Chain for 3 or 4-Phase Operation

Jumper Settings in 2-EVM Daisy-Chain for 3 or 4-Phase Operation described four-phase operating with 90° interleaving. By connecting secondary EVM J30 pin 2,3 instead of pin 1,2, three-phase operating is obtained.

J6 is open and J32 is closed in main EVM, thus interleaving angle changes automatically between 3 phase and 4 phase.

Note for bidirectional operation, the source and load needs to be set referring to Bench Setup.

3 Test Procedure

Please read the LM5171 data sheet (SNVSCM3) and this user guide before using the EVM. A typical EVM test bench setup is shown in Figure 2-2. The power supplies and loads need to be capable of handling the input and output voltage and current rating of the board.

By default, onboard 10-V bias supply is used. External 10-V bias supply can also be applied following the jumper settings described in Table 2-2

Four external control signals can be used to operate the EVM, which are UVLO, DIR, EN1/2, and ISETA or ISETD (refer to Figure 2-3).

- UVLO: The main enable command. Apply a voltage > 2.5 V and < 6 V between J17-pins 5 and 6 to enable the EVM. Pulling the voltage at J17-pin 5 low keeps the EVM in shutdown mode.
- DIR: the current direction command. Apply a voltage > 2 V at J17-pin 9 or J18-pin 9 to operate the EVM in Buck Mode. Apply a voltage < 1 V at the same pin to operate the EVM in Boost Mode. DIR command can also be programmed using J28. Note that DIR must be either active high or low to operate the EVM. If the DIR signal is floating, the EVM can not run.
- EN1/2: The channel switching enable commands. Apply a voltage > 2 V at J17-pin 7 turns on CH-1 converter, and at J17-pin 21 can turn on CH-2 converter. Removing the voltage at the EN1 and EN2 pins to disable each channel. The channel enable can also be controlled by J29, J30 and J24.
- ISETA or ISETD: The channel current regulation setting. Applying an analog voltage across J17-pins 11 and 12, or J18-pins 11 and 12, or a PWM signal across J17-pins 13 and 14, or J18-pins 13 and 14, to the EVM regulates the channel DC current, which is also the power inductor dc current, to a level proportional the ISETA voltage or ISETD PWM duty ratio. ISETA is set by the onboard outer voltage loop when closed. Note that, ISETA has 1 V offset, and ISETA=2.2 V commands the EVM to produce 60 A into or out of the 12VDC-port, depending on the operation mode.

3.1 Buck Mode Power-Up and Power-Down Sequence

For Buck Mode with Voltage Regulation,

1. Refer to Buck Mode with Voltage Regulation for proper jumper settings.
2. Set LV-E-Load to CC mode. Turn on the HV-PS power supply and LV-E-Load.
3. Perform the test.
4. After the tests are done, turn off the HV-PS and LV-E-Load.

For Buck Mode with Current Regulation,

1. Refer to Buck Mode with Current Regulation for proper jumper settings.
2. Set LV-E-Load to CV mode. Turn on the HV-PS power supply and LV-E-Load.
3. Apply an analog voltage gradually rising from 1 V to 2.2 V at J17-pin 11 or J18-pin 11 (ISETA), or a PWM signal at J17-pin 13 or J18-pin 13.
4. Perform the test.
5. After the tests are done, set ISETA to 1 V, and turn off the HV-PS and LV-E-Load.

3.2 Boost Mode Power-Up and Power-Down Sequence

For Boost Mode with Voltage Regulation,

1. Refer to Boost Mode with Voltage Regulation for proper jumper settings.
2. Set HV-E-Load to CC mode. Turn on the LV-PS power supply and HV-E-Load.
3. Perform the test.
4. After the tests are done, and turn off the LV-PS and HV-E-Load.

For Boost Mode with Current Regulation,

1. Refer to Buck Mode with Current Regulation for proper jumper settings.
2. Set HV-E-Load to CV mode. Turn on the LV-PS power supply and HV-E-Load.
3. Apply an analog voltage gradually rising from 1 V to 2.2 V at J17-pin 11 or J18-pin 11 (ISETA), or a PWM signal at J17-pin 13 or J18-pin 13.
4. Perform the test.
5. After the tests are done, set ISETA to 1 V, and turn off the LV-PS and HV-E-Load.

3.3 Bidirectional Operation Power-Up and Power-Down Sequence

1. Refer to Table 2-1 through Table 2-4 for proper jumper settings.
2. Turn on the HV-PS power supply and HV-E-load.
3. Turn on the HV-PS power supply and HV-E-load.
4. Apply a voltage > 2.5 V and < 6 V at J17-pin 5 (main enable).
5. Apply the direction command (DIR) at J17-pin 9 or J18-pin 9.
6. Apply an analog voltage gradually rising from 1 V to 2.2 V at J17-pin 11 or J18-pin 11 (ISETA), or a PWM signal at J17-pin 13 or J18-pin 13.
7. Dynamically flip the DIR signal state between 0 (DIR < 1 V) and 1 (DIR > 2 V), the EVM operates in dynamic bidirectional transition mode. In FPWM mode, the user can change direction by setting ISETA below 1 V.
8. Perform the test.
9. After the tests are done, set ISETA to 1 V, remove the voltage at J17-pin 5, and turn off the E-Load, HV-PS and LV-PS.

3.4 Operating the EVM With External MCU or Other Digital Circuit

1. Onboard analog voltage loop control circuit must be disconnected.
2. Use J17 header to interface the external MCU or other control circuit.
3. Follow the power-up and power-down sequence for buck mode or boost mode operation.

Signals required from an MCU or other digital control circuit include UVLO, EN1/EN2, DIR, ISETA or ISETD. Contact TI for info on operating the EVM with the MSPM0 Launchpad or C2000 MCU.

4 Test Data

4.1 Efficiency

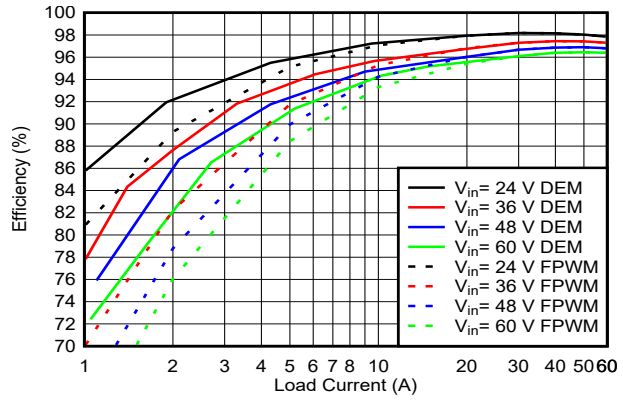

Figure 4-1. Buck Mode Efficiency vs Input Voltage and Load Current: V_{OUT} = 14.5 V

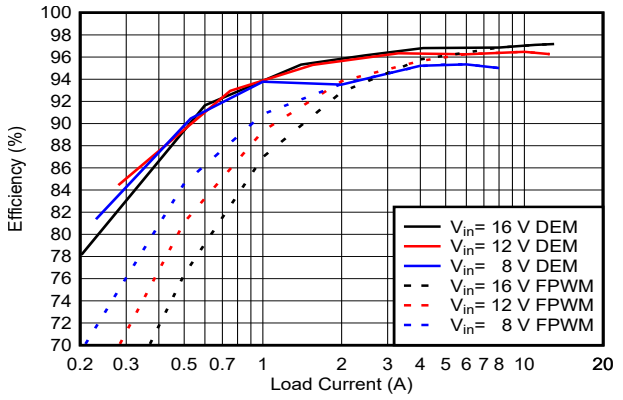

Figure 4-2. Boost Mode Efficiency vs Input Voltage and Load Current: V_{OUT} = 50.5 V

4.2 Step Load Response

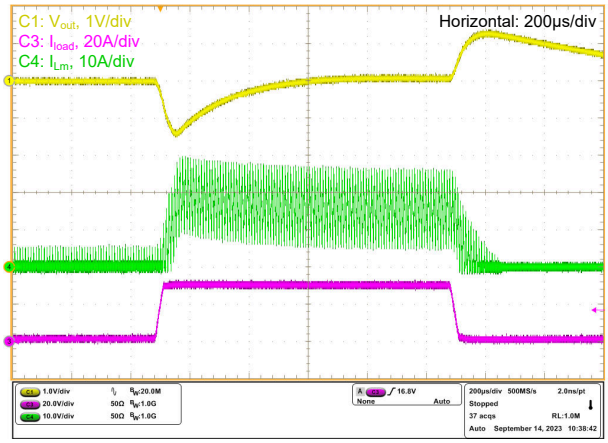

Figure 4-3. Step Load Response: Buck Mode; DEM; 1 A to 30 A Load Step; 1 A/µs

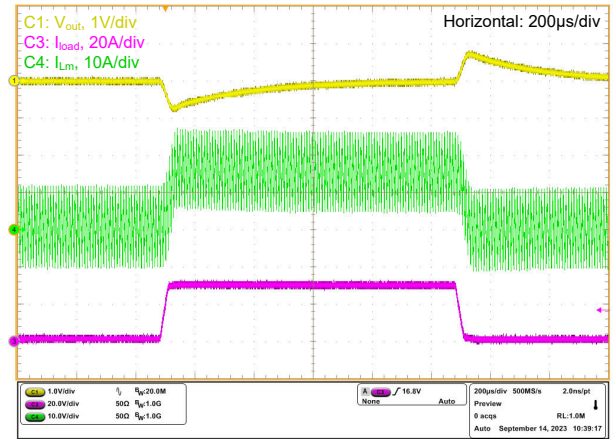

Figure 4-4. Step Load Response: Buck Mode; FPWM; 1 A to 30 A Load Step; 1 A/µs

4.3 Dual-Channel Interleaving Operation

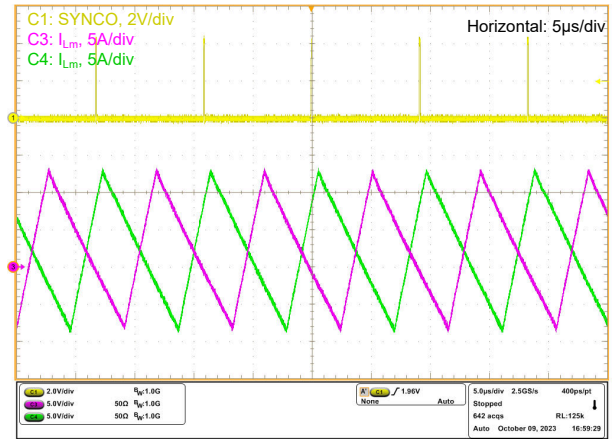

Figure 4-5. Dual-Channel Interleaving Operation: Buck Mode, I_{load}= 4 A

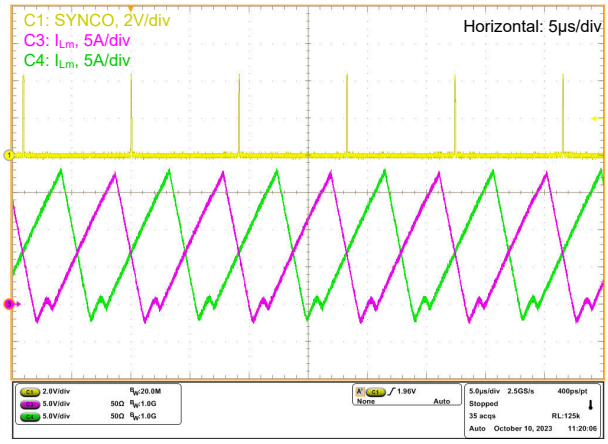

Figure 4-6. Dual-Channel Interleaving Operation: Boost Mode, I_{load}= 4 A

4.4 Typical Start Up and Shutdown

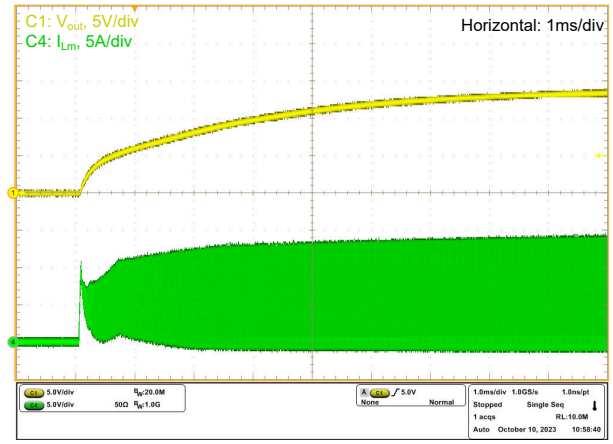

Figure 4-7. Start Up: Buck Mode, I_{load}= 10 A

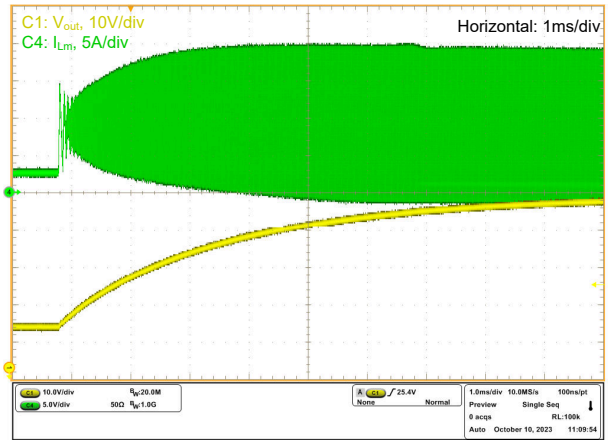

Figure 4-8. Start Up: Boost Mode, I_{load}= 4 A

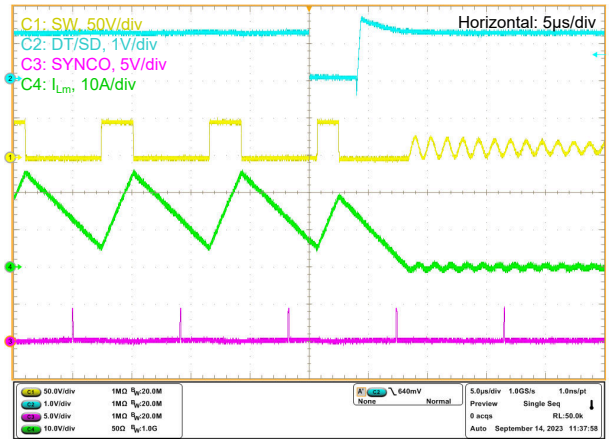

Figure 4-9. Shutdown: Latched Shutdown by DT/SD

4.5 DEM and FPWM

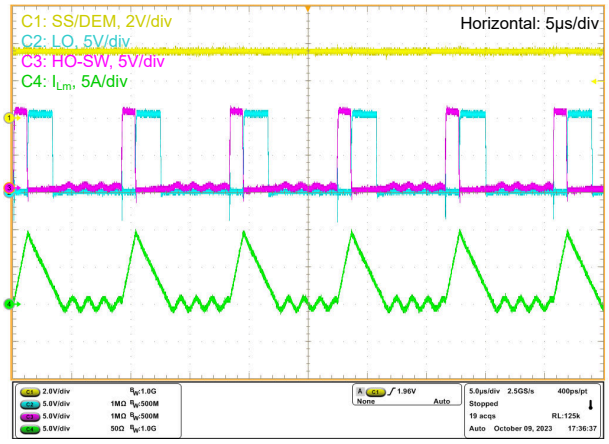

Figure 4-10. DEM: Buck Mode, I_{load}= 4 A

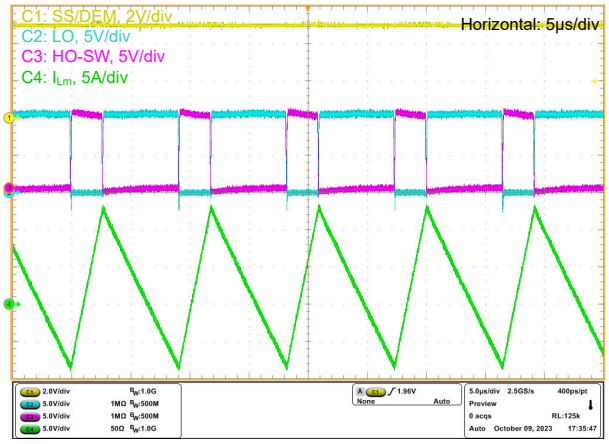

Figure 4-11. FPWM: Buck Mode, I_{load}= 4 A

4.6 Mode transition between DEM and FPWM

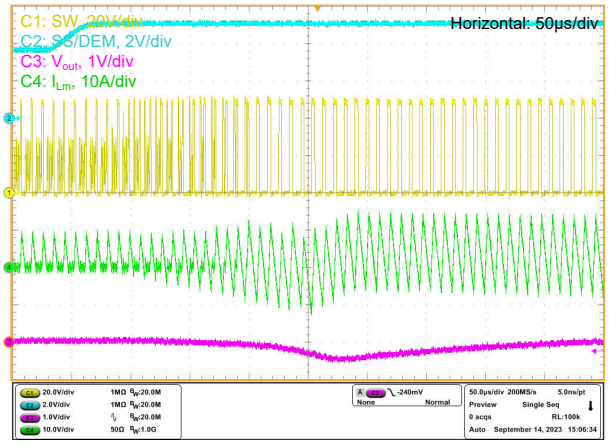

Figure 4-12. Mode Transition from DEM to FPWM: Buck Mode, I_{load}=4A

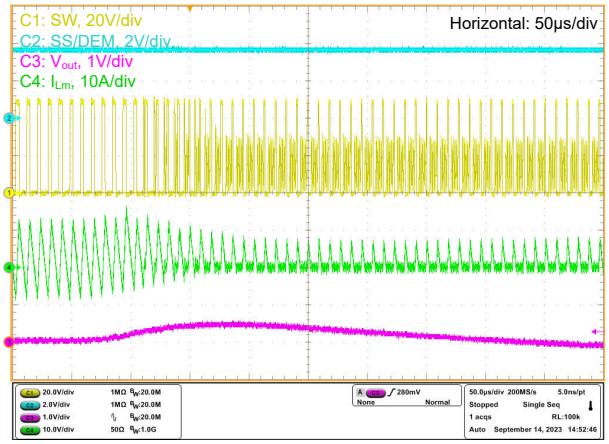

Figure 4-13. Mode Transition from FPWM to DEM: Buck Mode, I_{load}=4A

4.7 ISET Tracking

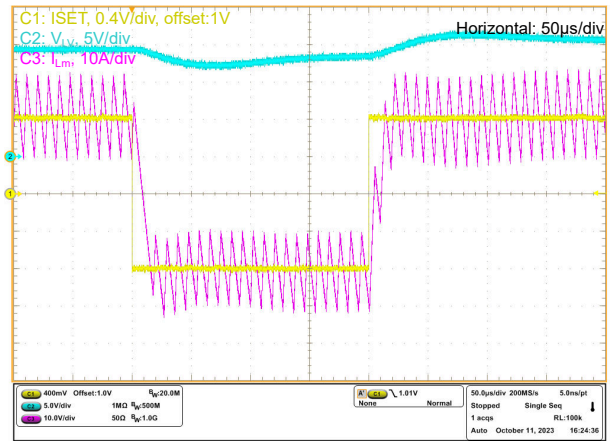

Figure 4-14. ISET Tracking: Inductor Current Tracking with Direction Change

4.8 Pre-charge

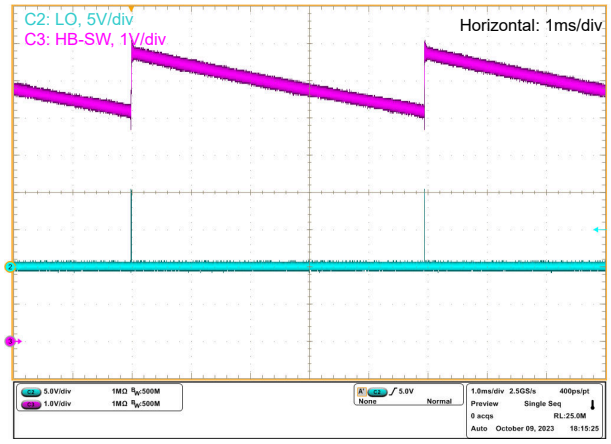

Figure 4-15. Pre-charge: Buck Mode, I_{load}= 0 A

4.9 Protections

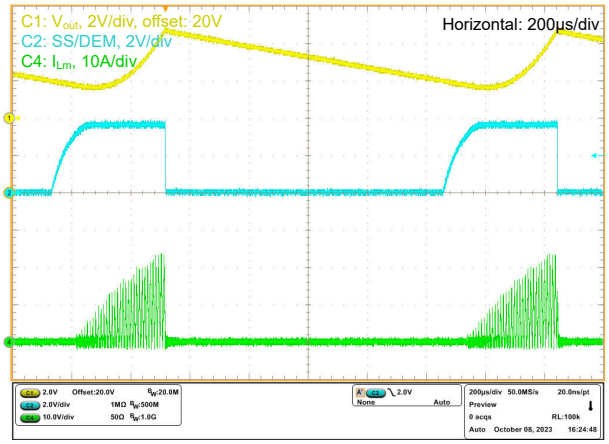

Figure 4-16. OVP: Buck Mode

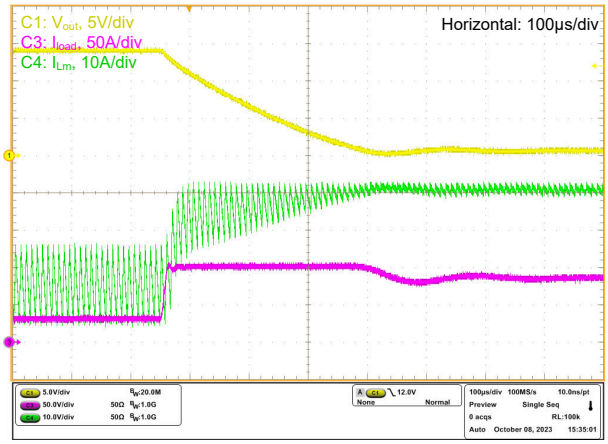

Figure 4-17. Output Short Circuit: Buck Mode

5 Design Files

5.1 Schematics

To download the Schematics for the EVM board, see the design files at www.ti.com/tool.

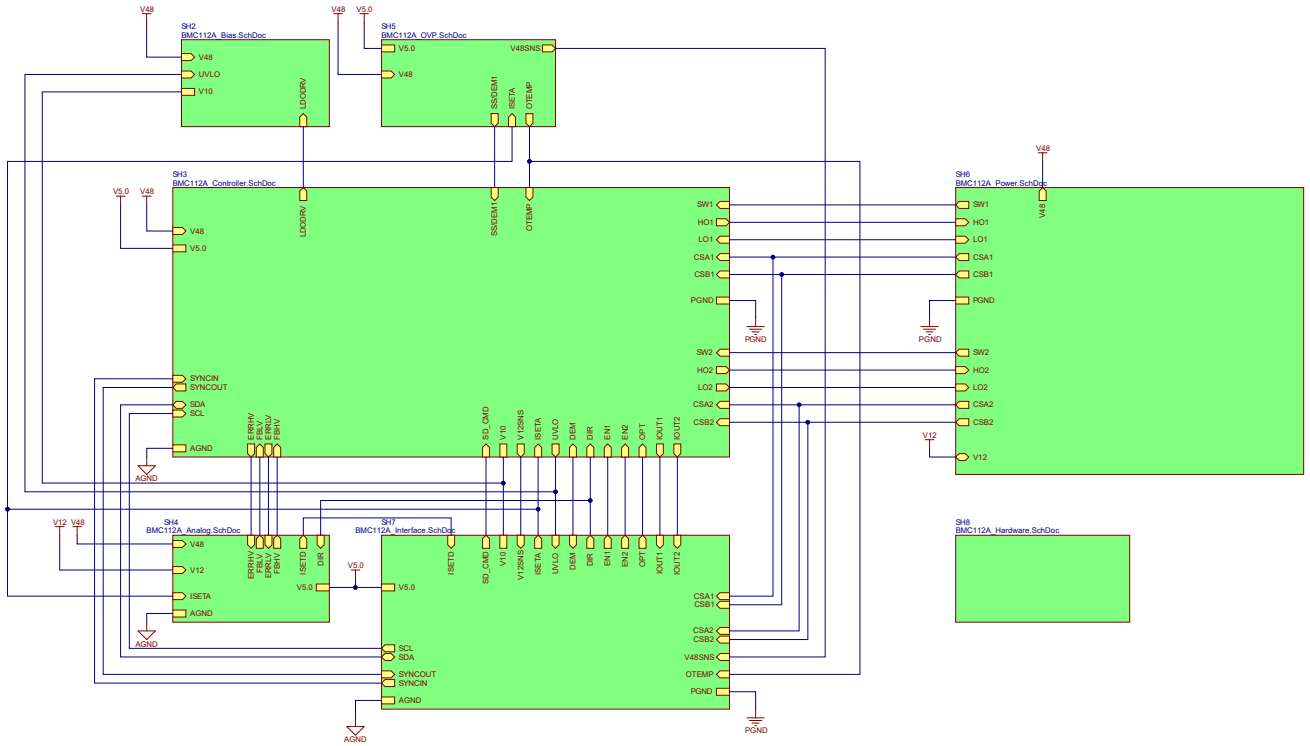

Figure 5-1. EVM Schematic Part 1: Over view

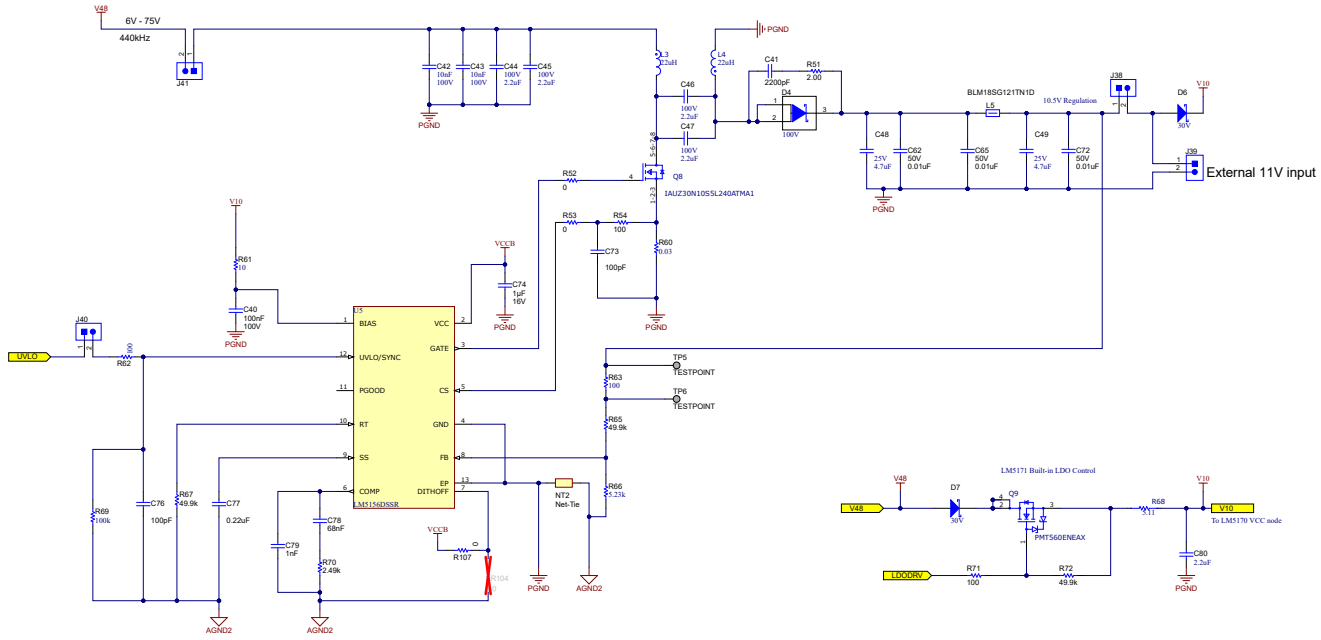

Figure 5-2. EVM Schematic Part 2: Bias Supplies

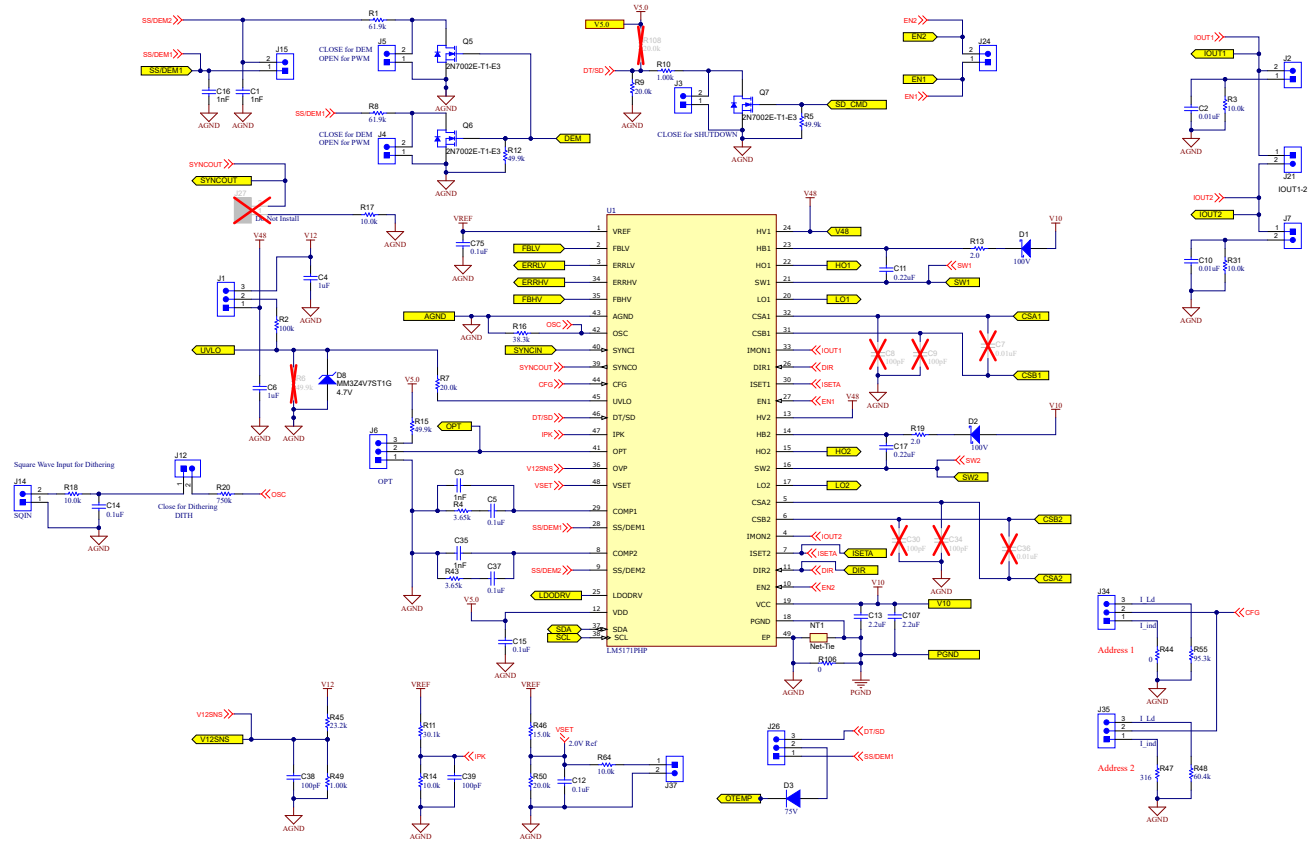

Figure 5-3. EVM Schematic Part 3: Controller

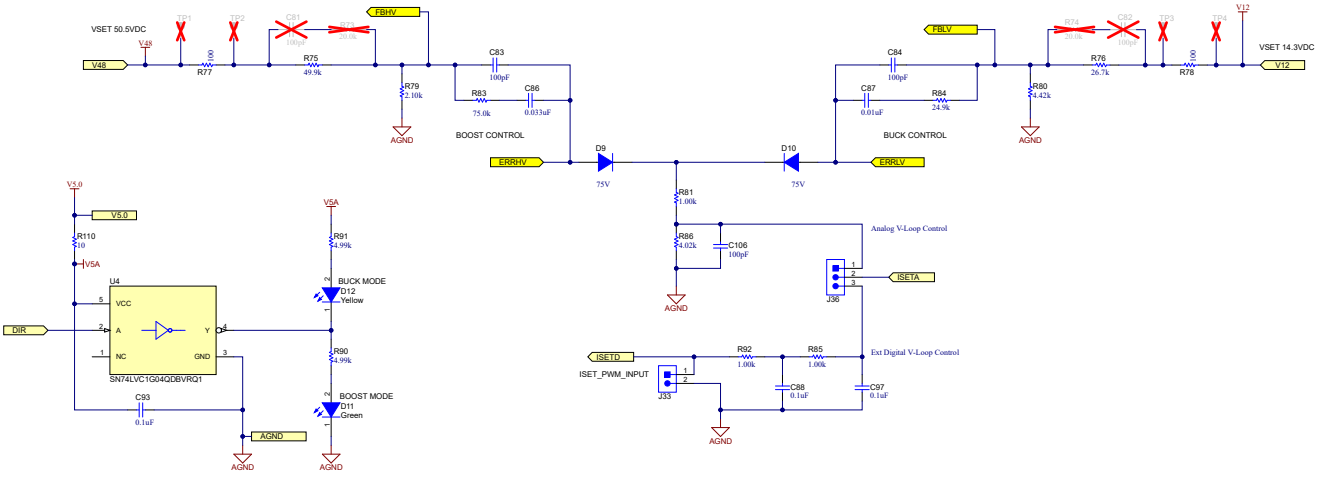

Figure 5-4. EVM Schematic Part 4: Outer Voltage Loop

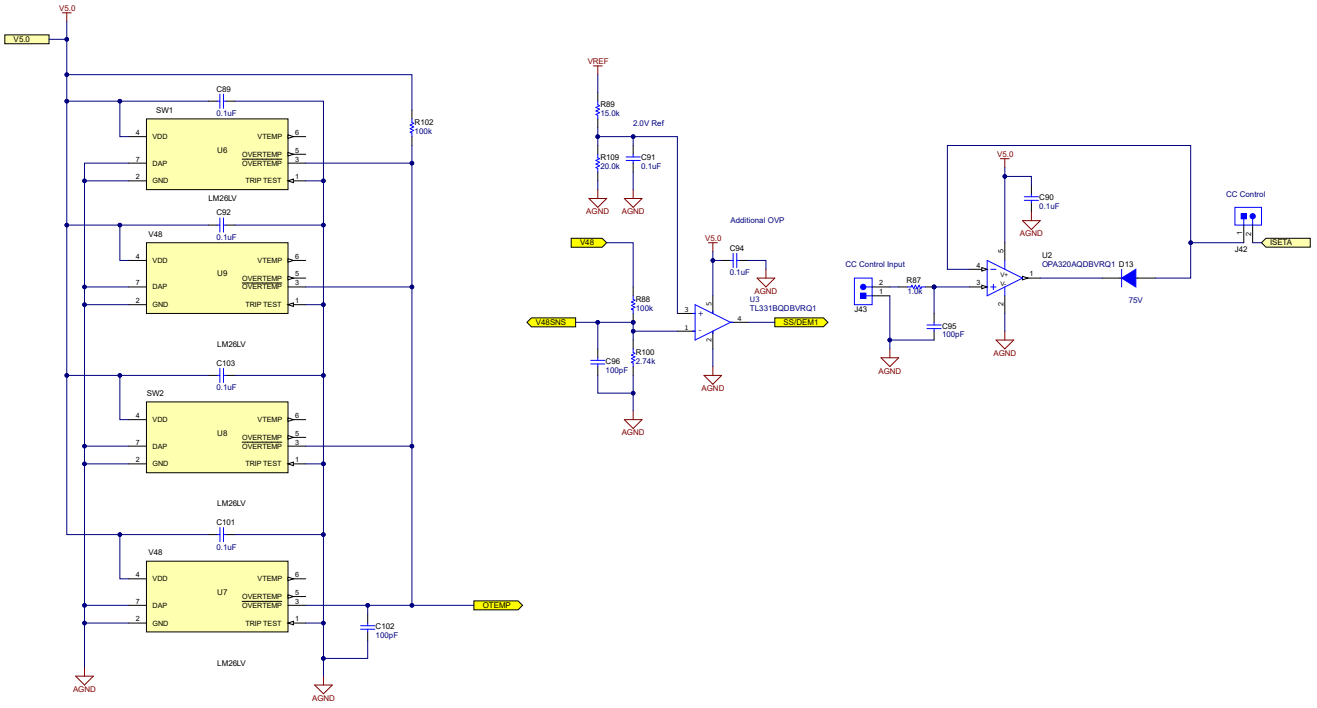

Figure 5-5. EVM Schematic Part 5: Protection

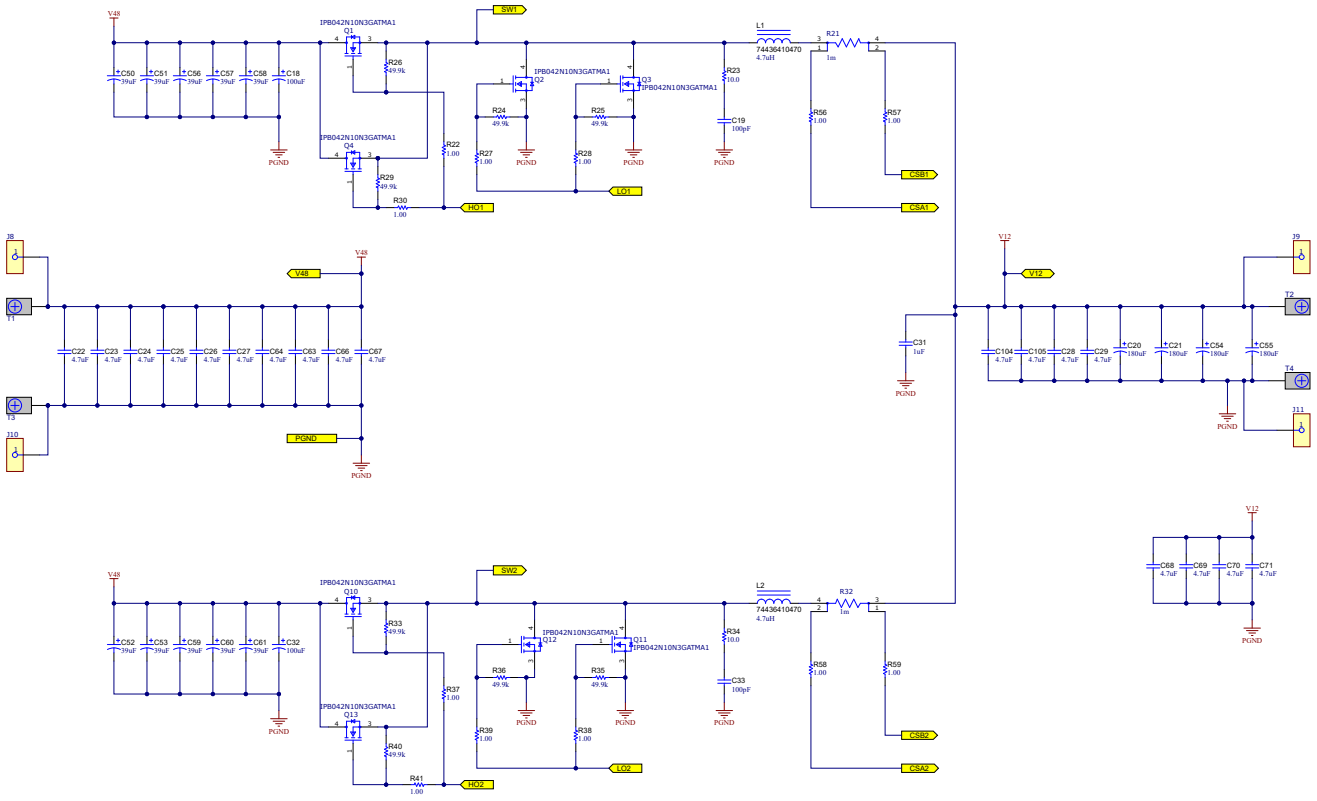

Figure 5-6. EVM Schematic Part 6: Power stage

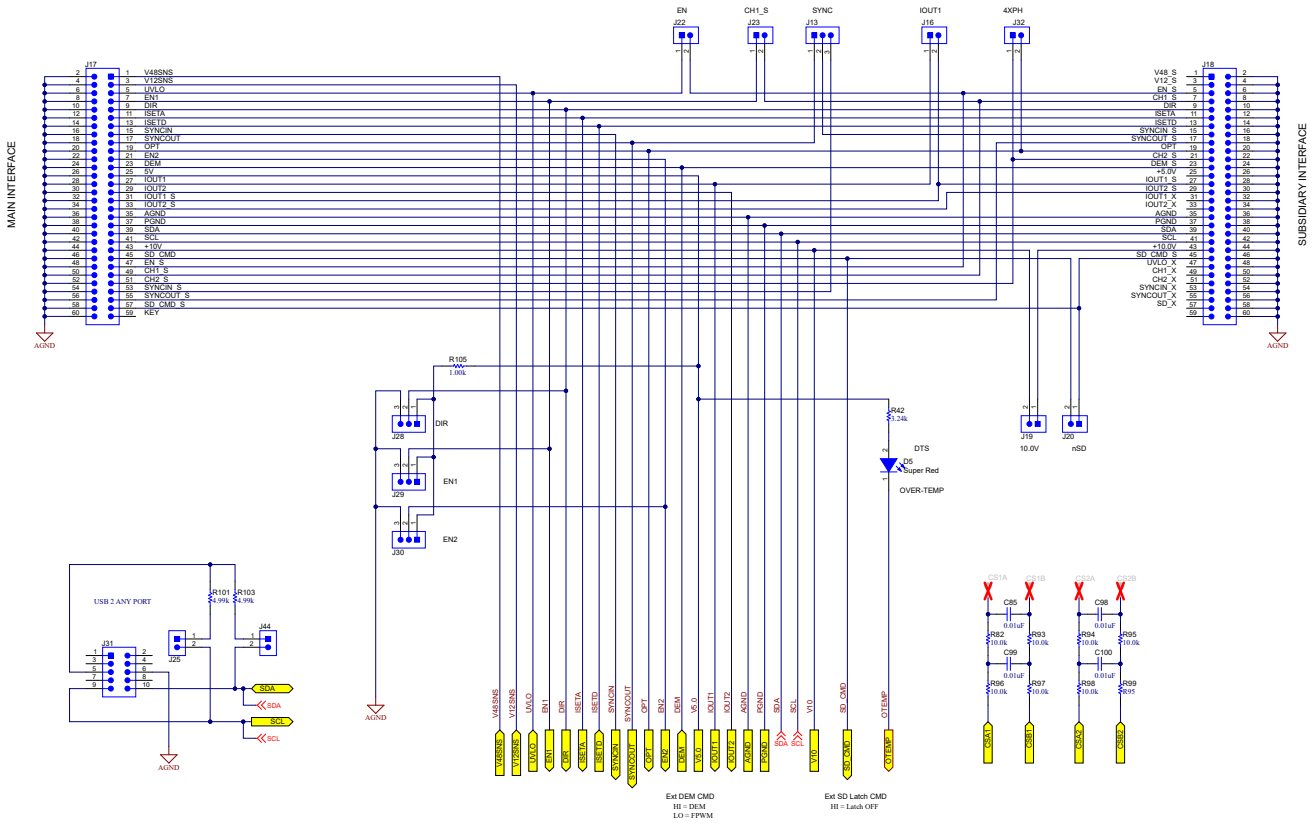

Figure 5-7. EVM Schematic Part 7: Interface Connectors and Configuration Headers

5.2 Bill of Materials

Table 5-1. Bill of Materials

COUNT	DESIGNATOR	DESCRIPTION	PART NUMBER	MANUFACTURER
5	C1, C3, C16, C35, C79	CAP, CERM, 1000 pF, 50 V, +/- 5%, X7R, AEC-Q200 Grade 1, 0603	C0603C102J5RACAUTO	Kemet
7	C2, C10, C85, C87, C98, C99, C100	CAP, CERM, 0.01 uF, 100 V, +/- 10%, X7R, 0603	06031C103KAT2A	AVX
2	C4, C6	CAP, CERM, 1 uF, 100 V, +/- 10%, X7S, 0805	C2012X7S2A105K125AB	TDK
16	C5, C12, C14, C15, C37, C75, C88, C89, C90, C91, C92, C93, C94, C97, C101, C103	CAP, CERM, 0.1 uF, 100 V, +/- 10%, X7R, 0603	GRM188R72A104KA35D	MuRata
2	C11, C17	CAP, CERM, 0.22 uF, 50 V, +/- 10%, X7R, 0603	C1608X7R1H224K080AB	TDK
3	C13, C80, C107	CAP, CERM, 2.2 uF, 16 V, +/- 10%, X7R, 0805	C2012X7R1C225K125AB	TDK
2	C18, C32	CAP, AL, 100 uF, 100 V, +/- 20%, 0.24 ohm, SMD	EMVH101GDA101MLH0S	Chemi-Con
2	C19, C33	CAP, CERM, 100 pF, 100 V, +/- 10%, C0G/NP0, 0805	08051A101KAT2A	AVX
4	C20, C21, C54, C55	CAP, Aluminum Polymer, 180 uF, 50 V, +/- 20%, 0.019 ohm, SMD, 2-Leads, Dia 10.5mm, Pin Spacing 8 mm SMD	PCR1H181MCL1GS	Nichicon
18	C22, C23, C24, C25, C26, C27, C28, C29, C63, C64, C66, C67, C68, C69, C70, C71, C104, C105	CAP, CERM, 4.7 uF, 100 V, +/- 20%, X7R, 2220	C5750X7R2A475M230KA	TDK
1	C31	CAP, CERM, 1 uF, 100 V, +/- 10%, X7R, 1206	GRM31CR72A105KA01L	MuRata
8	C38, C39, C83, C84, C95, C96, C102, C106	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	C0603C101J5GACTU	Kemet
1	C40	CAP, CERM, 0.1 uF, 100 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	GCJ188R72A104KA01D	MuRata
1	C41	CAP, CERM, 2200 pF, 100 V, +/- 10%, X7R, 0603	GRM188R72A222KA01D	MuRata
2	C42, C43	CAP, CERM, 0.01 uF, 100 V, +/- 10%, X7R, 0603	GRM188R72A103KA01D	MuRata
4	C44, C45, C46, C47	CAP, CERM, 2.2 uF, 100 V, +/- 10%, X7S, 1206	C3216X7S2A225K160AB	TDK
2	C48, C49	CAP, CERM, 4.7 uF, 25 V, +/- 10%, X5R, 0805	C0805C475K3PACTU	Kemet
10	C50, C51, C52, C53, C56, C57, C58, C59, C60, C61	CAP, Aluminum Polymer, 39 uF, 80 V, +/- 20%, 0.035 ohm, AEC-Q200 Grade 1, D10xL10mm SMD	HHXA800ARA390MJA0G	Chemi-Con
3	C62, C65, C72	CAP, CERM, 0.01 uF, 50 V, +/- 10%, X7R, 0402	GRM155R71H103KA88D	MuRata
2	C73, C76	CAP, CERM, 100 pF, 50 V,+/- 1%, C0G/NP0, 0603	C0603C101F5GACTU	Kemet
1	C74	CAP, CERM, 1 µF, 16 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	CGA3E1X7R1C105K080AC	TDK
1	C77	CAP, CERM, 0.22 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	CGA3E3X7R1H224K080AB	TDK
1	C78	CAP, CERM, 0.068 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	CGA3E2X7R1H683K080AA	TDK
1	C86	CAP, CERM, 0.033 uF, 100 V, +/- 10%, X7S, AEC-Q200 Grade 1, 0603	CGA3E3X7S2A333K080AB	TDK
2	D1, D2	Diode, Schottky, 100 V, 1 A, AEC-Q101, SOD-123W	PMEG10010ELRX	Nexperia
1	D3	Diode, Switching, 75 V, 0.3 A, SOD-523	1N4148X-TP	Micro Commercial Components

Table 5-1. Bill of Materials (continued)

COUNT	DESIGNATOR	DESCRIPTION	PART NUMBER	MANUFACTURER
1	D4	Diode, Schottky, 100 V, 5 A, AEC-Q101, PowerDI5	PDS5100HQ-13	Diodes Inc.
1	D5	LED, Super Red, SMD	150060SS75000	Wurth Elektronik
2	D6, D7	Diode, Schottky, 30 V, 2 A, SMA	B230A-13-F	Diodes Inc.
1	D8	Diode, Zener, 4.7 V, 300 mW, SOD-323	MM3Z4V7ST1G	ON Semiconductor
3	D9, D10, D13	Diode, Switching, 75 V, 0.25 A, SOD-323	1N4448WX-TP	Micro Commercial Components
1	D11	LED, Green, SMD	150060VS75000	Wurth Elektronik
1	D12	LED, Yellow, SMD	150060YS75000	Wurth Elektronik
6	FID1, FID2, FID3, FID4, FID5, FID6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
4	H1, H2, H3, H4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH	B&F Fastener Supply
4	H5, H6, H7, H8	Standoff, Hex, 0.5"L #4-40 Nylon	1902C	Keystone
10	J1, J6, J13, J26, J28, J29, J30, J34, J35, J36	Header, 2.54 mm, 3x1, Gold, TH	61300311121	Wurth Elektronik
26	J2, J3, J4, J5, J7, J12, J14, J15, J16, J19, J20, J21, J22, J23, J24, J25, J32, J33, J37, J38, J39, J40, J41, J42, J43, J44	Header, 2.54 mm, 2x1, Gold, TH	61300211121	Wurth Elektronik
4	J8, J9, J10, J11	Banana Jack Connector Standard Banana Solder Lug	6095	Keystone Electronics
2	J17, J18	Header, 100mil, 30x2, Gold, TH	HMTSW-130-07-G-D-240	Samtec
1	J31	Header (shrouded), 100mil, 5x2, High-Temperature, Gold, TH	N2510-6002-RB	3M
2	L1, L2	Inductor, Shielded, Ferrite, 4.7 uH, 32 A, 0.0015 ohm, SMD	74436410470	Wurth Elektronik
2	L3, L4	22 µH Shielded Inductor 5.8 A 46.9mOhm Max Nonstandard	XGL6060-223MEC	Coilcraft
1	L5	Ferrite Bead, 120 ohm @ 100 MHz, 3 A, 0603	BLM18SG121TN1D	MuRata
8	Q1, Q2, Q3, Q4, Q10, Q11, Q12, Q13	N-Channel 100 V 100 A (Tc) 214W (Tc) Surface Mount D²PAK (TO-263AB)	IPB042N10N3GATMA1	Infineon
3	Q5, Q6, Q7	MOSFET, N-CH, 60 V, 0.24 A, SOT-23	2N7002E-T1-E3	Vishay-Siliconix
1	Q8	N-Channel 100 V 30 A (Tc) 45.5W (Tc) Surface Mount PG-TSDSON-8-32	IAUZ30N10S5L240ATMA1	Infineon
1	Q9	Small Signal low RDSon automotive Trans MOSFET N-CH 100 V 1.1A 3-Pin SC-73 T/R	PMT560ENEAX	Nexperia
2	R1, R8	RES, 61.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060361K9FKEA	Vishay-Dale
2	R2, R88	RES, 100 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	CRCW0805100KFKEA	Vishay-Dale
14	R3, R14, R17, R18, R31, R64, R82, R93, R94, R95, R96, R97, R98, R99	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310K0FKEA	Vishay-Dale
2	R4, R43	RES, 3.65 k, 1%, 0.1 W, 0603	RC0603FR-073K65L	Yageo
3	R5, R12, R15	RES, 49.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060349K9FKEA	Vishay-Dale
4	R7, R9, R50, R109	RES, 20.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060320K0FKEA	Vishay-Dale
5	R10, R49, R81, R85, R92	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K00FKEA	Vishay-Dale
1	R11	RES, 30.1 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060330K1FKEA	Vishay-Dale

Table 5-1. Bill of Materials (continued)

COUNT	DESIGNATOR	DESCRIPTION	PART NUMBER	MANUFACTURER
2	R13, R19	RES, 2.0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	CRCW08052R00JNEA	Vishay-Dale
1	R16	RES, 38.3 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060338K3FKEA	Vishay-Dale
1	R20	RES, 750 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603750KFKEA	Vishay-Dale
2	R21, R32	1 mOhms ±2% 4W Chip Resistor Wide 3518 (9045 Metric), 1835 Current Sense, Moisture Resistant Metal Foil	FC4L90R001GER	Ohmite
8	R22, R27, R28, R30, R37, R38, R39, R41	RES, 1.00, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	CRCW08051R00FKEA	Vishay-Dale
2	R23, R34	RES, 10.0, 1%, 1 W, AEC-Q200 Grade 0, 1218	CRCW121810R0FKEK	Vishay-Dale
9	R24, R25, R26, R29, R33, R35, R36, R40, R75	RES, 49.9 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	CRCW080549K9FKEA	Vishay-Dale
1	R42	RES, 3.24 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06033K24FKEA	Vishay-Dale
2	R44, R106	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3GEY0R00V	Panasonic
1	R45	RES, 23.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060323K2FKEA	Vishay-Dale
2	R46, R89	RES, 15.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060315K0FKEA	Vishay-Dale
1	R47	RES, 316, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603316RFKEA	Vishay-Dale
1	R48	RES, 60.4 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060360K4FKEA	Vishay-Dale
1	R51	RES, 2.00, 1%, 0.5 W, AEC-Q200 Grade 0, 1210	ERJ-14BQF2R0U	Panasonic
3	R52, R53, R107	RES, 0, 5%, 0.1 W, 0603	RC0603JR-070RL	Yageo
2	R54, R71	RES, 100, 1%, 0.1 W, 0603	RC0603FR-07100RL	Yageo
1	R55	RES, 95.3 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060395K3FKEA	Vishay-Dale
4	R56, R57, R58, R59	RES, 1.00, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031R00FKEA	Vishay-Dale
1	R60	RES, 0.03, 1%, 1 W, 0612	PRL1632-R030-F-T1	Susumu Co Ltd
2	R61, R110	RES, 10, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	CRCW080510R0JNEA	Vishay-Dale
4	R62, R63, R77, R78	RES, 100, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603100RFKEA	Vishay-Dale
3	R65, R67, R72	RES, 49.9 k, 1%, 0.1 W, 0603	RC0603FR-0749K9L	Yageo
1	R66	RES, 5.23 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06035K23FKEA	Vishay-Dale
1	R68	Res Thick Film 0612 5.11Ohm 1% 1/2W ±100ppm/K Molded Paper T/R	RCL06125R11FKEA	Vishay Dale
1	R69	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603100KFKEA	Vishay-Dale
1	R70	RES, 2.49 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06032K49FKEA	Vishay-Dale
1	R76	RES, 26.7 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	CRCW080526K7FKEA	Vishay-Dale
1	R79	RES, 2.10 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06032K10FKEA	Vishay-Dale
1	R80	RES, 4.42 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06034K42FKEA	Vishay-Dale

Table 5-1. Bill of Materials (continued)

COUNT	DESIGNATOR	DESCRIPTION	PART NUMBER	MANUFACTURER
1	R83	RES, 75.0 k, 1%, 0.1 W, 0603	RC0603FR-0775KL	Yageo
1	R84	RES, 24.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060324K9FKEA	Vishay-Dale
1	R86	RES, 4.02 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06034K02FKEA	Vishay-Dale
1	R87	RES, 1.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K00JNEA	Vishay-Dale
2	R90, R91	RES, 4.99 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06034K99FKEA	Vishay-Dale
1	R100	RES, 2.74 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06032K74FKEA	Vishay-Dale
2	R101, R103	RES, 4.99 k, 1%, 0.1 W, 0603	CRCW06034K99FKEAC	Vishay-Dale
1	R102	RES, 100 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402100KFKED	Vishay-Dale
1	R105	RES, 1.00 k, 1%, 0.1 W, 0603	RC0603FR-071KL	Yageo
15	SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J13, SH-J14, SH-J15	Single Operation 2.54mm Pitch Open Top Jumper Socket	M7582-05	Harwin
4	T1, T2, T3, T4	Terminal 70 A Lug	CXS70-14-C	Panduit
1	U1	Dual Channel 48V-12V Bidirectional PWM Controller	LM5171PHP	Texas Instruments
1	U2	Automotive Qualified Precision, Zero-Crossover, 20 MHz, 0.9pA Ib, RRIO, CMOS Operational Amplifier, DBV0005A (SOT-23-5)	OPA320AQDBVRQ1	Texas Instruments
1	U3	Automotive Catalog Single Differential Comparator 5-SOT-23 -40 to 125	TL331BQDBVRQ1	Texas Instruments
1	U4	Automotive Catalog Single Inverter, DBV0005A, LARGE T&R	SN74LVC1G04QDBVRQ1	Texas Instruments
1	U5	2.2-MHz Wide VIN 65-V Non-synchronous Boost/SEPIC/Flyback Controller with Dual Random Spread Spectrum, DSS0012B (WSON-12)	LM5156DSSR	Texas Instruments
4	U6, U7, U8, U9	1.6V-Capable Temperature Sensor Switch with Factory Programmed Trip Points, NGF0006A (WSON-6)	LM26LVCISD-145/NOPB	Texas Instruments

5.3 Board Layout

The EVM includes various headers for flexible configurations designed for different applications. Figure 5-8 through Figure 5-17 show the EVM PCB images.

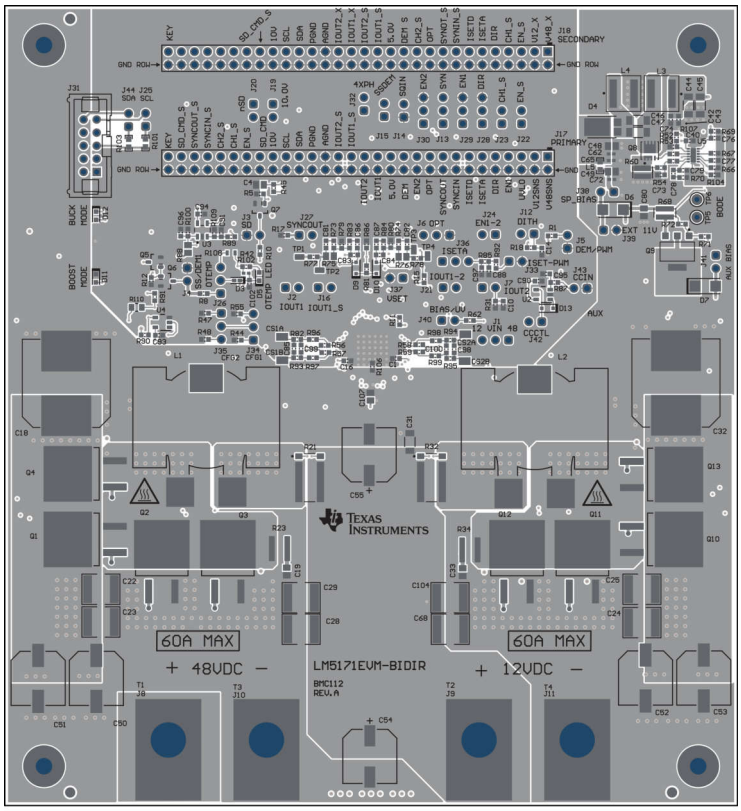

Figure 5-8. EVM Top Layer Silkscreen

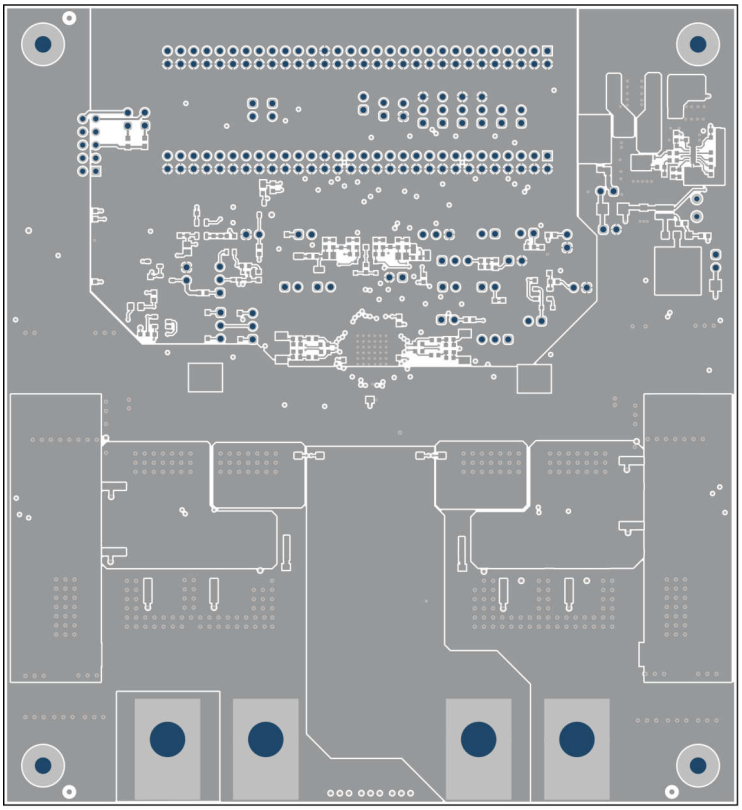

Figure 5-9. EVM Top Layer Copper

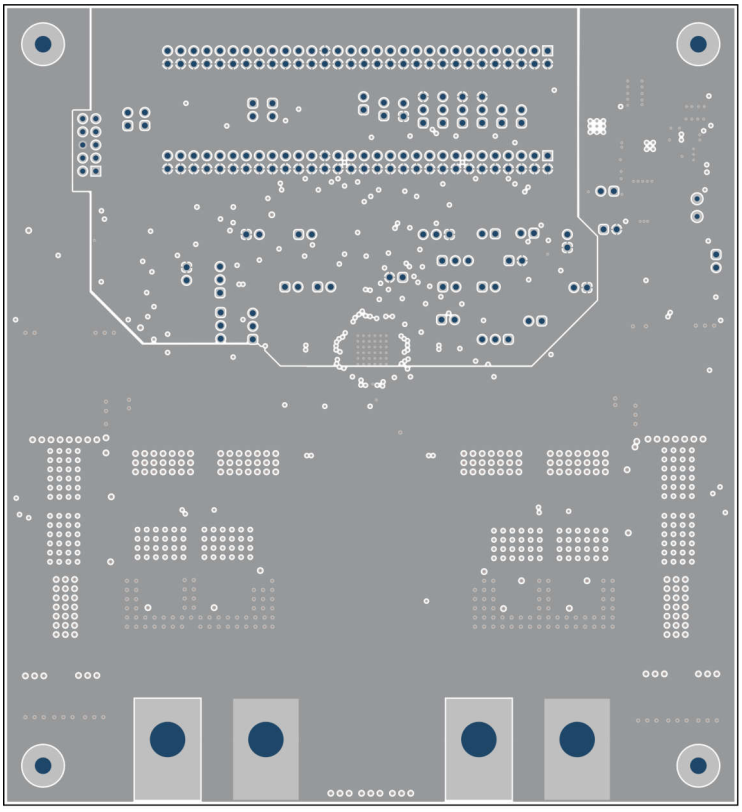

Figure 5-10. EVM Middle Layer 1

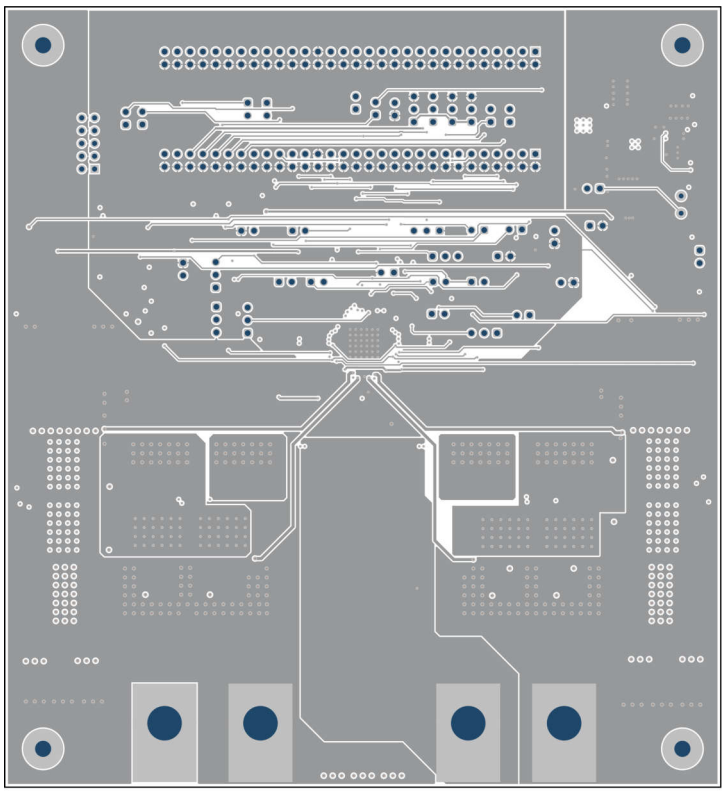

Figure 5-11. EVM Middle Layer 2

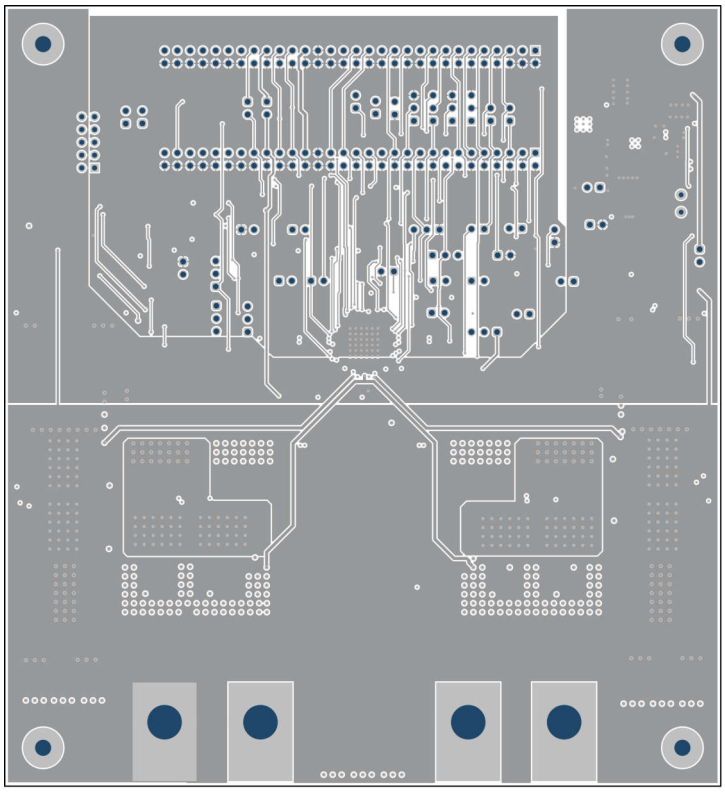

Figure 5-12. EVM Middle Layer 3

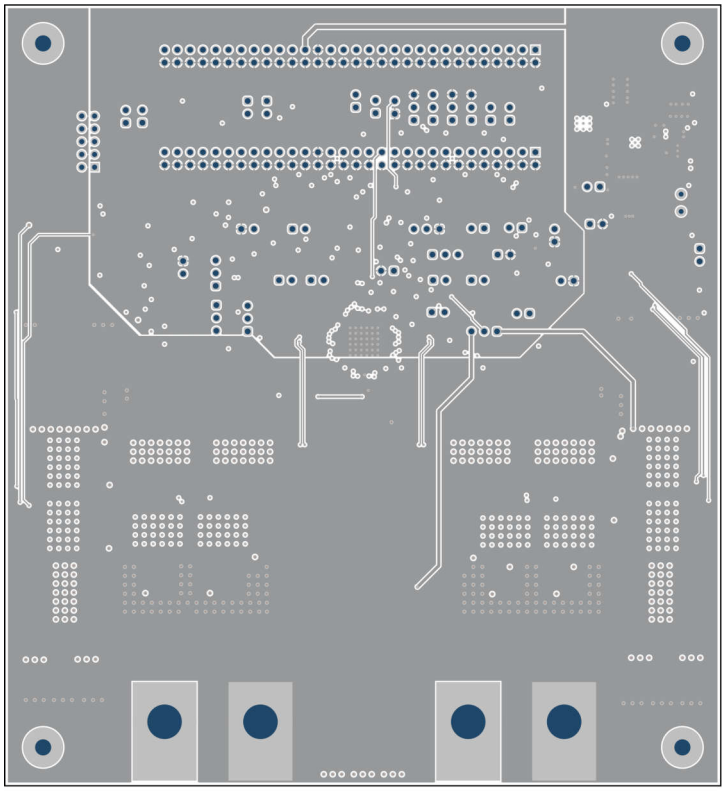

Figure 5-13. EVM Middle Layer 4

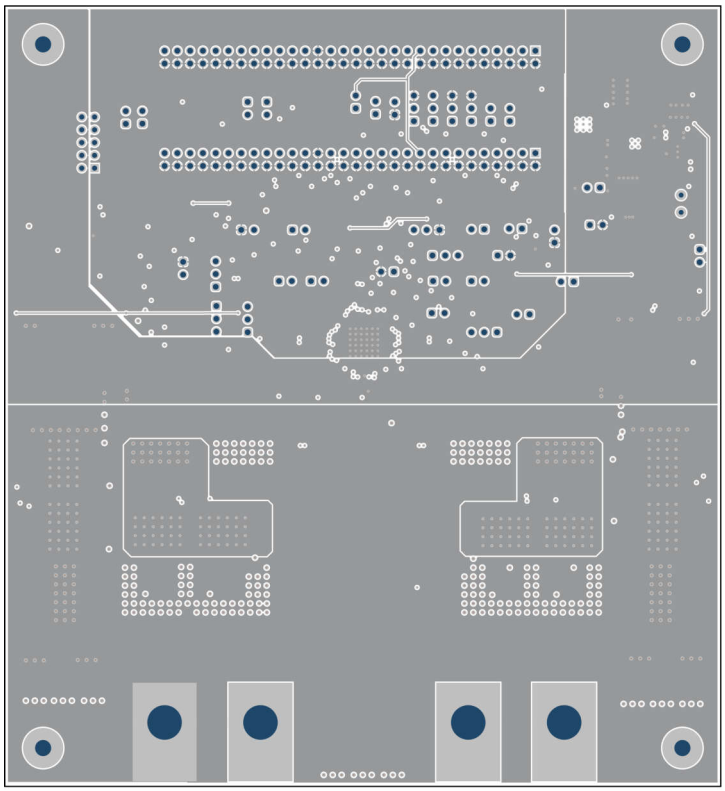

Figure 5-14. EVM Middle Layer 5

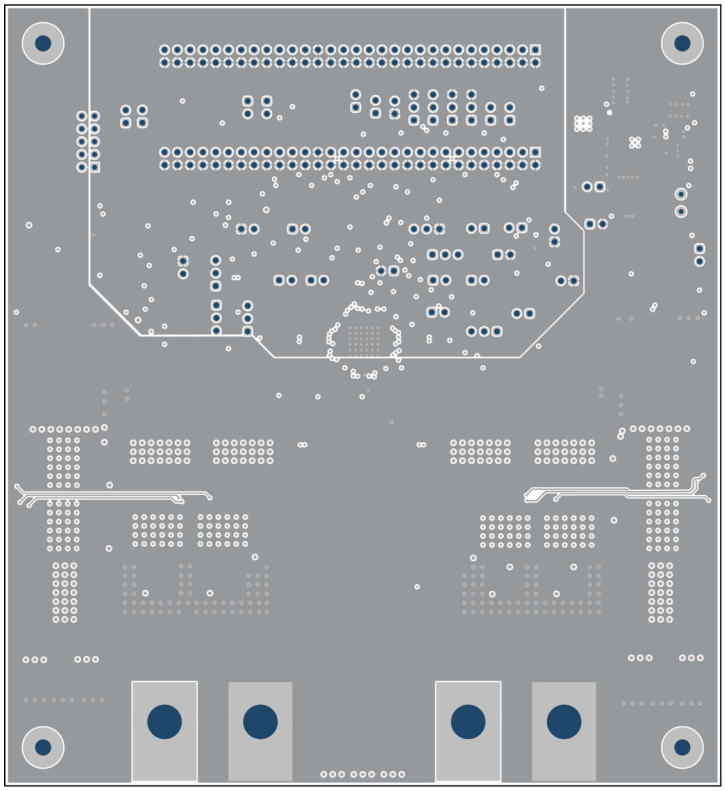

Figure 5-15. EVM Middle Layer 6

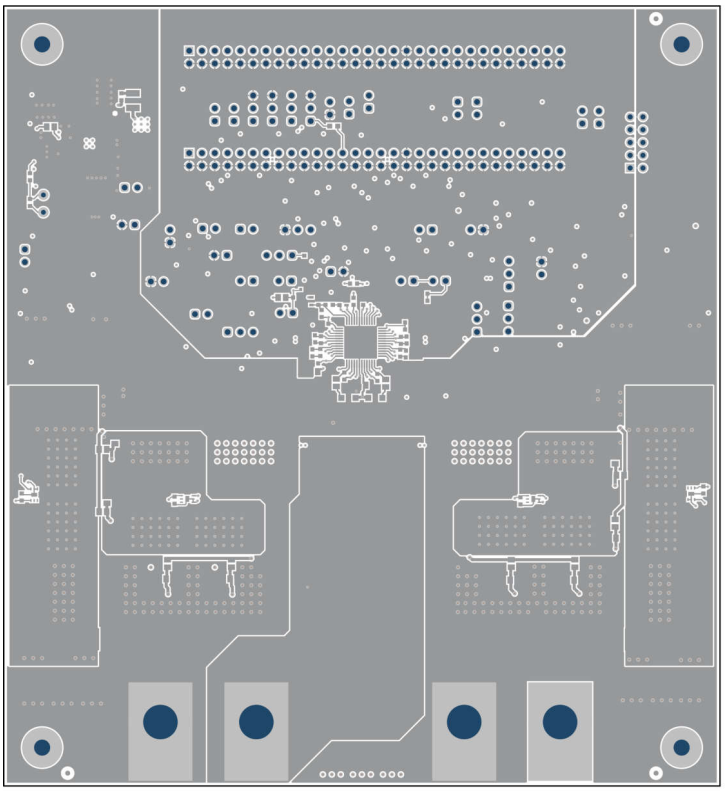

Figure 5-16. EVM Bottom Layer Copper

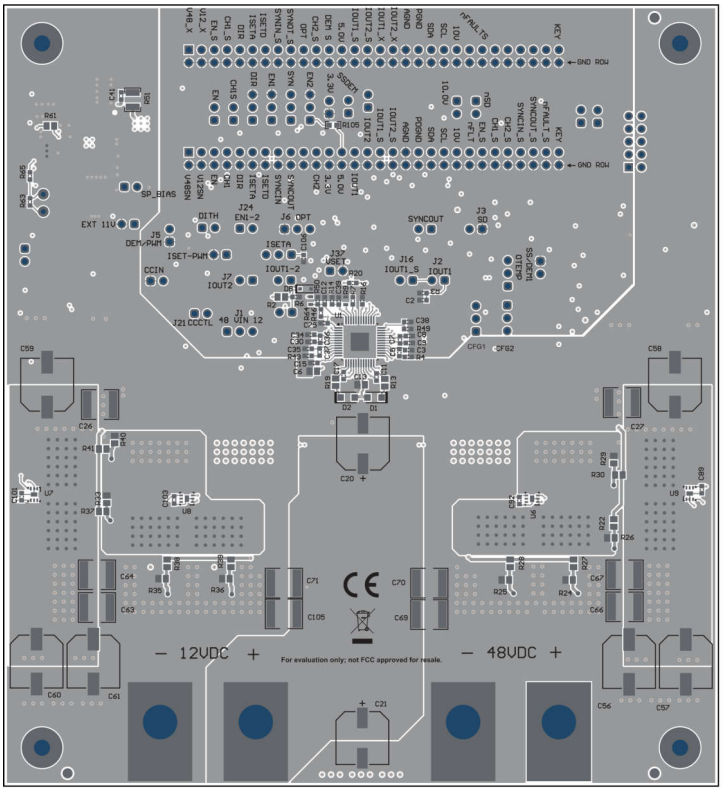

Figure 5-17. EVM Bottom Layer Silkscreen

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2023) to Revision A (November 2023)	Page
• Updated EVM from rev E3 to rev A	1
• Changed device from LM5171-Q1 to LM5171	1
• Updated schematic images	25
• Updated *Bill of Materials* table	29
• Updated board layout images	33

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   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

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   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

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4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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