

# Technical Reference Manual

## LP875241S-Q1 Technical Reference Manual



### ABSTRACT

This document provides the register bit values for the one-time programmable (OTP) bits of the orderable part number LP875241SRNFRQ1.

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## 1 Introduction

This technical reference manual can be used as a reference for the LP875241S-Q1 default register bits after OTP memory download. This technical reference manual does not provide information about the electrical characteristics, external components, package, or the functionality of the device. For this information and the full register map, refer to the [LP8752x-Q1 Four-Phase 10-A Buck Converter With Integrated Switches data sheet](#)

[Table 1-1](#) lists the main OTP settings for power rails. [Table 2-1](#) lists the register bits loaded from OTP memory.

**Table 1-1. Main OTP Settings for Power Rails**

Description		Bit Name	LP875241S-Q1 Value
Device identification	OTP configuration	OTP_ID	0x19
BUCK0	Output voltage	BUCK0_VSET	900 mV
	Enable, EN pin, or I <sup>2</sup> C register	EN_BUCK0, EN_PIN_CTRL0, BUCK0_EN_PIN_SELECT	EN1
	Force PWM	BUCK0_FPWM	Yes
	Peak current limit	ILIM0	3.5 A
	Maximum load current	N/A	2.5 A
	Slew rate	SLEW_RATE0	1.9 mV/μs
BUCK1	Output voltage	BUCK1_VSET	900 mV
	Enable, EN pin, or I <sup>2</sup> C register	EN_BUCK1, EN_PIN_CTRL1, BUCK1_EN_PIN_SELECT	EN1
	Force PWM	BUCK1_FPWM	Yes
	Peak current limit	ILIM1	3.5 A
	Maximum load current	N/A	2.5 A
	Slew Rate	SLEW_RATE1	1.9 mV/μs

**Table 1-1. Main OTP Settings for Power Rails (continued)**

Description	Bit Name	LP875241S-Q1 Value	
BUCK2	Output voltage	BUCK2_VSET	900 mV
	Enable, EN pin, or I <sup>2</sup> C register	EN_BUCK2, EN_PIN_CTRL2, BUCK2_EN_PIN_SELECT	EN3
	Force PWM	BUCK2_FPWM	Yes
	Peak current limit	ILIM2	4 A
	Maximum load current	N/A	3 A
	Slew rate	SLEW_RATE2	1.9 mV/μs
BUCK3	Output voltage	BUCK3_VSET	1000 mV
	Enable, EN pin, or I <sup>2</sup> C register	EN_BUCK3, EN_PIN_CTRL3, BUCK3_EN_PIN_SELECT	EN3
	Force PWM	BUCK3_FPWM	Yes
	Peak current limit	ILIM3	3.5 A
	Maximum load current	N/A	2.5 A
	Slew rate	SLEW_RATE3	1.9 mV/μs
Switching frequency	N/A	2 MHz	
I <sup>2</sup> C address	N/A	0x60	

**Note**

The maximum total output capacitance (local + POL) per phase (BUCK0, BUCK1, BUCK2, and BUCK3) depends on the slew rate setting. Check the data sheet for the allowed capacitance value.

## 2 Register Bits Loaded From OTP Memory

Table 2-1 lists the register bit values loaded from the OTP memory during device start-up.

**Table 2-1. Summary of Registers Bits**

Address	Register Name	Bit	LP87241S-Q1 Value
0x01	OTP_REV	OTP_ID[7:0]	0x19
0x02	BUCK0_CTRL1	EN_BUCK0	0x01
0x02	BUCK0_CTRL1	EN_PIN_CTRL0	0x01
0x02	BUCK0_CTRL1	BUCK0_EN_PIN_SELECT[1:0]	0x00
0x02	BUCK0_CTRL1	BUCK0_FPWM	0x01
0x02	BUCK0_CTRL1	BUCK0_FPWM_MP	0x00
0x03	BUCK0_CTRL2	ILIM0[2:0]	0x04
0x03	BUCK0_CTRL2	SLEW_RATE0[2:0]	0x05
0x04	BUCK1_CTRL1	EN_BUCK1	0x01
0x04	BUCK1_CTRL1	EN_PIN_CTRL1	0x01
0x04	BUCK1_CTRL1	BUCK1_EN_PIN_SELECT[1:0]	0x00
0x04	BUCK1_CTRL1	BUCK1_FPWM	0x01
0x05	BUCK1_CTRL2	ILIM1[2:0]	0x04
0x05	BUCK1_CTRL2	SLEW_RATE1[2:0]	0x05
0x06	BUCK2_CTRL1	EN_BUCK2	0x01
0x06	BUCK2_CTRL1	EN_PIN_CTRL2	0x01
0x06	BUCK2_CTRL1	BUCK2_EN_PIN_SELECT[1:0]	0x02
0x06	BUCK2_CTRL1	BUCK2_FPWM	0x01
0x06	BUCK2_CTRL1	BUCK2_FPWM_MP	0x00
0x07	BUCK2_CTRL2	ILIM2[2:0]	0x05
0x07	BUCK2_CTRL2	SLEW_RATE2[2:0]	0x05
0x08	BUCK3_CTRL1	EN_BUCK3	0x01
0x08	BUCK3_CTRL1	EN_PIN_CTRL3	0x01
0x08	BUCK3_CTRL1	BUCK3_EN_PIN_SELECT[1:0]	0x02
0x08	BUCK3_CTRL1	BUCK3_FPWM	0x01
0x09	BUCK3_CTRL2	ILIM3[2:0]	0x04
0x09	BUCK3_CTRL2	SLEW_RATE3[2:0]	0x05
0x0A	BUCK0_VOUT	BUCK0_VSET[7:0]	0x39
0x0C	BUCK1_VOUT	BUCK1_VSET[7:0]	0x39
0x0E	BUCK2_VOUT	BUCK2_VSET[7:0]	0x39
0x10	BUCK3_VOUT	BUCK3_VSET[7:0]	0x4D
0x12	BUCK0_DELAY	BUCK0_SHUTDOWN_DELAY[3:0]	0x00
0x12	BUCK0_DELAY	BUCK0_STARTUP_DELAY[3:0]	0x00
0x13	BUCK1_DELAY	BUCK1_SHUTDOWN_DELAY[3:0]	0x00
0x13	BUCK1_DELAY	BUCK1_STARTUP_DELAY[3:0]	0x00
0x14	BUCK2_DELAY	BUCK2_SHUTDOWN_DELAY[3:0]	0x00
0x14	BUCK2_DELAY	BUCK2_STARTUP_DELAY[3:0]	0x00
0x15	BUCK3_DELAY	BUCK3_SHUTDOWN_DELAY[3:0]	0x00
0x15	BUCK3_DELAY	BUCK3_STARTUP_DELAY[3:0]	0x00
0x16	GPIO2_DELAY	GPIO2_SHUTDOWN_DELAY[3:0]	0x00
0x16	GPIO2_DELAY	GPIO2_STARTUP_DELAY[3:0]	0x00
0x17	GPIO3_DELAY	GPIO3_SHUTDOWN_DELAY[3:0]	0x00
0x17	GPIO3_DELAY	GPIO3_STARTUP_DELAY[3:0]	0x00
0x19	CONFIG	DOUBLE_DELAY	0x00
0x19	CONFIG	CLKIN_PD	0x01
0x19	CONFIG	EN4_PD	0x00
0x19	CONFIG	EN3_PD	0x01
0x19	CONFIG	TDIE_WARN_LEVEL	0x01

**Table 2-1. Summary of Registers Bits (continued)**

Address	Register Name	Bit	LP87241S-Q1 Value
0x19	CONFIG	EN2_PD	0x01
0x19	CONFIG	EN1_PD	0x01
0x21	TOP_MASK1	GPIO_MASK	0x01
0x21	TOP_MASK1	SYNC_CLK_MASK	0x01
0x21	TOP_MASK1	TDIE_WARN_MASK	0x00
0x21	TOP_MASK1	I_LOAD_READY_MASK	0x01
0x22	TOP_MASK2	RESET_REG_MASK	0x01
0x23	BUCK_0_1_MASK	BUCK1_PG_MASK	0x00
0x23	BUCK_0_1_MASK	BUCK1_ILIM_MASK	0x00
0x23	BUCK_0_1_MASK	BUCK0_PG_MASK	0x00
0x23	BUCK_0_1_MASK	BUCK0_ILIM_MASK	0x00
0x24	BUCK_2_3_MASK	BUCK3_PG_MASK	0x00
0x24	BUCK_2_3_MASK	BUCK3_ILIM_MASK	0x00
0x24	BUCK_2_3_MASK	BUCK2_PG_MASK	0x00
0x24	BUCK_2_3_MASK	BUCK2_ILIM_MASK	0x00
0x28	PGOOD_CTRL1	PG3_SEL[1:0]	0x01
0x28	PGOOD_CTRL1	PG2_SEL[1:0]	0x01
0x28	PGOOD_CTRL1	PG1_SEL[1:0]	0x01
0x28	PGOOD_CTRL1	PG0_SEL[1:0]	0x01
0x29	PGOOD_CTRL2	HALF_DELAY	0x00
0x29	PGOOD_CTRL2	EN_PG0_NINT	0x00
0x29	PGOOD_CTRL2	PGOOD_SET_DELAY	0x00
0x29	PGOOD_CTRL2	EN_PGFLT_STAT	0x00
0x29	PGOOD_CTRL2	PGOOD_WINDOW	0x01
0x29	PGOOD_CTRL2	PGOOD_OD	0x00
0x29	PGOOD_CTRL2	PGOOD_POL	0x00
0x2B	PLL_CTRL	PLL_MODE[1:0]	0x00
0x2B	PLL_CTRL	EXT_CLK_FREQ[4:0]	0x01
0x2C	PIN_FUNCTION	EN_SPREAD_SPEC	0x01
0x2C	PIN_FUNCTION	EN_PIN_CTRL_GPIO3	0x01
0x2C	PIN_FUNCTION	EN_PIN_SELECT_GPIO3	0x00
0x2C	PIN_FUNCTION	EN_PIN_CTRL_GPIO2	0x01
0x2C	PIN_FUNCTION	EN_PIN_SELECT_GPIO2	0x00
0x2C	PIN_FUNCTION	GPIO3_SEL	0x00
0x2C	PIN_FUNCTION	GPIO2_SEL	0x00
0x2C	PIN_FUNCTION	GPIO1_SEL	0x00
0x2D	GPIO_CONFIG	GPIO3_OD	0x01
0x2D	GPIO_CONFIG	GPIO2_OD	0x01
0x2D	GPIO_CONFIG	GPIO1_OD	0x00
0x2D	GPIO_CONFIG	GPIO3_DIR	0x00
0x2D	GPIO_CONFIG	GPIO2_DIR	0x00
0x2D	GPIO_CONFIG	GPIO1_DIR	0x00
0x2F	GPIO_OUT	GPIO3_OUT	0x01
0x2F	GPIO_OUT	GPIO2_OUT	0x01

### 3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>DATE</b>	<b>REVISION</b>	<b>NOTES</b>
June 2024	*	Initial Release

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