

EVM User's Guide: LMG5126

LMG5126EVM Evaluation Module



Description

The LMG5126EVM evaluation module showcases the features and performance of the LMG5126 wide input voltage synchronous GaN boost converter. This EVM is designed for ease of configuration, enabling the user to evaluate many different applications on the same module. The standard configuration is designed to provide a regulated output voltage of 24V and switching at 420kHz. The output voltage can be dynamically adjusted via the ATRK/DTRK pin.

Get Started

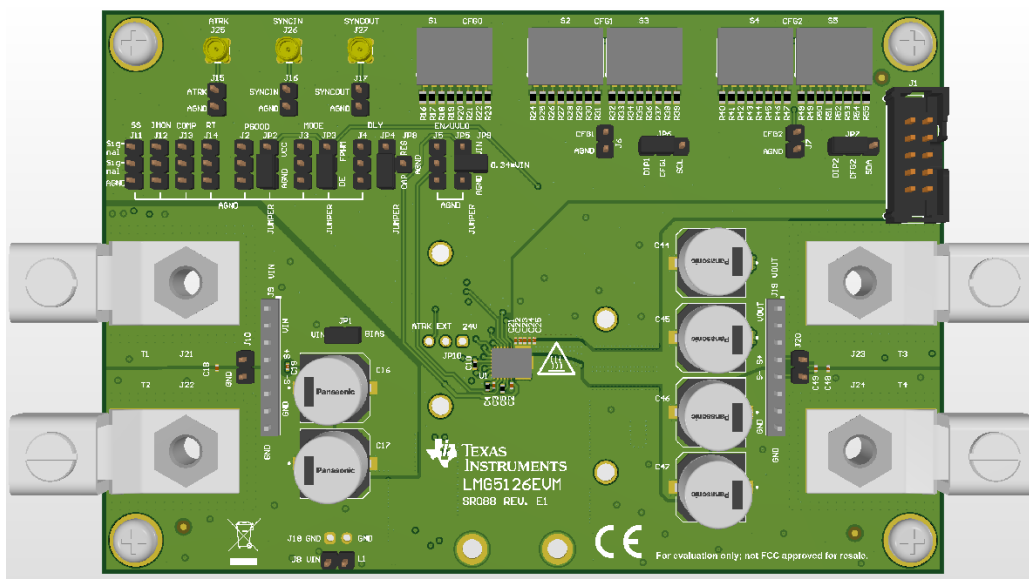
1. Connect EVM to power supply and load

Features

- Stackable
- Output voltage tracking
- Wide input voltage range
- Inductor current monitoring and average current limit
- Bypass mode, PGOOD indicator and Dual Random Spread Spectrum (DRSS)
- Soft-start and peak current limit
- Optional synchronization (SYNC)
- Programmable line undervoltage lockout (UVLO) and hysteresis

Applications

- Automotive Class H audio power amplifier
- Automotive LED headlight applications



1 Evaluation Module Overview

1.1 Introduction

The LMG5126EVM evaluation module provides the design engineer with a fully functional synchronous boost converter to evaluate the The LMG5126 synchronous GaN boost converter. The EVM operates over an input voltage range of 8V to 18V and can handle input transients up to 42V. The EVM provides an output voltage of 24V with 350W maximum power. The output voltage can also be adjusted up to 60V via ATRK/DTRK pin. [Figure 1-1](#) shows the standard application circuit for the LMG5126EVM evaluation module.

1.2 Kit Contents

- One LMG5126EVM PCB assembly
- EVM Disclaimer Read Me

1.3 Specification

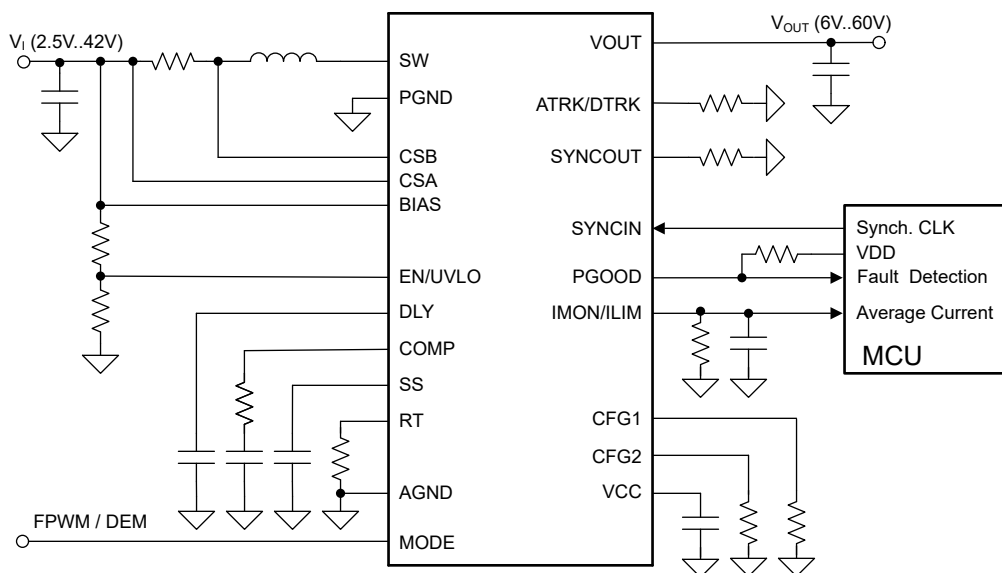


Figure 1-1. Typical Application Circuit

1.4 Device Information

The LMG5126 is a synchronous GaN boost converter. It enters bypass mode when input voltage is higher than the desired output voltage.

- Wide input voltage range from 2.5V to 42V
- Output Voltage 6V to 60V
- Peak current regulation scheme
- Dynamic output voltage tracking
 - Analog and digital PWM tracking input
- Minimum quiescent current
 - Low shut down I_q of 50 μ A

2 Hardware

2.1 EVM characteristics, Test Point, and Connector Description

[Section 2.1](#) describes the operating conditions for the EVM, as well as the configuration points of the evaluation module.

2.1.1 EVM Characteristics

[Table 2-1](#) details the EVM characteristics.

Table 2-1. EVM Characteristics

Parameter	Test Condition		MIN	TYP	MAX	UNIT
INPUT VOLTAGE CHARACTERISITCS						
Input Voltage Range	Operation		8	14	18	V
	UVLO voltage levels	Turn-on		4.2		V
		Turn-off		3.9		V
Input Current	No load operation Vin=12V, Vout=24V			1.7		mA
OUTPUT CHARACTERISITCS						
Output Voltage	R _{ATRK} = 40.2 kΩ			24		V
	R _{ATRK} = 75 kΩ			45		V
Output Power	Vin=16V, JP4 Pin2-JP8 (average current limit feature deactivated)				350	W
SYSTEM CHARACTERISITCS						
Switching Frequency				420		kHz
Full Load Efficiency	V _{IN} = 12 V, V _{OUT} = 24 V			95.6		%

2.1.2 EVM Connectors and Test Points

Section 2.1.2 describes the connection points of the evaluation module. Table 2-2 to Table 2-4 describe these connections. Table 2-2 lists the power connections of the evaluation module. These connections are intended to handle relatively large currents.

Table 2-2. Power Connections

Connector	Pin	Description
T1	VIN+	Positive input voltage power for the evaluation module
T2	VIN-	Negative input voltage power for the evaluation module
T3	VOUT+	Positive output voltage power for the evaluation module
T4	VOUT-	Negative output voltage power for the evaluation module
J9	VIN	Positive input voltage pin 1 - pin 3, negative input pin 6 - pin 8 (Pin 4 and 5 are only for sensing the input voltage)
J19	VOUT	Positive output voltage pin 1 - pin 3, negative output pin 6 - pin 8 (Pin 4 and 5 are only for sensing the output voltage)

Table 2-3 lists the EVM jumpers and test points that configure the LM5125-Q1 and LM51251-Q1 as desired. These jumpers can set different modes of operation or provide signals to different pins of the LM5125-Q1 and LM51251-Q1.

Table 2-3. Programmable Jumper Connections

Connector	Pins	Description	Default Connection
JP1	BIAS to VIN	Connecting BIAS pin of LMG5126 to the VIN	X
JP2	Pin1 to pin 2	Connecting PGOOD pin to the VCC enabling the power good indicator	X
	OPEN	If power good indicator is not used this pin can be left floating	
JP3	Pin 1 to pin 2	Connecting MODE pin to VCC to enable FPWM mode	X
	Pin 2 to Pin 3	Connecting MODE pin to AGND to enable DEM	
JP4	Pin1 to pin 2	Connecting DLY pin to a resistor to disable delay function and average current limit feature	
	Pin 2 to Pin 3	Connecting DLY pin to a capacitor to enable delay function	X
	Pin 2 to JP8	Connecting DLY pin to GND to disable delay function and average current limit feature	
JP5	Pin 1 to pin 2	UVLO/EN Connected to VIN as VIN ramps up the UVLO/EN pin also ramps up and LMG5126 is enabled once the UVLO threshold is surpassed.	
	Pin 2 to pin 3	Connects EN2 to AGND disabling LMG5126	
	Pin 2 to JP9	EN/UVLO pin tied to resistor divider network consisting of R14, R15 and C51, where this resistor divider network sets the UVLO threshold for enabling LMG5126.	X
JP6	Pin 1 to Pin 2	Uses DIP switches S2 and S3 for CFG1 settings	X
	Pin 2 to Pin 3	Sets CFG1 as I2C pin for I2C version	
JP7	Pin 1 to pin 2	Uses DIP switches S4 and S5 for CFG2 settings	X
	Pin 2 to pin 3	Sets CFG2 as I2C pin for I2C version	
JP10	Pin 1 to pin 2	Connecting ATRK to 40.2k resistor to set Vout to 24V	X
	Pin 2 to pin 3	Connecting ATRK to J15 to supply from external	
J25	MMCX jack	Digital PWM signal input to the ATRK/DTRK Pin	
J26	MMCX jack	External syncin	
J27	MMCX jack	External SYNCOUT	

Table 2-4 indicates the dedicated voltage probe points of the EVM. These points are used to make measurements on the EVM.

Table 2-4. Probe Points

Sense Point	Name	Description
TP1	SW	Sense point for switch node of the Boost converter
J1	I2C	I2C measuring header with analog ground
J2	PGOOD	Power Good measuring header with analog ground
J3	MODE	MODE pin measuring header with analog ground
J4	DLY	DLY pin measuring header with analog ground
J5	UVLO	UVLO pin measuring header with analog ground
J6	CFG1	CFG1 pin measuring header with analog ground
J7	CFG2	CFG2 pin header with analog ground
J8	CS	Terminals of the current sense resistors
J10	Vin sense	Sense pins for the input voltage
J11	SS	SS pin measuring header with analog ground
J12	ILIM/IMON	ILIM/IMON pin header with analog ground
J13	COMP	COMP pin header with analog ground
J14	RT	RT pin header with analog ground
J15	ATRK	ATRK pin header with analog ground
J16	SYNCIN	SYNCIN pin header with analog ground
J17	SYNCOUT	SYNCOUT pin header with analog ground
J18	PGND	Connection to PGND
J20	Vout sense	Sense pins for the output voltage

3 EVM Configurations

Section 3 shows modifications outside of the default configuration that are used to further evaluate the LMG5126.

3.1 Output Voltage Tracking

Section 3.1 describes how to setup the evaluation module for dynamic output voltage tracking.

The LMG5126EVM is typically configured to have fixed output voltage of 24V. Figure 3-1 shows the resistor from the ATRK/DTRK pin to the analog ground sets the output voltage to 24V. R_{ATRK} is R11 referring to the schematic.

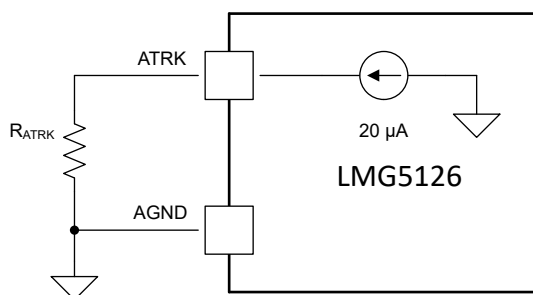


Figure 3-1. Fixed Output Voltage Configuration

To dynamically change the output voltage via analog signal, R_{ATRK} is removed or disconnected via jumper JP10 and the ATRK/DTRK pin voltage is driven directly to change the output voltage. See the LMG5126 datasheet for selecting the voltage range and setting the ATRK pin voltage to produce the desired output voltage. Figure 3-2 shows the configuration to change the output voltage dynamically by applying voltage or supplying analog signal.

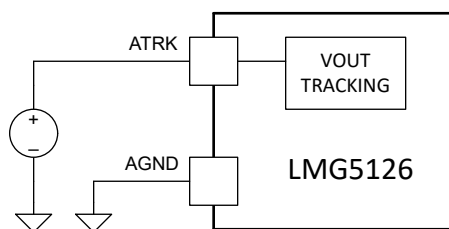


Figure 3-2. Variable Output Voltage Configuration via analog signal

Applying an analog voltage of around 0.8V and 1.5V to the ATRK/DTRK pin, will set the output voltage of 24V and 45V respectively.

To dynamically change the output voltage digitally, R_{ATRK} is removed or disconnected via jumper JP2 and the ATRK/DTRK pin is fed a PWM signal directly to change the output voltage. See the LMG5126 datasheet for setting the PWM duty cycle of DTRK pin voltage to produce the desired output voltage. Figure 3-3 shows the configuration to change the output voltage dynamically by applying a digital signal.

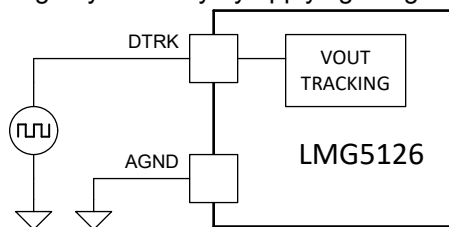


Figure 3-3. Variable Output Voltage Configuration via digital signal

Applying a PWM signal on the ATRK/DTRK pin with duty cycle of 32% and 60%, will set the output voltage to 24V and 45V respectively.

3.2 Device configuration

LMG5126 can be configured using three pins SYNCOUT, CFG1 and CFG2 . In the LMG5126EVM, these pins can be configured through the five DIP switches, when the jumpers on connectors JP6 and JP7 are connecting CFG1 to DIP1 and CFG2 to DIP2 respectively, by selecting one of the 16 levels presented for each of the two configuration pins. Each DIP switch has 8 toggling switches that either connects or disconnects a fixed valued resistor from the configuration pins. It is important to note that at one time there should be only one of the 16 levels, for each configuration pin, selected to configure the LMG5126 as seen below and according to the information given on the LMG5126 datasheet.

The SYNCOUT-pin defines the overvoltage protection level and the ATRK/DTRK-pin 20uA current used for output voltage programming via resistor.

Table 3-1. CFG0-Pin Settings

Level	OVP level	20 uA ATRK current
1	25V	ON
2	25V	OFF
3	35V	ON
4	35V	OFF
5	50V	ON
6	50V	OFF
7	65V	ON
8	65V	OFF

The CFG1-pin setting defines the Clock Dithering, the peak current limit (ICL_latch) operation, current sense voltage level and the gate driver strength.

Table 3-2. CFG1-Pin Settings

Level	Spread Spectrum	Sense voltage	ICL_latch	Gate drive strength
1	DRSS ON	30mV	enabled	weak
2	DRSS ON	60mV	enabled	weak
3	DRSS ON	30mV	enabled	strong
4	DRSS ON	60mV	enabled	strong
5	DRSS ON	30mV	disabled	weak
6	DRSS ON	60mV	disabled	weak
7	DRSS ON	30mV	disabled	strong
8	DRSS ON	60mV	disabled	strong
9	DRSS OFF	30mV	enabled	weak
10	DRSS OFF	60mV	enabled	weak
11	DRSS OFF	30mV	enabled	strong
12	DRSS OFF	60mV	enabled	strong
13	DRSS OFF	30mV	disabled	weak
14	DRSS OFF	60mV	disabled	weak
15	DRSS OFF	30mV	disabled	strong
16	DRSS OFF	60mV	disabled	strong

The CFG2-pin defines if the device is configured for a single-or multichip setup, which then defines the operation mode of SYNCIN and SYNCOUT pin. Also PGOOD OVP can be set.

Table 3-3. CFG2-Pin Settings

Level	Single/Multichip	SYNCOUT	SYNCIN	PGOOD OVP enable
1	Single	OFF	OFF	ON
2	Single	OFF	ON	ON
3	Primary	90°	ON	ON
4	Primary	120°	ON	ON
5	Primary	180°	ON	ON
6	Secondary	OFF	ON	ON
7	Secondary	90°	ON	ON
8	Secondary	120°	ON	ON
9	Single	OFF	OFF	OFF
10	Single	OFF	ON	OFF
11	Primary	90°	ON	OFF
12	Primary	120°	ON	OFF
13	Primary	180°	ON	OFF
14	Secondary	OFF	ON	OFF
15	Secondary	90°	ON	OFF
16	Secondary	120°	ON	OFF

4 Implementation Results

4.1 Test Setup and Procedure

4.1.1 Test Setup

Figure 4-1 shows the required test setup to evaluate the LMG5126EVM

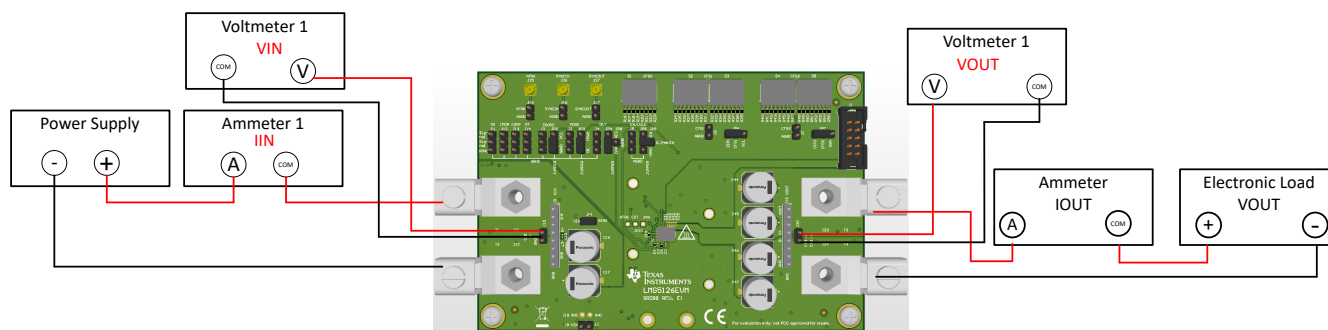


Figure 4-1. EVM Test Setup

4.1.2 Test Procedure and Equipment

The following test equipment is needed to test the LMG5126EVM:

- Power supply: The input voltage source (V_{IN}) should be a variable supply. The power supply should source up to at least 20V and be able to supply more than 30A of current. Turn off the power supply. Connect the positive output of the power supply to T1 and the negative output to T2.
- Electronic Load: Connect the load to T3 for the positive connection and T4 for the negative connection. The electronic load should be able to dissipate 350W at 60V.

Multimeters: For DC measurements, connected as shown in Figure 5-1.

- Voltmeter 1 (V_{IN}): Capable of measuring the input voltage range up to at least 20V
- Voltmeter 2 (V_{OUT}): Capable of measuring output voltage of 60V
- Ammeter 1 (I_{IN}): Capable of 30A DC measurement. A shunt resistor may also be used to measure the input current
- Ammeter 2 (I_{OUT}): Capable of at least 15A DC measurement
- Oscilloscope: minimum of 20MHz bandwidth and 10x probes.
- Set the power supply voltage to 12V and the electronic load to 0.1A. The electronic load voltage must be in regulation with a nominal 24V output.
- Slowly increase the load while monitoring the output voltage between J23-VOUT and J24-GND. The voltage must remain in regulation with a nominal 24V output as the load is increased up to 7A.
- Slowly sweep the input voltage from 8V to 18V. The output voltage must remain in regulation with a nominal 24V output.
- Slowly sweep the input voltage from 18V to 8V. The output voltage must remain in regulation with a nominal 24V output.

4.1.3 Precautions



Board surface and heatsink is hot. Do not touch! Contact may cause burns.

5 Hardware Design Files

5.1 Schematic

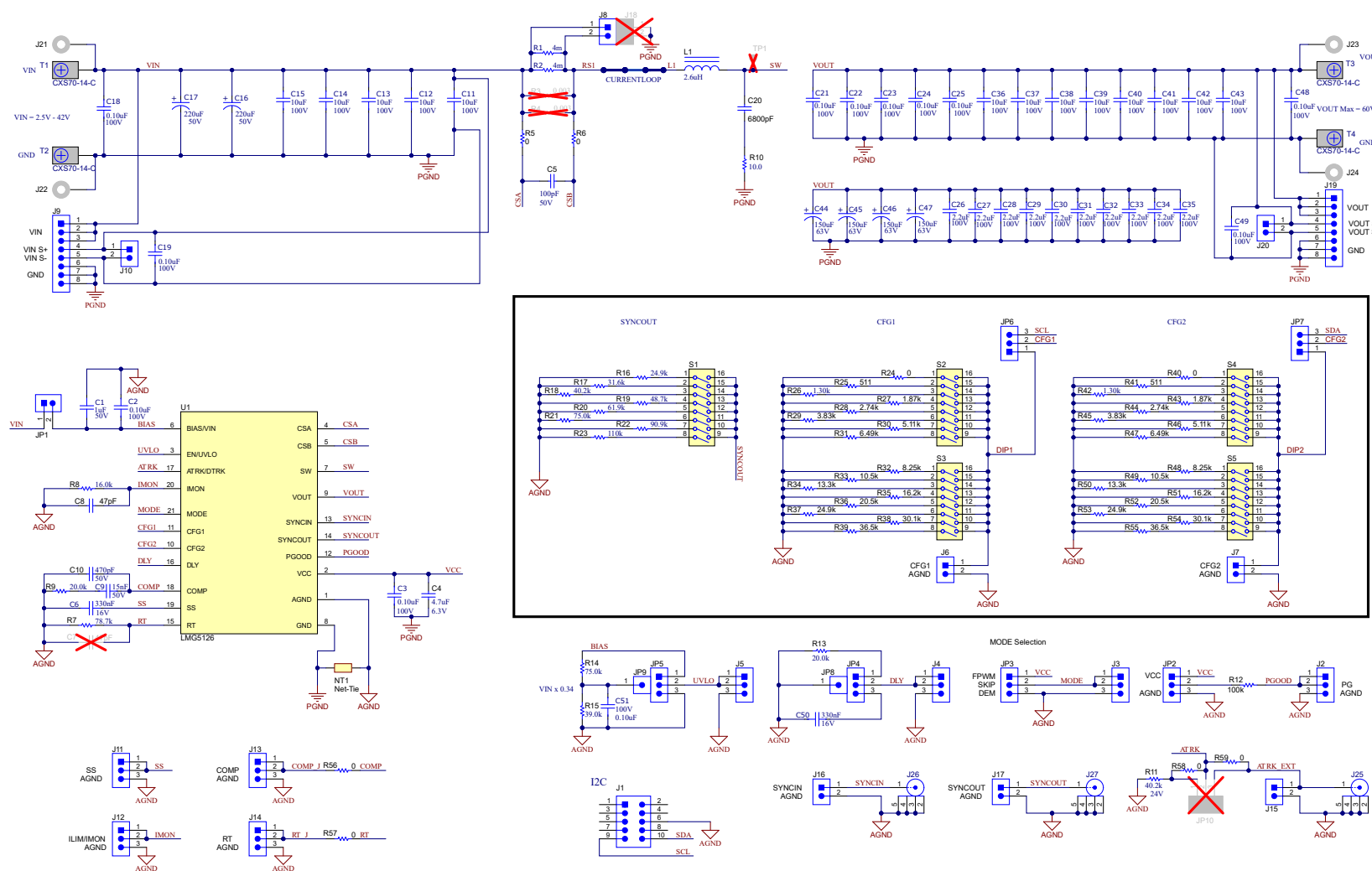


Figure 5-1. Schematic

5.2 PCB Layers

Figure 5-2 through Figure 5-3 illustrate the EVM PCB layout.

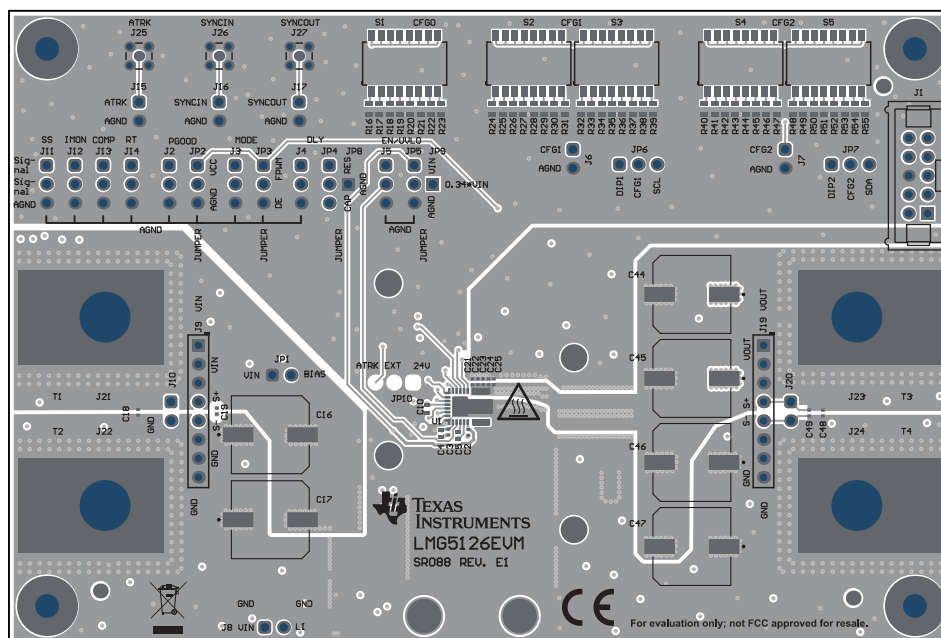


Figure 5-2. Top Silk Screen

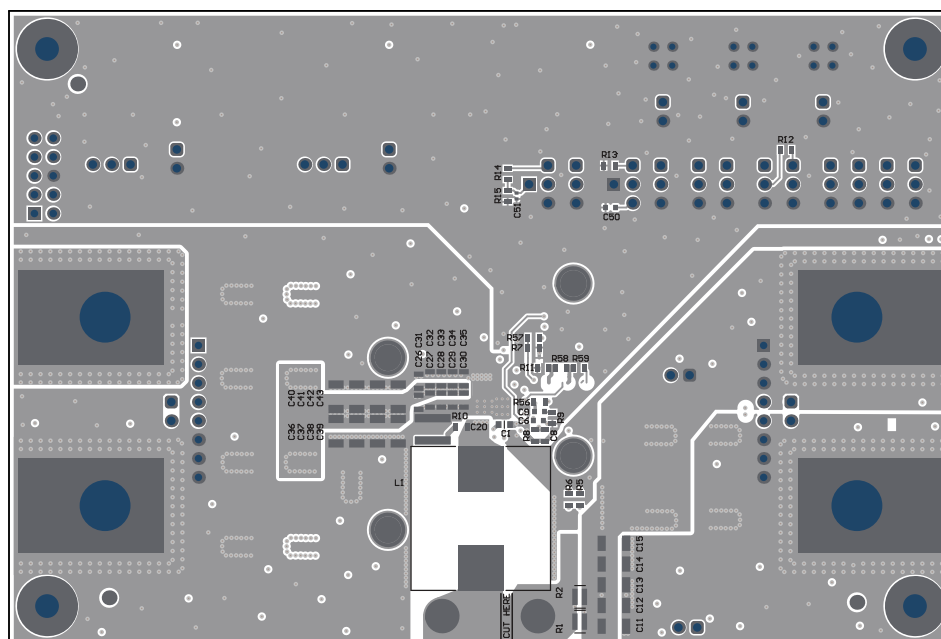
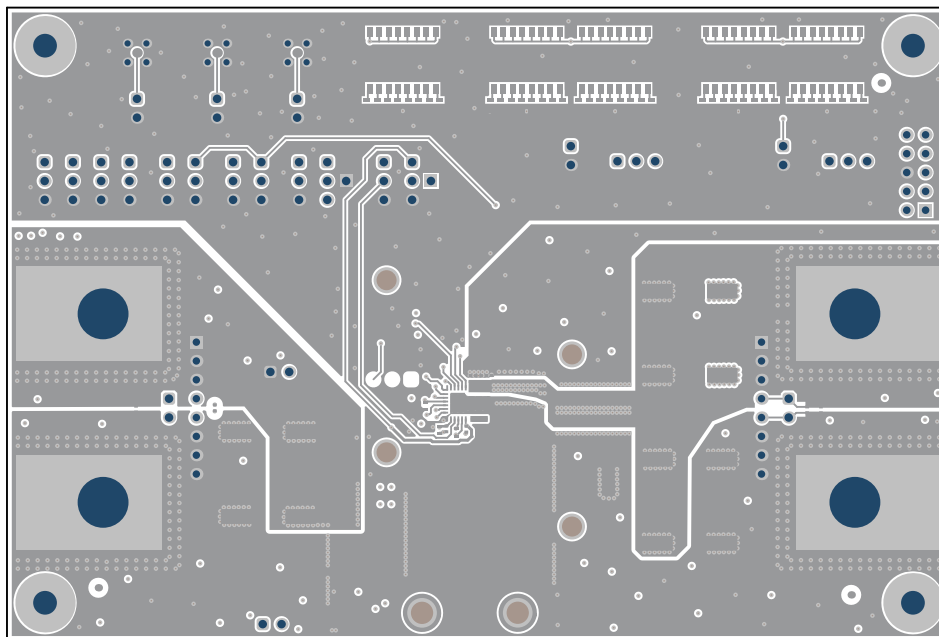
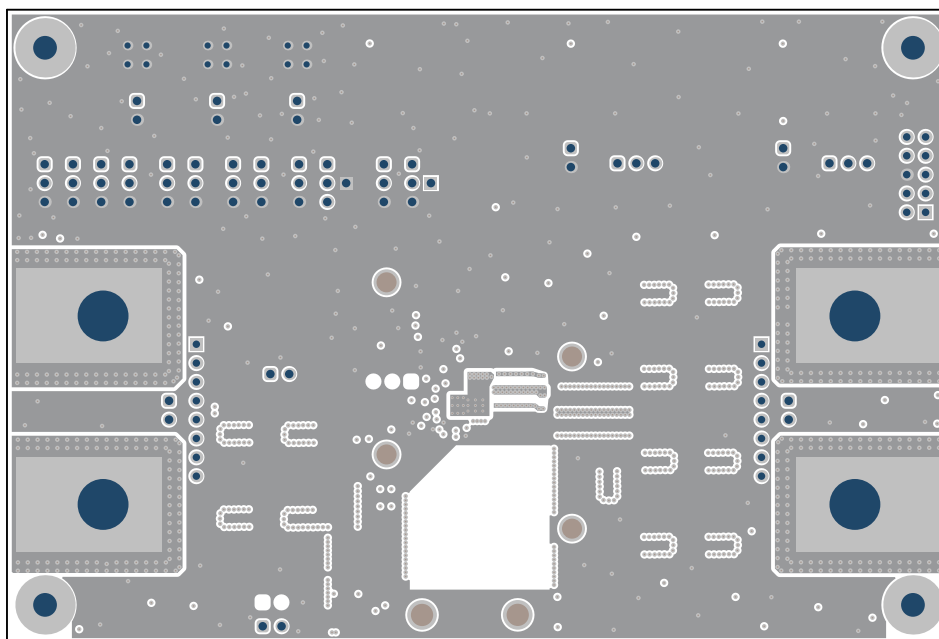


Figure 5-3. Bottom Silk Screen

**Figure 5-4. Top Layer****Figure 5-5. Signal Layer 1**

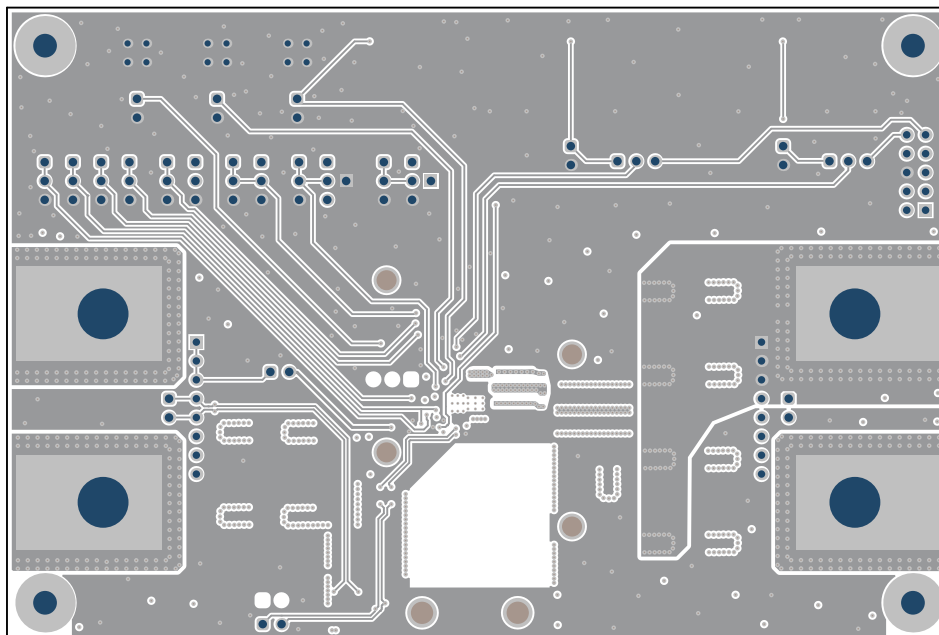


Figure 5-6. Signal Layer 2

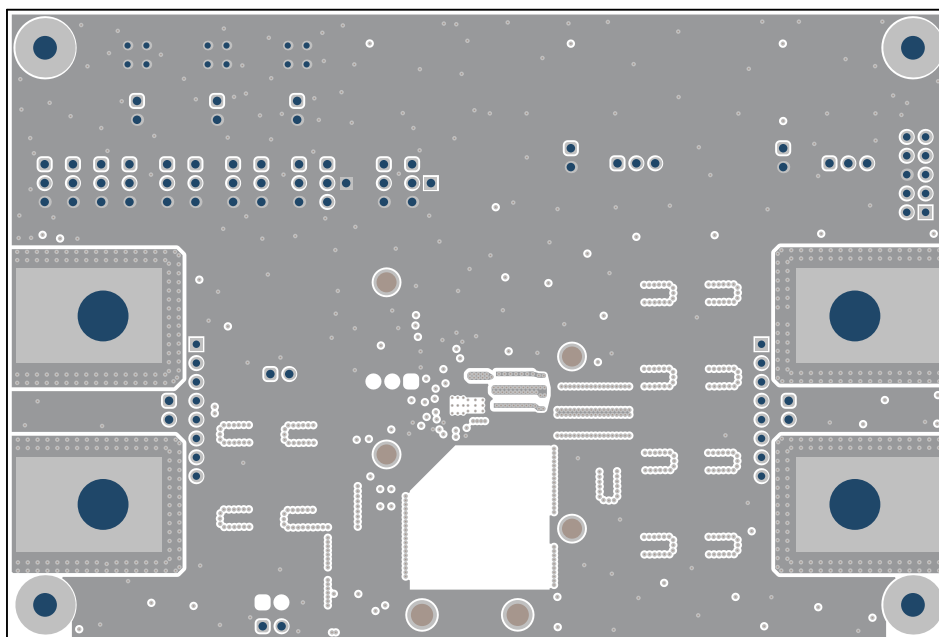


Figure 5-7. Signal Layer 3

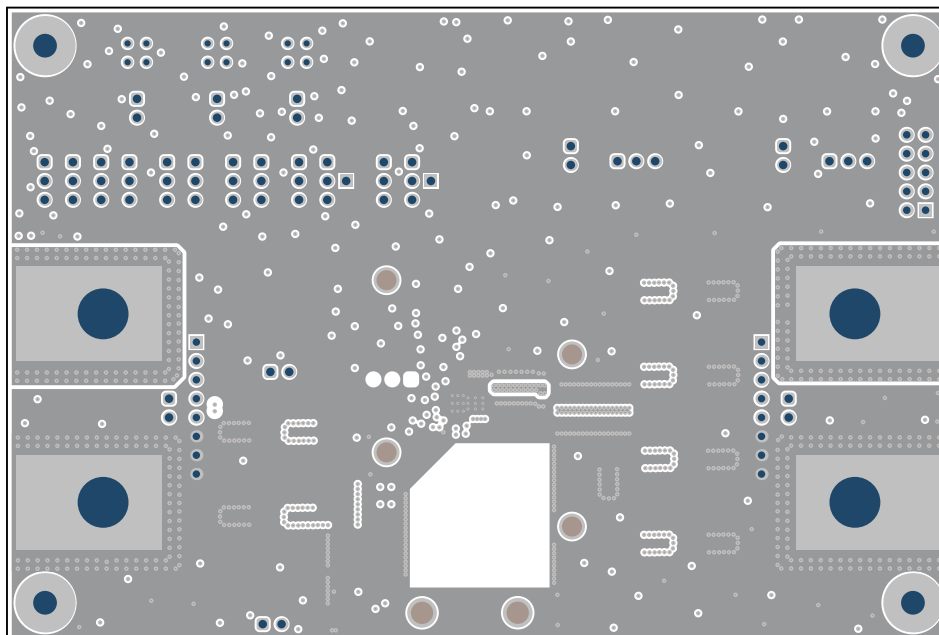


Figure 5-8. Signal Layer 4

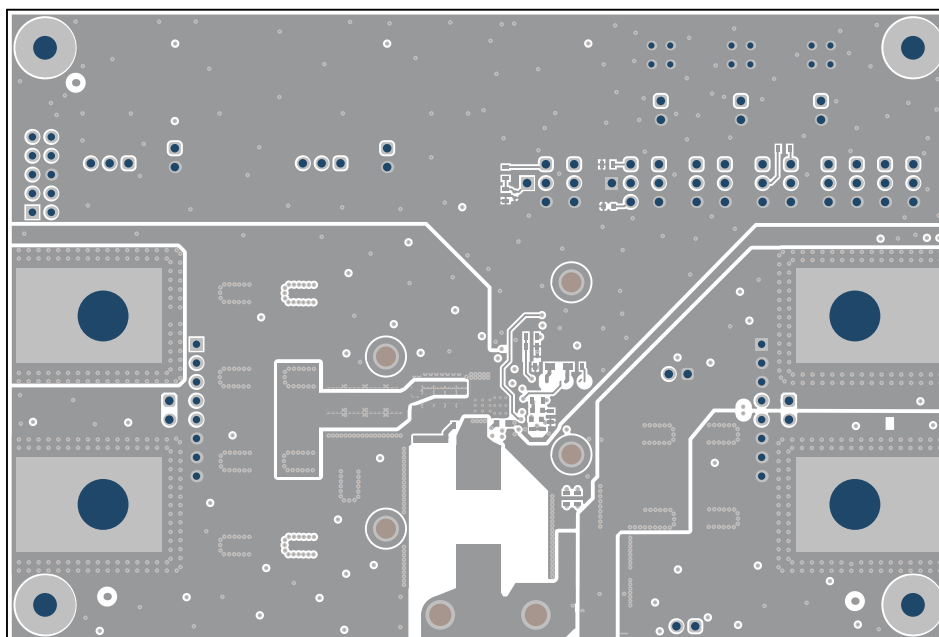


Figure 5-9. Bottom Layer

5.3 Bill of Materials

Table 5-1 details the EVM bill of materials.

Table 5-1. Bill of Materials

Designator	Quantity	Value	PartNumber	Manufacturer	Description
!PCB1	1		SR088	Any	Printed Circuit Board
C1	1	1 μ F	GCM188D71H105KE36J	Murata	1 μ F $\pm$ 10% 50V Ceramic Capacitor X7T 0603 (1608 Metric)
C2, C3, C18, C19, C21, C22, C23, C24, C25, C48, C49, C51	12	100nF	GRM155R62A104ME14D	Murata	Chip Multilayer Ceramic Capacitors for General Purpose, 0402, 0.10 μ F, X5R, 15%, 20%, 100V
C4	1	4.7 μ F	GRM155R60J475ME87D	MuRata	CAP, CERM, 4.7 μ F, 6.3V, +/- 20%, X5R, 0402
C5	1	100pF	CGA2B2C0G1H101J050BA	TDK	CAP, CERM, 100pF, 50V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402
C6, C50	2	330nF	GRT188R71C334KE01D	Murata	Multi-Layer Ceramic Capacitor 330nF 16V X7R $\pm$ 10% 0603 Paper T/R
C8	1	47pF	C0603C470J1GACAUTO	Kemet	CAP, CERM, 47 pF, 100 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603
C9	1	15nF	GCD188R71H153KA01D	Murata	Chip Multilayer Ceramic Capacitors for Automotive, 0603, 15000pF, X7R, 15%, 10%, 50V, Grade 1
C10	1	470pF	GRM1555C1H471JA01D	MuRata	CAP, CERM, 470 pF, 50 V, +/- 5%, C0G/NP0, 0402
C11, C12, C13, C14, C15, C36, C37, C38, C39, C40, C41, C42, C43	13		GRM32EC72A106KE05L	Murata	10 μ F $\pm$ 10% 100V Ceramic Capacitor X7S 1210 (3225 Metric)
C16, C17	2	220 μ F	EEHZU1H221P	Panasonic	Aluminum Hybrid Polymer Capacitors 220 μ F 20% 50V Life 4000Hours AEC-Q200 RADIAL SMT
C20	1	6800pF	GRM1885C1H682JA01D	MuRata	CAP, CERM, 6800 pF, 50 V, +/- 5%, C0G/NP0, 0603
C26, C27, C28, C29, C30, C31, C32, C33, C34, C35	10	2.2 μ F	GRM21BD72A225ME01K	Murata	Chip Multilayer Ceramic Capacitor for General Purpose 2.2 μ F $\pm$ 20% 100V X7T SMD 0805

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	PartNumber	Manufacturer	Description
C44, C45, C46, C47	4	150μF	EEHZU1J151P	Panasonic	Aluminum Hybrid Polymer Capacitors 150uF 20% 63V Life 4000Hours AEC-Q200 RADIAL SMT
FID1, FID2, FID3, FID4, FID5, FID6	6		N/A	N/A	Fiducial mark. There is nothing to buy or mount.
H1, H2, H3, H4	4		NY PMS 440 0025 PH	B&F Fastener Supply	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead
J1	1		N2510-6002-RB	3M	Header (shrouded), 100mil, 5x2, High-Temperature, Gold, TH
J2, J3, J4, J5, J11, J12, J13, J14, JP2, JP3, JP4, JP5, JP6, JP7	14		61300311121	Würth Elektronik	Header, 2.54 mm, 3x1, Gold, TH
J6, J7, J8, J10, J15, J16, J17, J20, JP1	9		61300211121	Würth Elektronik	Header, 2.54 mm, 2x1, Gold, TH
J9, J19	2		PEC08SAAN	Sullins Connector Solutions	Header, 100mil, 8x1, Tin, TH
J21, J22, J23, J24	4		108-0740-001	Cinch Connectivity	Standard Banana Jack, Uninsulated, 15A
J25, J26, J27	3		MMCX-J-P-X-ST-MT1	Samtec	50 ohm MMCX Jack, TH
JP8, JP9	2		61300111121	Würth Elektronik	Header, 2.54 mm, 1x1, Gold, TH
L1	1	3.3uH	XGL1712-332MED	Coilcraft	Inductor, Shielded Composite Core, 3.3uH, 30.3A, 0.0016 ohm, SMD
R1, R2	2	4m	KRL2012E-M-R004-F-T5	Susumu	4 mOhms ±1% 1W Chip Resistor Wide 0805 (2012 Metric), 0508 Automotive AEC-Q200, Current Sense Metal Foil
R5, R6	2	0	ERJ-3GEY0R00V	Panasonic	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603
R7	1	78.7k	CRCW060378K7FKEA	Vishay-Dale	RES, 78.7 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R8	1	16.0k	RC0603FR-0716KL	Yageo	RES, 16.0 k, 1%, 0.1 W, 0603
R9, R13	2	20.0k	CRCW060320K0FKEA	Vishay-Dale	RES, 20.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R10	1	10	CRCW121810R0FKEK	Vishay-Dale	RES, 10.0, 1%, 1 W, AEC-Q200 Grade 0, 1218
R11, R18	2	40.2k	CRCW060340K2FKEA	Vishay-Dale	RES, 40.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	PartNumber	Manufacturer	Description
R12	1	100k	CRCW0603100KFKEA	Vishay-Dale	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R14, R21	2	75.0k	CRCW060375K0FKEA	Vishay-Dale	RES, 75.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R15	1	39.0k	RC0603FR-0739KL	Yageo	RES, 39.0 k, 1%, 0.1 W, 0603
R16, R37, R53	3	24.9k	CRCW060324K9FKEA	Vishay-Dale	RES, 24.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R17	1	31.6k	CRCW060331K6FKEA	Vishay-Dale	RES, 31.6 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R19	1	48.7k	CRCW060348K7FKEA	Vishay-Dale	RES, 48.7 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R20	1	61.9k	CRCW060361K9FKEA	Vishay-Dale	RES, 61.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R22	1	90.9k	CRCW060390K9FKEA	Vishay-Dale	RES, 90.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R23	1	110k	CRCW0603110KFKEA	Vishay-Dale	RES, 110 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R24, R40, R56, R57, R58, R59	6	0	RMCF0603ZT0R00	Stackpole Electronics Inc	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R25, R41	2	511	CRCW0603511RFKEA	Vishay-Dale	RES, 511, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R26, R42	2	1.30k	CRCW06031K30FKEA	Vishay-Dale	RES, 1.30 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R27, R43	2	1.87k	CRCW06031K87FKEA	Vishay-Dale	RES, 1.87 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R28, R44	2	2.74k	CRCW06032K74FKEA	Vishay-Dale	RES, 2.74 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R29, R45	2	3.83k	CRCW06033K83FKEA	Vishay-Dale	RES, 3.83 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R30, R46	2	5.11k	CRCW06035K11FKEA	Vishay-Dale	RES, 5.11 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R31, R47	2	6.49k	CRCW06036K49FKEA	Vishay-Dale	RES, 6.49 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R32, R48	2	8.25k	CRCW06038K25FKEA	Vishay-Dale	RES, 8.25 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R33, R49	2	10.5k	CRCW060310K5FKEA	Vishay-Dale	RES, 10.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R34, R50	2	13.3k	CRCW060313K3FKEA	Vishay-Dale	RES, 13.3 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	PartNumber	Manufacturer	Description
R35, R51	2	16.2k	CRCW060316K2FKEA	Vishay-Dale	RES, 16.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R36, R52	2	20.5k	CRCW060320K5FKEA	Vishay-Dale	RES, 20.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R38, R54	2	30.1k	CRCW060330K1FKEA	Vishay-Dale	RES, 30.1 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R39, R55	2	36.5k	CRCW060336K5FKEA	Vishay-Dale	RES, 36.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
S1, S2, S3, S4, S5	5		218-8LPST	CTS Electrocomponents	Switch, SPST, 8 Pos, 25mA, 24VDC, SMD
SH-JP1, SH-JP2, SH-JP3, SH-JP4, SH-JP5, SH-JP6, SH-JP7	7	1x2	SPC02SYAN	Sullins Connector Solutions	Shunt, 100mil, Flash Gold, Black
T1, T2, T3, T4	4		CXS70-14-C	Panduit	Terminal 70A Lug
U1	1		LMG5126	Used in BOM report	
C7	0	47pF	C0603C470J1GACAUTO	Kemet	CAP, CERM, 47 pF, 100 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603
J18	0		61300211121	Würth Elektronik	Header, 2.54 mm, 2x1, Gold, TH
JP10	0		61300311121	Würth Elektronik	Header, 2.54 mm, 3x1, Gold, TH
R3, R4	0	0.003	KRL6432E-M-R003-F-T1	Susumu Co Ltd	RES, 0.003, 1%, 3 W, AEC-Q200 Grade 0, 2512 WIDE
TP1	0		RCU-0C	TE Connectivity	PC Test Point, SMT

6 Additional Information

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