Application Report
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Seismic Sensor Demonstration Using an ADS1255 and TMS320VC5510A DSP

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ABSTRACT

A prototype system for seismic sensing for such applications as oil exploration, earthquake detection, and acoustic monitoring is described. The system uses a delta-sigma converter and low-power DSP. Measured system performance met the requirements for such systems.

Oil exploration, earthquake detection, and acoustic monitoring of drilling operations are all applications that use seismic sensing capabilities. Such applications require signal conditioning of the input of a geophone, hydrophone, or other acoustic sensor, demanding effective amplification, filtering, and digitization of the target acoustic signal.

An ideal seismic sensing system has the characteristics of good signal-to-noise ratio, low power consumption (to allow for remote operation), programmable signal filtering to accommodate several applications, a variable sampling rate, and cost-effectiveness. An additional goal is to make the system easy to prototype for fast evaluation.

The system architecture that was selected is shown in Figure 1 and consists of an excellent front-end processor followed by a programmable, powerful, low-power filter engine.

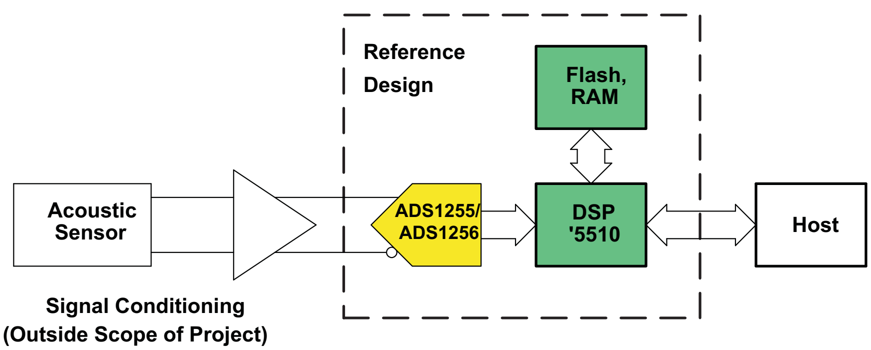

Figure 1. Seismic System Architecture

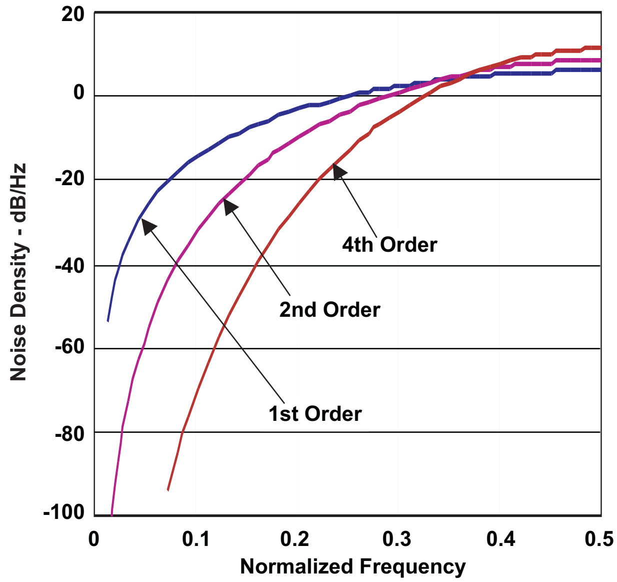

Figure 2. ADS1255 Modulator Noise

The system input is an acoustic sensor that drives a signal conditioning circuit which in turn drives an A/D converter. The ADS1255 24-bit sigma-delta converter was chosen because it contains a programmable gain front-end stage that can replace the signal conditioning circuit. Further, the sigma-delta ADC's fourth-order oversampling architecture (Figure 2) provides signal-to-noise gain by moving the quantization noise up in frequency, where it is filtered out. This is a performance level that cannot be met by pipeline or successive-approximation architectures.

Seismic sensing applications require a processor that is fast, efficient, requires little logic glue, and is easy to implement. The TMS320VC5510A digital signal processor provides the low-power operation desired. The DSP has a 40-bit accumulator that makes the implementation of the pseudo-floating point operation used for the filtering easy – filter operations could be accumulated in 40 bits of resolution and truncated to 32 bits at the end of the filter. The DSP library provides for an efficient 32-bit x 32-bit multiply, making the filter operations efficient. Finally, the onboard McBSP interface allows interfacing to the ADC with minimal processor intervention.

The filtering architecture combined the fifth-order filter built into the ADS1255 with the flexible filter architecture of the DSP (Figure 3). The filter architecture allowed a variable rate output while providing a flat passband, sharp filter cutoff for noise reduction, >130-dB stopband rejection, and 50-Hz/60-Hz rejection.

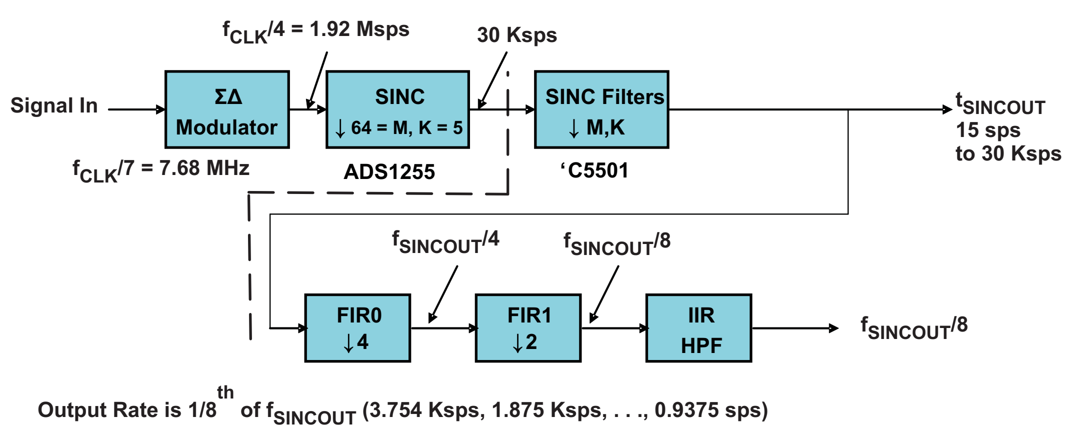

Figure 3. Filtering Architecture Block Diagram

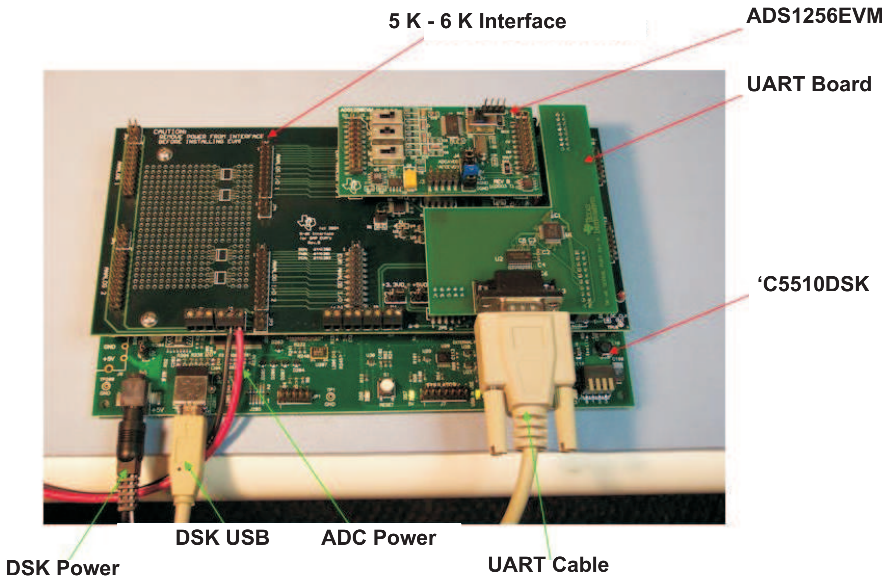

Figure 4. Seismic System Prototype Board

This solution can be built using evaluation boards that are readily available from Texas Instruments with the exception of the UART board (Figure 4). The system can attach to a host computer for complete system evaluation.

The measured results from the system showed performance that meets the needs of the application as Table 1 shows.

Table 1. Prototype System Performance

PARAMETER	MIN	TYP	MAX	UNIT
Sample Rate	0.9375		3750	Hz
SNR (3.75 ksps)		116		dB
SNR (117 sps)		131		dB

References

1. *TMS320VC5510/5510A Fixed Point DSP* data manual (SPRS076)
2. *ADS1255/ADS1256 Very Low Noise 24-Bit ADC* data sheet (SBAS288)
3. *TMS320VC5501/5502/5503/5507/5509/5510 DSP (McBSP) Reference Guide* (SPRU592)
4. TMS320VC5510 DSP Starter Kit
5. 5-6K Interface Evaluation Module
6. ADS1256 Evaluation Module

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