TMS320C24x
General Purpose Timer 1
Symmetric Mode

Application Report
SPRA368

TEXAS INSTRUMENTS

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Overview

There are three General Purpose (GP) Timers in the Event Manager of the ℃240. There timers can be used as independant time bases in applications such as:

- generation of sampling period in a control system,
- providing time base for quadrature encoder sensor signal processing in a motor control system,
- providing time base for the operation of Full and Simple Compare Units and associated PWM circuits to generate PWM outputs in a motor control system.

This application report present one application of the GP Timer: Time base and PWM generation using GP Timer One in asymmetric mode.

Index

1. Possibilities of GP Timer 1 in Symmetric Mode _____ 4

2. Description : Event Manager Programming _____ 6

2.1 Timer Composition _____ 6

2.2 Preparation Phase for Timer Configuration _____ 6

2.3 Calculation for the Time Slots in the Symmetric Case _____ 7

2.4 Example _____ 7

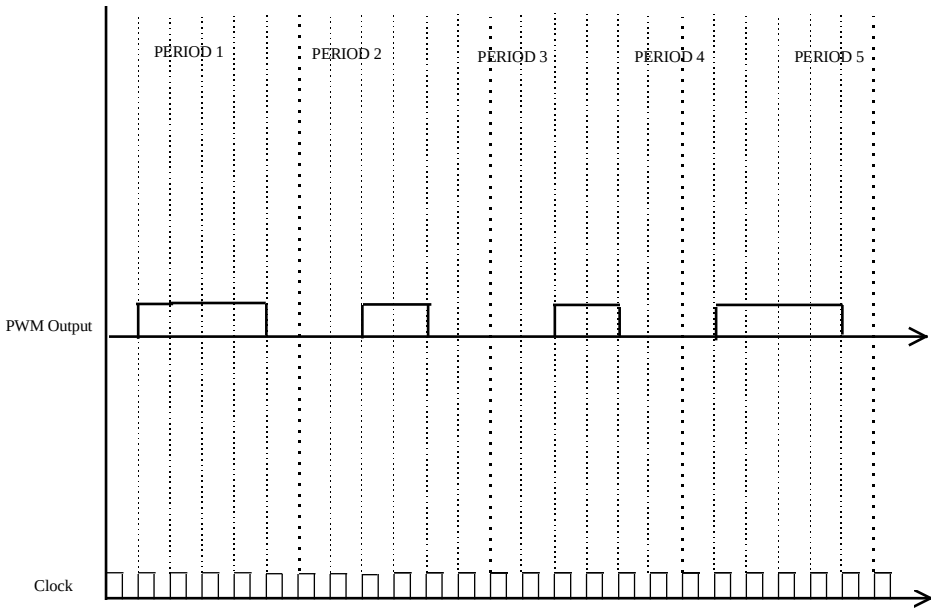
2.5 Modification of the Active Width during Running _____ 10

Note:
General Purpose Timer 2 and General Purpose Timer 3 have same functionalities than Timer 1 except for Time Base generation for Full or Simple Compare.

1. Possibilities of GP Timer 1 in Symmetric Mode

General Purpose Timer 1 in symmetric mode can be used:

- To generate one **symmetrical PWM** on the GP Timer 1 output with following features :
  - this PWM connected to Time Base One is Time Base dependent (Counter and Period) with the three pairs PWM (Full Compare) connected exclusively to Time Base One.
  - this PWM could be totally independent with the three PWM (Simple Compare) if these three PWM are based on Time Base Two.



- To generate a time base for the Compare and/or the Simple compare module.

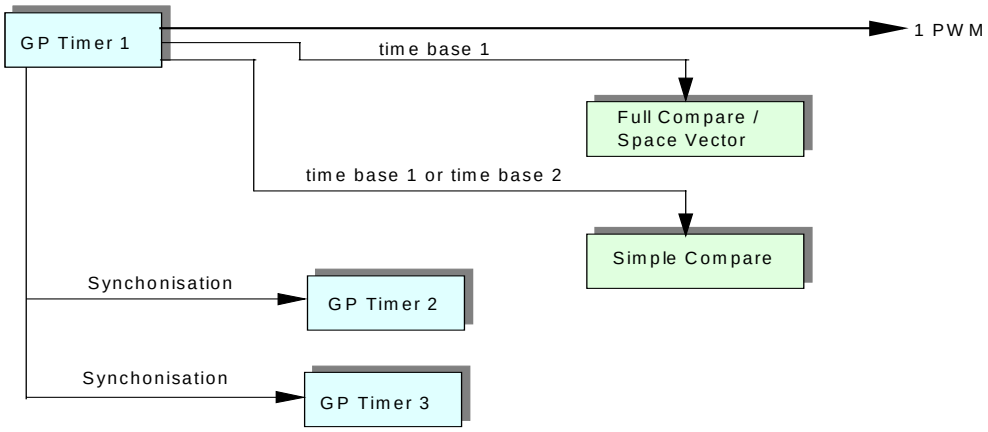
Three pairs PWM (Full Compare) are exclusively based on the Time Base One.
Three PWM (Simple Compare) can be connected to the Time Base One or Time Base Two.

- To generate a Time Base for the Space Vector modulation module.

- To generate a Time Base for GP Timer 2 and GP Timer 3.

Time Base Two or Three can be independently or both synchronous to Time Base One.

Time Base One

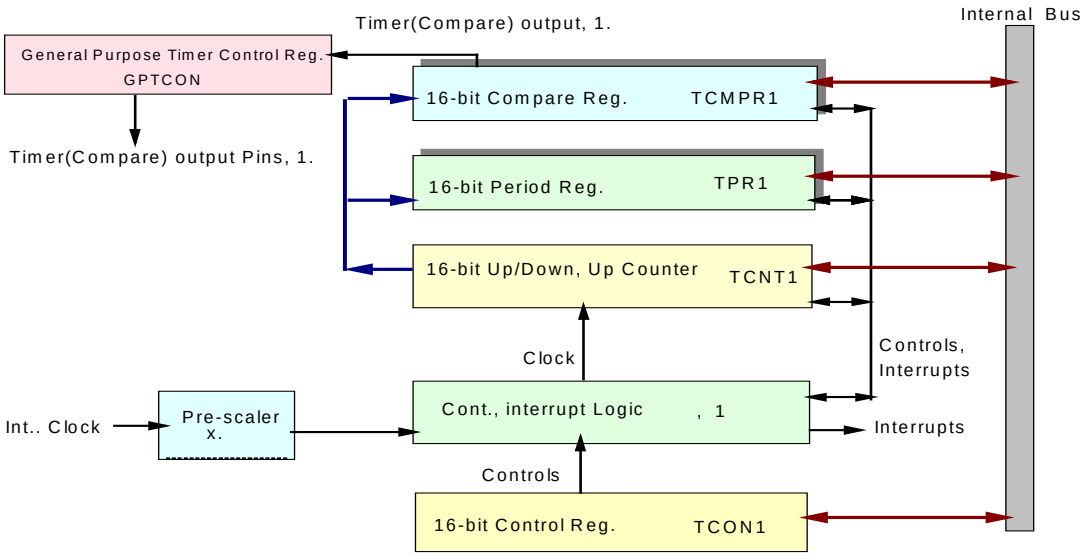


- To generate a Time Base with Period modification on the fly.

- To generate a Time Base for QEP, Capture, ...

2. Description : Event Manager Programming

2.1 Timer Composition:



2.2 Preparation Phase to Configure this Timer

The preparation phase for timer configuration is to:

- write GPTCON to determine action on GP Timer 1 compare output pin (active low, active high, forced low, forced high)
- write TPR1 : Timer Period register.
- write TCMPR1 : Compare Period register.
- write TCNT1 : Counter Period register.
- write TCON1 with bit 6=0b (timer disable)
  : Control register to program Count Mode Selection, Clock Pre-scaler, Clock Source, compare reload condition, enable compare operation .
- write TCON1 with bit 6=1b to start the timer.
  : Control register to enable the Timer 1

2.3 Calculation for the Time Slots in the Symmetric Case

- PWM cycle time: T_{PWM}=2*TPER timer counts. TPER is the value programmed into the period register for the PWM time base counter.
- ACTIVE pulse width: Ton=(TPER-CMPRup+TPER-CMPRdn) timer counts. CMPRup is the value programmed into the compare register during the UP count half of the PWM cycle. Likewise, CMPRdn is the value programmed into the compare register during the DOWN count half of the PWM cycle. If these are one and the same (CMPR), the equation will reduce to T_{ON}=2*(TPER-CMPR). This equation is only true for CMPR values in the range 0 to TPER-1. If CMPR is TPER, the output will remain in its INACTIVE state.
- INACTIVE time: T_{OFF}=CMPRup+CMPRdn timer counts. If these two compare triggers are the same, the equation reduces to T_{OFF}=2*CMPR. The off times will be at the start and the end of the PWM cycle.

2.4 Example:

Timer 1B is programmed to generate an up/down count with a symmetrical PWM.

- Free run, no emulation mode.
- Timer count mode Continuous Up/Down-Count Mode.
- No timer input pres-caler and internal clock.
- Reload the shadow compare register when counter=0.
- PWM output Active Low.

- Period: 5 * 2 * 50ns.
- Compare transition after 3 * 50ns.

Register programming

```
  GPTCON        =  042h
                Bit 1&2         : 10b  , State of GP Timer 1
                                       compare output active High.
                Bit 6           : 1b   , All 3 GP Timer outputs
                                       are enabled (no High
                                       Impedance State).
  TPR1          =  5h
  TCMPR1        =  3h
  TCNT1         =  0h
  TCON1 (1st)   =  a802h
                Bit 1           : 1b   , Enable timer compare
                                       operation.
                Bit 3&2         : 00b  , Compare Register reload
                                       when counter is zero.
                Bit 5&4         : 00b  , Internal Clock source
                                       selected.
                Bit 6           : 0b   , Timer 1 Disabled and
                                       prescaler reset.
                Bit 13,12&11    : 101b , Continuous-Up/Down Count
                                       Mode.
                Bit 15&14       : 10b  , GP timer not affected by
                                       emulation suspend.
  TCON1 (2nd) = a842h
                Bit 6           : 1b   , Timer 1 is enabled.
```

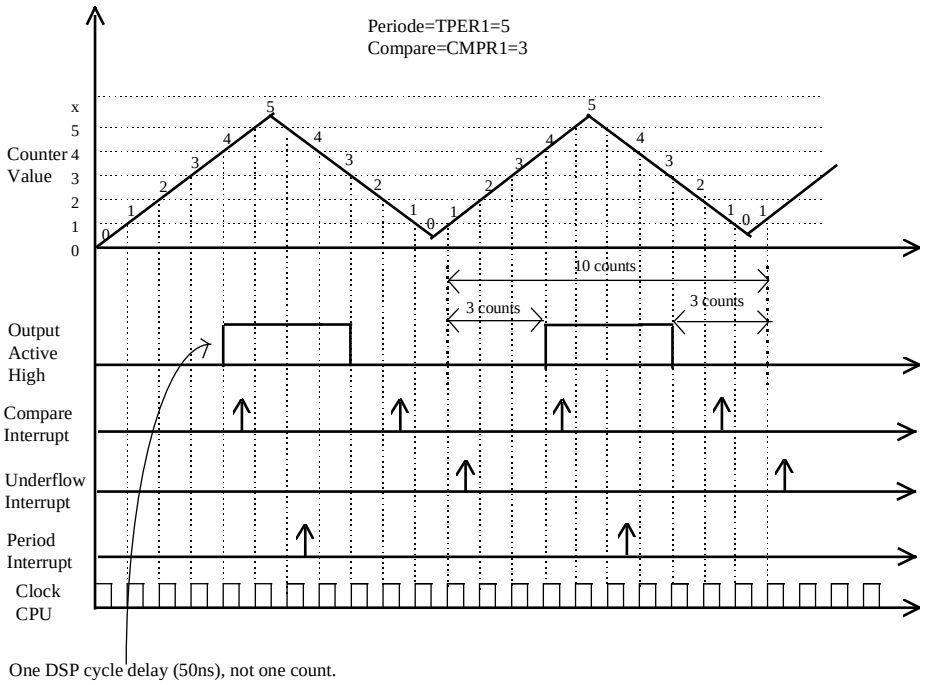
Initialization Assembly code:

```
        ;Note : GP timer registers are memory mapped.

  GPTCON .set   7400h          ;General Timer Controls
  TCNT1  .set   7401h          ;T1 Counter Register
  TCMPR1 .set   7402h          ;T1 Compare Register
  TPR1   .set   7403h          ;T1 Period Register
  TCON1  .set   7404h          ;T1 Control Register

        LDP     #232
        SPLK    #42h,GPTCON
        SPLK    #5h,TPR1
        SPLK    #3h,TCMPR1
        SPLK    #0h,TCNT1
        SPLK    #0a802h,TCON1
```

Result of this example:



Note:
The first period of a continuous up/down count is 1 DSP cycle longer and is not totally symmetrical (see diagram above).

2.5 Modification of the Active Width during Running

When a new compare value in the CMPR1 register is written, the new value is loaded in the timer register and is active at the end of the period, when TCNT1=0 (for this base configuration).

Example:
CMPR1 switches from 3 to 4 during the second period, the result will be: