Using Boundary Scan on the TMS320VC5471/VC5470 DSPs

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ABSTRACT

The Texas Instruments (TI) TMS320VC5471 and TMS320VC5470 DSPs (hereafter referred to as VC547x) are dual-core processor devices implementing standard IEEE 1149.1† boundary scan capability. This application report contains a description of the VC547x boundary scan implementation and information about how to use it with other boundary scan tools and devices.

The material covered in this application report assumes the reader is familiar with the boundary scan concepts defined by IEEE Standard 1149.1. An overview of these concepts is presented in the *IEEE Std 1149.1 (JTAG) Testability Primer* (literature number SSYA002). For detailed information on the operation and requirement for boundary scan, refer to the IEEE standard itself. Copies of the standard are available from IEEE at 1-800-678-IEEE.

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† IEEE Standard 1149.1-1990 Standard Test-Access Port and Boundary Scan Architecture

1 VC547x Boundary Scan Implementation

1.1 VC547x Silicon Revision Requirements

The VC547x boundary scan implementation described in this document applies to all silicon revisions.

1.2 Observe and Control Capability

The VC547x implements standard observe and control capability with respect to the IEEE Standard 1149.1. This means pins with input functions (input or I/O pins) have observe capability and pins with output functions (outputs and I/O pins) have control capability.

1.3 VC547x Hardware Requirements for Boundary Scan Test

Boundary scan test requires control of the five test-access port signals (TMS, TCK, TDI, TDO and TRST) as described in IEEE standard 1149.1. Two additional signals, EMU0 and EMU1/OFF, are used by TI DSPs to provide emulation debug capability through the JTAG test-access port. Also, TI uses these signals for scan-based factory tests.

During boundary scan tests, EMU0 and EMU1/OFF must be held high while TRST is transitioned from low to high. This operation sets the correct internal test mode for boundary scan test to be performed. EMU0 and EMU1/OFF should be pulled high through 4.7-kΩ pullup resistors on each pin. The pullup resistors are connected to the DV_{DD} power supply for the VC547x.

Boundary scan automatic test pattern generation (ATPG) tools should be configured to cycle TRST prior to beginning boundary scan tests to ensure that the device is in the proper test mode.

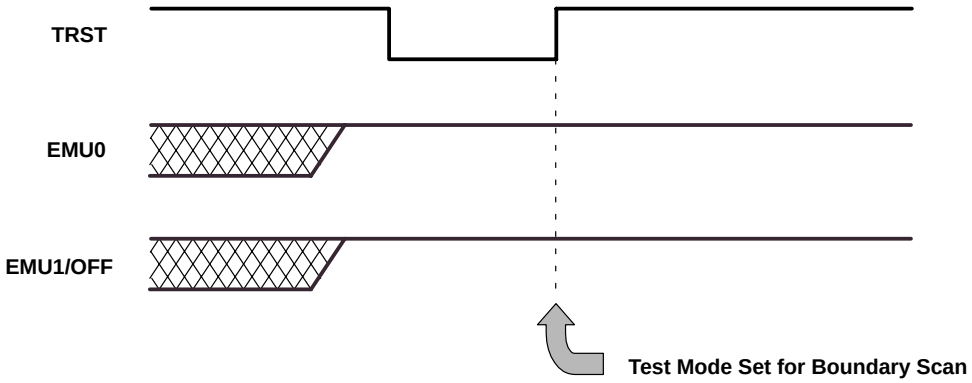

Figure 1. Initialization for Boundary Scan Test Mode Using TRST, EMU0 and EMU1/OFF

1.4 VC547x Boundary Scan Pin Coverage

All digital pins on the VC547x have boundary scan cells for test with the following exceptions. The device pins not testable through boundary scan are shown in Table 1.

Table 1. Device Pins Not Testable Through Boundary Scan

Pin	Pin Function
DV_{DD}, CV_{DD}, Vss	Power supply pins
TMS, TCK, TDI, TDO, TRST	JTAG test access pins
EMU0, EMU1/OFF	Emulation test pins

1.5 VC547x Boundary Scan Description Language (BSDL) Implementation

A representation of the internal structure of the VC547x with respect to boundary scan is shown in Figure 2. The VC547x is composed of two internal processor [general-purpose processor (GPP) and digital signal processor (DSP)] subsystems and internal ASIC logic. Each of the subsystems and the ASIC logic have independent TAP controllers to provide boundary scan test and emulation capability. The device signals TMS, TCK, and TRST are connected to each TAP in parallel. The device TDI is connected to the GPP ARM™ subsystem. The internal equivalent of TDO for the GPP subsystem is connected to the internal TDI for the DSP subsystem. The internal equivalent of TDO for the DSP subsystem is connected to the internal TDI for the ASIC TAP. The output of the chain from the ASIC TAP is connected to the device TDO. To a boundary scan test system, this structure is equivalent to treating the subsystems as independent devices.

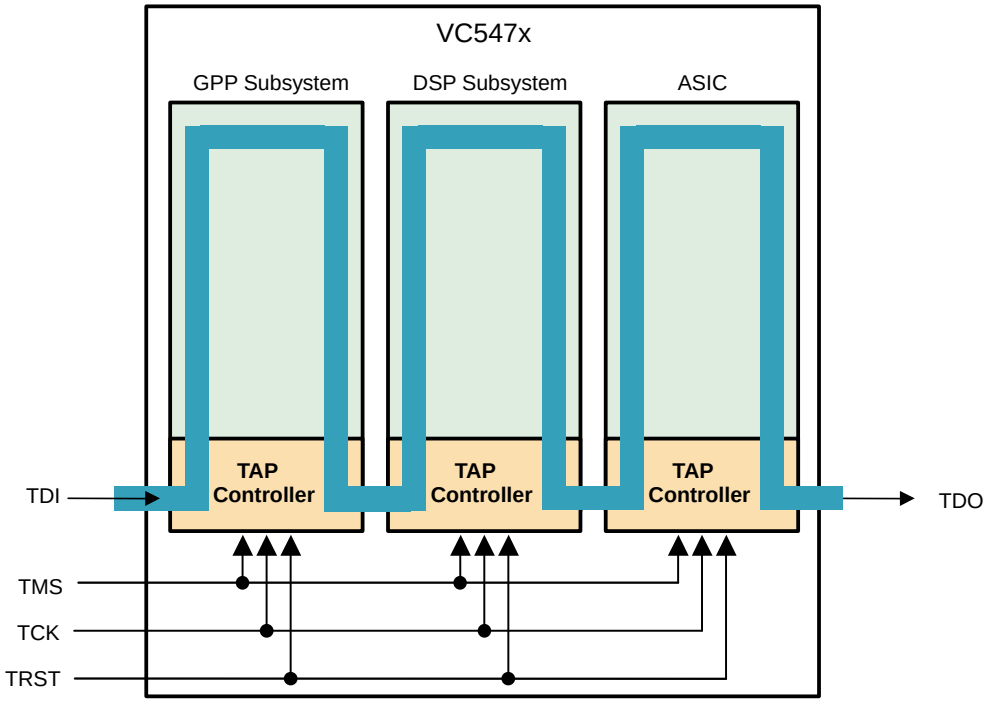

Figure 2. Boundary Scan Structure of the VC547x

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Although ATPG tools vary in how they describe system-level structure, all tools provide a method to describe the order of the devices in the scan chain. The BSDL description of the VC547x is implemented as three BSDL files, one for each subsystem and one for the ASIC TAP. These three boundary scan objects must always be used together and described to the ATPG tools in the proper order. The ASIC TAP *must* be described as the subsystem closest to TDO, with the DSP subsystem in the middle, and the GPP subsystem closest to TDI. If the order is reversed, tests generated by the ATPG tools will be incorrect.

The connection between the scan chains of the GPP and DSP subsystems is internal to the device. Similarly, the DSP subsystem and ASIC are internally connected. Some ATPG tools may issue a warning or error indicating that the TDO-TDI connections between the subsystems and ASIC objects are not present. In this case, the device can be modeled as a multichip module using the hierarchical capabilities of the ATPG tool. Many boundary scan systems have hierarchical scan chain descriptions where, for example, a plug-in module may be described as a sub-chain to the main boundary scan chain. The model for the sub-chain is generated separately, and then referenced in the description of the main boundary scan chain. The same approach can be used to model the VC547x as a single object if necessary. The device can be modeled as a sub-chain composed of a GPP subsystem, a DSP subsystem, and an ASIC, as shown in Figure 3. Then, the VC547x can be referenced in the main description of the scan chain as a single device “module”. Since the methods to describe hierarchical and modular systems are tool-dependent, a single method cannot be described here. It will be necessary to contact the ATPG tool vendor regarding how this procedure is done on their particular tool. Given the BSDL files for each TAP and the information in this document, a model can be generated.

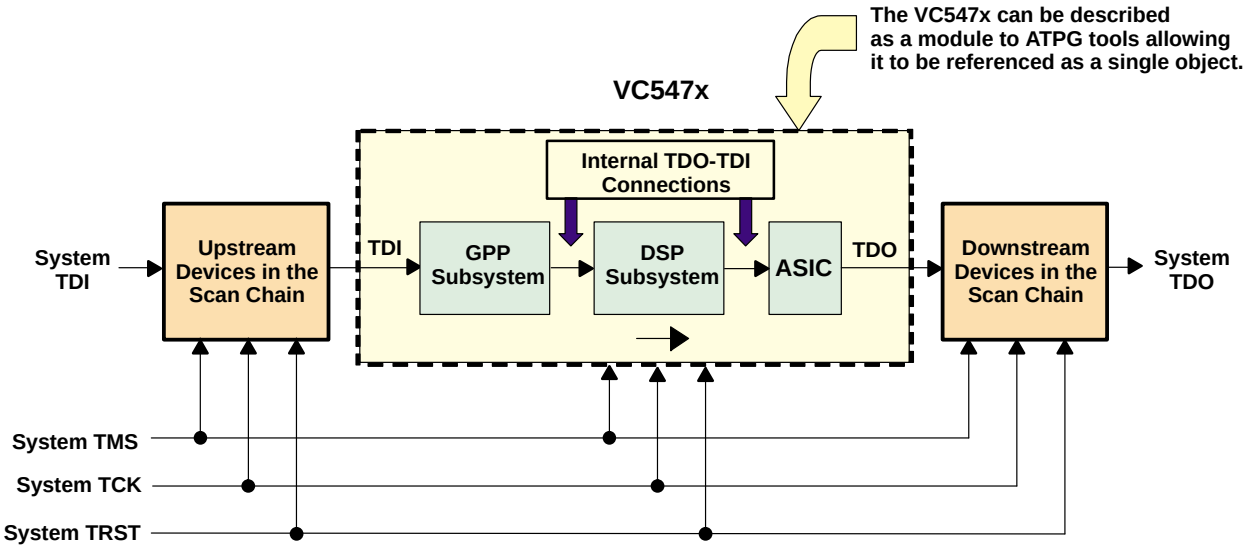

Figure 3. The VC547x Subsystems Modeled as a “Module” in the Scan Chain

Separate BSDL files are provided for the GPP subsystem, the DSP subsystem, and the ASIC TAP. Current VC547x BSDL files and information are available on the web at:

http://www–k.ext.ti.com/sc/technical_support/tools/dsp/ftp/c54x.htm

The ASIC TAP has the ability to capture and control pins on the device during boundary scan test. The ARM and DSP subsystems do not control device pins for the purpose of boundary scan testing and are bypassed. See Section 1.6, VC547x Boundary Scan Instruction Implementation, and the BSDL files for more details.

1.6 VC547x Boundary Scan Instruction Implementation

The VC547x implements the following instructions for boundary scan:

- SAMPLE/PRELOAD
- EXTEST
- BYPASS
- HIGHZ

IEEE standard 1149.1 specifies that the SAMPLE/PRELOAD instruction samples inputs and preloads but does not drive outputs. During the SAMPLE/PRELOAD instruction, the device pins maintain their normal functional behavior. The behavior of the VC547x during execution of this instruction is consistent with the specification in the standard. The ASIC TAP supports this instruction.

IEEE standard 1149.1 specifies that the EXTEST instruction samples inputs, and loads and drives outputs. The behavior of the VC547x during execution of this instruction is consistent with the specification in the standard. The ASIC TAP supports this instruction.

IEEE standard 1149.1 specifies that the BYPASS instruction maps a 1-bit bypass register between TDI and TDO (to minimize the chain length when a device is not being tested) and the device pins operate in their normal functional (non-test) mode. The behavior of the VC547x during execution of this instruction is consistent with the specification in the standard. Note that the VC547x has one bypass bit for each subsystem (since there is a TAP controller for each subsystem) for a total of three bits between the device TDI and TDO. This behavior is accounted for (and maintains compliance with IEEE standard 1149.1) through the use of separate BSDL files for each subsystem. The ASIC TAP and both subsystem TAPs support this instruction

IEEE standard 1149.1 specifies that the HIGHZ instruction places the bypass register in the scan chain and causes all output pins (either dedicated outputs or I/O pins) to enter a high-impedance state. The behavior of the VC547x during execution of this instruction is consistent with the specification in the standard. The ASIC TAP supports this instruction.

None of the other boundary scan instructions specified as optional in IEEE standard 1149.1 are implemented on the VC547x.

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