EVM Application #4

Generating a PWM Signal Modulated by an Analog Input Using the TMS320F240 EVM

APPLICATION REPORT: SPRA413

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TEXAS INSTRUMENTS

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Abstract

This EVM application converts an input value with the analog-to-digital converter (ADC) module of the Texas Instruments (TI™) TMS320F240 Evaluation Module (EVM) and outputs a pulse width modulated (PWM) signal corresponding to the digital conversion of the analog input.

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Overview

This application converts an input value with the analog-to-digital converter (ADC) module of the TI TMS320F240 EVM and outputs a pulse width modulated (PWM) signal corresponding to the digital conversion of the analog input. In other words, the pulse width of the PWM signal will be proportional to the input value and represents an *equivalent* analog output signal. The PWM signal will be created asymmetrically. This application is implemented using C2xx Assembly code. The algorithm described in this application report was implemented using the TMS320F240 EVM.

Module(s) Used

- ❑ 10 bit Analog-to-Digital Converter
- ❑ Event Manager Module
- ❑ General Purpose Timer 1

Input

ADCIN0

Output

T1PWM / T1CMP

Background and Methodology

This application uses the ADC and the Event Manager Module to convert an input signal (with the ADC) and output a proportional pulse width signal (with a General Purpose Timer of the Event Manager). The setup of this program is similar to the setup for Application #2 (PWM1.ASM) except instead of going to a look-up table to find the next value for the compare register, the program uses the value that is located in the ADCFIFO register.

The initial setup of the PWM signal is similar to the setup that was done for Application #1 and #2. The PLL Module, Digital I/O Port, and the Event Manager Module need to be set up properly to set up the PWM signal. Similar to the Timer Module of the Event Manager Module, the ADC also shares some of its pins with the pins of the I/O Port. As a result, in the setup of the Digital I/O Port, the Event Manager Module and the ADC need to be configured so that their respective pins are TxPWM/TxCMP outputs and ADCINx inputs, rather than generic I/O pins.

Similar to Application #2 (PWM1.ASM), this application uses the General Purpose Timer's period register to generate an interrupt that updates the compare register.

Analog-to-Digital Converter

Once the Event Manager registers are set up to generate a PWM signal, then the ADC needs to be set up. Since the ADC has a FIFO register that can store two converted values at a time, the ADC can be set up to convert continuously. By converting continuously, the ADC's values will not be dependent on the interrupt service routine to be restarted. Because the ADC will be converting continuously, the value that is in the ADCFIFO register will be a recent conversion.

Because the ADC has a resolution of 10 bits and the registers of the timers are 16 bits, scaling has to be done so that the resulting pulse width can have a duty cycle of 0 to 100 percent of the PWM period. The ADC converts the input values and places them into the ADCFIFO register. The ADCFIFO register is 16 bits wide, yet the ADC only has a 10 bit resolution. As a result the converted value’s most significant bit occupies the most significant bit of the register, thereby always leaving the 6 least significant bits of the register filled with zeros.

If the values in the ADCFIFO register were used without modification, the pulse width would have a discontinuity as the input value went from 1/1024 of V_{ref} to 0V. This discontinuity would result because the compare register would switch from 40h to 00h during the transition from 1/1024 of V_{ref} to 0V. To avoid this discontinuity, the ADCFIFO register result is shifted to the right so that the least significant bit, which resided at bit 6, now resides at bit 0. By shifting ADCFIFO, the maximum values go from FFC0h to 3FFh, and the minimum value (above 0) goes from 40h to 1h. By shifting the ADCFIFO results, the period register can be set to a 10 bit maximum of 3FFh. Because the period register is set to the maximum value 3FFh, with the CPUCLK at 20MHz, the resulting PWM frequency will be 19.5kHz.

Like the previous applications, this application is interrupt driven, and once the registers are set up, the program can be ended. The PWM output continues to run because of the interrupt structure, but when the program is halted, the PWM signal stops.

```
;******************************************************************
; File Name:         adc0.asm
; Originator:        Digital Control systems Apps group - Houston
; Target System:     'C24x Evaluation Board
;
; Description:    Uses the ADC and outputs the conversion to the
;                 compare register of the Event Manager to modify
;                 duty cycle of a PWM signal in proportion to the
;                 input analog value.

; Last Updated:    20 June 1997
;
; ************************************************************
                    .include f240regs.h
; ----------------------------------------------------------
; I/O Mapped EVM Registers
; ----------------------------------------------------------
DAC0             .set  0000h ;Input data register for DAC0
DAC1             .set  0001h ;Input data register for DAC1
DAC2             .set  0002h ;Input data register for DAC2
DAC3             .set  0003h ;Input data register for DAC3
DACUPDATE        .set  0004h ;DAC Update Register
;-----------------------------------------------------------
; Variable Declarations for B2
;-----------------------------------------------------------
                 .bss  GPR0,1     ;General Purpose Register
                 .bss  DAC0VAL,1  ;DAC0 Channel Value
                 .bss  DAC1VAL,1  ;DAC0 Channel Value
                 .bss  DAC2VAL,1  ;DAC0 Channel Value
                 .bss  DAC3VAL,1  ;DAC0 Channel Value
;-----------------------------------------------------------
; Vector address declarations
;-----------------------------------------------------------
                 .sect ".vectors"
RSVECT           B     START      ; Reset Vector
INT1             B     PHANTOM    ; Interrupt Level 1
INT2             B     CHG_CMPR   ; Interrupt Level 2
INT3             B     PHANTOM    ; Interrupt Level 3
INT4             B     PHANTOM    ; Interrupt Level 4
INT5             B     PHANTOM    ; Interrupt Level 5
INT6             B     PHANTOM    ; Interrupt Level 6
RESERVED         B     PHANTOM    ; Reserved
SW_INT8          B     PHANTOM    ; User S/W Interrupt
SW_INT9          B     PHANTOM    ; User S/W Interrupt
SW_INT10         B     PHANTOM    ; User S/W Interrupt
SW_INT11         B     PHANTOM    ; User S/W Interrupt
SW_INT12         B     PHANTOM    ; User S/W Interrupt
SW_INT13         B     PHANTOM    ; User S/W Interrupt
SW_INT14         B     PHANTOM    ; User S/W Interrupt
SW_INT15         B     PHANTOM    ; User S/W Interrupt
SW_INT16         B     PHANTOM    ; User S/W Interrupt
TRAP             B     PHANTOM    ; Trap vector
```

```
NMINT            B     PHANTOM     ; Non-maskable Interrupt
EMU_TRAP         B     PHANTOM     ; Emulator Trap
SW_INT20         B     PHANTOM     ; User S/W Interrupt
SW_INT21         B     PHANTOM     ; User S/W Interrupt
SW_INT22         B     PHANTOM     ; User S/W Interrupt
SW_INT23         B     PHANTOM     ; User S/W Interrupt
;===========================================================
; M A I N   C O D E  - starts here
;===========================================================
                 .text
                 NOP
START:    SETC   INTM              ;Disable interrupts
                 SPLK  #0002h,IMR ;Mask all interrupts except INT2
                 LACC  IFR         ;Read Interrupt flags
                 SACL  IFR         ;Clear all interrupt flags

                 CLRC  SXM         ;Clear Sign Extension Mode
                 CLRC  OVM         ;Reset Overflow Mode
                 CLRC  CNF         ;Config Block B0 to Data mem
;------------------------------
; Set up PLL Module
;------------------------------
                 LDP   #00E0h
;The following line is necessary if a previous program set the PLL
;to a different setting than the settings which the application
;uses.  By disabling the PLL, the CKCR1 register can be modified so
;that the PLL can run at the new settings when it is re-enabled.
                 SPLK #0000000001000001b,CKCR0  ;CLKMD=PLL Disable
                                                ;SYSCLK=CPUCLK/2
;                        5432109876543210
                 SPLK  #0000000010111011b,CKCR1 ;CLKIN(OSC)=10MHz
                                                ;CPUCLK=20MHz

;CKCR1 - Clock Control Register 1
;   Bits 7-4     (1011)CKINF(3)-CKINF(0) - Crystal or Clock-In
                          Frequency
;                         Frequency = 10MHz
;   Bit 3        (1)   PLLDIV(2) - PLL divide by 2 bit
;                         Divide PLL input by 2
;   Bits 2-0     (011) PLLFB(2)-PLLFB(0) - PLL multiplication ratio
;                                     PLL Multiplication Ratio = 4

;                        5432109876543210
                 SPLK  #0000000011000011b,CKCR0 ;CLKMD=PLL Enable
                                                ;SYSCLK=CPUCLK/2

;CKCR0 - Clock Control Register 0
;   Bits 7-6     (11)  CLKMD(1),CLKMD(0) - Operational mode of Clock
                          ; Module PLL Enabled
                          ; Run on CLKIN on exiting low power mode
;   Bits 5-4     (00)  PLLOCK(1),PLLOCK(0) - PLL Status. READ ONLY
;   Bits 3-2     (00)  PLLPM(1),PLLPM(0) - Low Power Mode - LPM0
;   Bit 1        (0)   ACLKENA - 1MHz ACLK Enable
;                            ACLK Enabled
;   Bit 0        (1)   PLLPS - System Clock Prescale Value
;                            f(sysclk)=f(cpuclk)/2

;                       5432109876543210
                 SPLK  #0100000011000000b,SYSCR ;CLKOUT=CPUCLK

;SYSCR - System Control Register
;   Bit 15-14    (01)  RESET1,RESET0 - Software Reset Bits
;                                  No Action
;   Bits 13-8    (000000)      Reserved
;   Bit 7-6      (11)  CLKSRC1,CLKSRC0 - CLKOUT-Pin Source Select
;                                  CPUCLK: CPU clock output mode
;   Bit 5-0      (000000)      Reserved


                 SPLK  #006Fh, WDCR     ;Disable WD if VCCP=5V
                                        ;   (JP6 in pos. 2-3)
                    KICK_DOG            ;Reset Watchdog

;------------------------------
; Set up Digital I/O Port
;------------------------------
   LDP           #225           ;DP=225, Data Page to Configure OCRA
;                       5432109876543210
                 SPLK  #0011100000001111b,OCRA

;OCRA  - Output Control Register A
;   Bit 15       (0)   CRA.15 - IOPB7
;   Bit 14       (0)   CRA.14 - IOPB6
;   Bit 13       (1)   CRA.13 - T3PWM/T3CMP
;   Bit 12       (1)   CRA.12 - T2PWM/T2CMP
;   Bit 11       (1)   CRA.11 - T1PWM/T1CMP
;   Bit 10       (0)   CRA.10 - IOPB2
;   Bit 9        (0)   CRA.9 - IOPB1
;   Bit 8        (0)   CRA.8 - IOPB0
;   Bits 7-4     (0000)Reserved
;   Bit 3        (1)   CRA.3 - ADCIN8
;   Bit 2        (1)   CRA.2 - ADCIN9
;   Bit 1        (1)   CRA.1 - ADCIN1
;   Bit 0        (1)   CRA.0 - ADCIN0
;*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-
;- Event Manager Module Reset
;*
;-    This section resets all of the Event Manager Module
;     Registers. This is necessary for silicon revision 1.1;
;     but not necessary for silicon revisions 2.0 and later.
;*
;-
;*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-

   LDP           #232     ;DP=232 Data Page for the Event Manager
   SPLK          #0000h,GPTCON ;Clear General Purpose Time Control
   SPLK          #0000h,T1CON  ;Clear GP Timer 1 Control
   SPLK          #0000h,T2CON  ;Clear GP Timer 2 Control
   SPLK          #0000h,T3CON  ;Clear GP Timer 3 Control

   SPLK          #0000h,COMCON ;Clear Compare Control
   SPLK          #0000h,ACTR   ;Clear Full Compare Action Control
;                                   Register
   SPLK          #0000h,SACTR  ;Clear Simple Compare Action
;                                   Control Register
   SPLK          #0000h,DBTCON ;Clear Dead-Band Timer Control
;                                   Register

   SPLK          #0000h,CAPCON ;Clear Capture Control

   SPLK          #0FFFFh,EVIFRA;Clear Interrupt Flag Register A
   SPLK          #0FFFFh,EVIFRB;Clear Interrupt Flag Register B
   SPLK          #0FFFFh,EVIFRC;Clear Interrupt Flag Register C

   SPLK          #0000h,EVIMRA ;Clear Event Manager Mask Register A
   SPLK          #0000h,EVIMRB ;Clear Event Manager Mask Register B
   SPLK          #0000h,EVIMRC ;Clear Event Manager Mask Register C

;*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-
;-      End of RESET section for silicon revision 1.1          *
;*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-*-

;-------------------------------
; Set up Event Manager Module
;-------------------------------
T1COMPARE        .set  11111111b        ;Value does not matter
T1PERIOD         .set  1111111111b      ;Maximum ADC Value


                 LDP   #232           ;DP=232, Data Page for Event
;                                      Manager Addresses
                 SPLK  #T1COMPARE,T1CMPR   ;Compare value for 50%
;                                       duty cycle

;                       2109876543210
                 SPLK  #0000001010101b,GPTCON

;GPTCON - GP Timer Control Register
;   Bit 15       (0)   T3STAT - GP Timer 3 Status.  READ ONLY
;   Bit 14       (0)   T2STAT - GP Timer 2 Status.  READ ONLY
;   Bit 13       (0)   T1STAT - GP Timer 1 Status.  READ ONLY
;   Bits 12-11   (00)  T3TOADC - ADC start by event of GP Timer 3
;                         No event starts ADC
;   Bits 10-9    (00)  T2TOADC - ADC start by event of GP Timer 2
;                         No event starts ADC
;   Bits 8-7     (00)  T1TOADC - ADC start by event of GP Timer 1
;                         No event starts ADC
;   Bit 6        (1)   TCOMPOE - Compare output enable
;                         Enable all three GP timer compare outputs
;   Bits 5-4     (01)  T3PIN - Polarity of GP Timer 3 compare
;                                  output, Active Low
;   Bits 3-2     (01)  T2PIN - Polarity of GP Timer 2 compare
;                                    output, Active Low
;   Bits 1-0     (01)  T1PIN - Polarity of GP Timer 1 compare
;                                    output, Active Low

   SPLK          #T1PERIOD,T1PR   ;Period value for 20kHz signal
   SPLK          #0000h,T1CNT     ;Clear GP Timer 1 Counter
   SPLK          #0000h,T2CNT     ;Clear GP Timer 2 Counter
   SPLK          #0000h,T3CNT     ;Clera GP Timer 3 Counter


;                       5432109876543210
                 SPLK  #0001000000001010b,T1CON

;T1CON - GP Timer 1 Control Register
;  Bits 15-14    (00)  FREE,SOFT - Emulation Control Bits
;                         Stop immediately on emulation suspend
;   Bits 13-11   (010) TMODE2-TMODE0 - Count Mode Selection
;                         Continuous-Up Count Mode
;   Bits 10-8    (000) TPS2-TPS0 - Input Clock Prescaler
;                         Divide by 1
;   Bit 7        (0)   Reserved
;   Bit 6        (0)   TENABLE - Timer Enable
;                         Disable timer operations
;   Bits 5-4     (00)  TCLKS1,TCLKS0 - Clock Source Select
;                         Internal Clock Source
;   Bits 3-2     (10)  TCLD1,TCLD0 - Timer Compare Register
;                         Reload Condition Immediately
;   Bit 1        (1)   TECMPR - Timer compare enable
;                         Enable timer compare operation
;   Bit 0        (0)   Reserved

;                       5432109876543210
                 SPLK  #0000000000000000b,T2CON
                                             ;GP Timer 2 - Not Used

;T2CON - GP Timer 2 Control Register
;   Bits 15-14   (00)  FREE,SOFT - Emulation Control Bits
;                            Stop immediately on emulation suspend
;   Bits 13-11   (000) TMODE2-TMODE0 - Count Mode Selection
;                            Stop/Hold
;   Bits 10-8    (000) TPS2-TPS0 - Input Clock Prescaler
;                            Divide by 1
;   Bit 7        (0)   TSWT1 - GP Timer 1 timer enable bit
;                            Use own TENABLE bit
;   Bit 6        (0)   TENABLE - Timer Enable
;                            Disable timer operations
;   Bits 5-4     (00)  TCLKS1,TCLKS0 - Clock Source Select
;                            Internal Clock Source
;   Bits 3-2     (00)  TCLD1,TCLD0 - Timer Compare Register
;                            Reload Condition
;                            When counter is 0
;   Bit 1        (0)   TECMPR - Timer compare enable
;                            Disable timer compare operation
;   Bit 0        (0)   SELT1PR - Period Register select
;                            Use own period register

;                       5432109876543210
                 SPLK  #0000000000000000b,T3CON
                                              ;GP Timer 3 - Not Used

;T3CON - GP Timer 3 Control Register
;   Bits 15-14   (00)  FREE,SOFT - Emulation Control Bits
;                            Stop immediately on emulation suspend
;   Bits 13-11   (000) TMODE2-TMODE0 - Count Mode Selection
;                            Stop/Hold
;   Bits 10-8    (000) TPS2-TPS0 - Input Clock Prescaler
;                            Divide by 1
;   Bit 7        (0)   TSWT1 - GP Timer 1 timer enable bit
;                            Use own TENABLE bit
;   Bit 6        (0)   TENABLE - Timer Enable
;                            Disable timer operations
;   Bits 5-4     (00)  TCLKS1,TCLKS0 - Clock Source Select
;                            Internal Clock Source
;   Bits 3-2     (00)  TCLD1,TCLD0 - Timer Compare Register
;                            Reload Condition
;                            When counter is 0
;   Bit 1        (0)   TECMPR - Timer compare enable
;                            Disable timer compare operation
;   Bit 0        (0)   SELT1PR - Period Register select
;                            Use own period register

;                       5432109876543210
                 SPLK  #0000000010000000b,EVIMRA ;Enables the T1PINT
;------------------------------
; Set up ADC Module
;------------------------------
                 LDP   #224     ;DP = 224 Data Page for ADC Registers

;                       5432109876543210
                 SPLK  #1000110100000000b,ADCTRL1

;ADCTRL1 - ADC Control Register 1
;   Bit 15       (1)   Suspend-SOFT -
;                      Complete Conversion before halting emulator
;   Bit 14       (0)   Suspend-FREE -
;                            Operations is determined by Suspend-SOFT
;   Bit 13       (0)   ADCIMSTART - ADC start converting immediately
;                            Immediate Start of Conversion
;   Bit 12       (0)   ADC2EN - Enable/Disable ADC2
;                            Disable ADC2
;Bit 11          (1)   ADC1EN - Enable/Disable ADC1
;                            Enable ADC1
;   Bit 10       (1)   ADCCONRUN - ADC Continuous Conversion Mode
;                           Continuous Conversion
;   Bit 9        (1)   ADCINTEN - Enable ADC Interrupt
;                           Request Interrupt when ADCINTFLAG is set
;   Bit 8        (1)   ADCINTFLAG - ADC Interrupt Flag
;                           Clear Interrupt Flab Bit
;   Bit 7        (0)   ADCEOC - End of Conversion Bit  READ ONLY
;   Bits 6-4     (000) ADC2CHSEL - ADC2 Channel Select
;                           Channel 8
;   Bits 3-1     (000) ADC1CHSEL - ADC1 Channel Select
;                           Channel 0
;   Bit 0        (0)   ADCSOC - ADC Start of conversion bit
;                           No Action

;                       5432109876543210
                 SPLK  #0000000000000101b,ADCTRL2

;ADCTRL2 - ADC Control Register 2
;   Bits 15-11   (00000)Reserved
;   Bit 10       (0)   ADCEVSOC - Event Manager SOC mask bit
;                           Mask ADCEVSOC
;   Bit 9        (0)   ADCEXTSOC - External SOC mask bit
;                           Mask ADCEXTSOC
;   Bit 8        (0)   Reserved
;   Bits 7-6     (00)  ADCFIFO1 - Data Register FIFO1 Status
;                           READ ONLY
;   Bit 5        (0)   Reserved
;   Bits 4-3     (00)  ADCFIFO2 - Data Register FIFO2 Status
;                           READ ONLY
;   Bits 2-0     (101) ADCPSCALE - ADC Input Clock Prescaler
;                           Prescale Value 16
;                           SYSCLK Period = 0.1usec
;                           0.1usec x 16 x 6 = 9.6 usec >= 6usec

;-----------------------------------
; Set up EVM DAC Module
;-----------------------------------
;This section lets youuse the DAC as an input into the ADC if
; there is not an easily available source(a waveform generator).

                 LDP   #0

                 SPLK  #4h,GPR0         ;The DAC requires that
                 OUT   GPR0,WSGR        ;I/O accesses require 1WS

                 SPLK  #03FFh,DAC0VAL
                 SPLK  #07FFh,DAC1VAL
                 SPLK  #0BFFh,DAC2VAL
                 SPLK  #0FFFh,DAC3VAL

                 OUT   DAC0VAL,DAC0        ;DACOUT0 = 1.25V
                 OUT   DAC1VAL,DAC1        ;DACOUT1 = 2.50V
                 OUT   DAC2VAL,DAC2        ;DACOUT2 = 3.75V
                 OUT   DAC3VAL,DAC3        ;DACOUT3 = 5.00V
                 OUT   DAC3VAL,DACUPDATE   ;Output the values on the
;                                    DAC pins

                 LDP   #232
                 SBIT1 T1CON,B6_MSK        ;Sets Bit 6 of T1CON

;T1CON - GP Timer 1 Control Register
;   Bit 6        (1)   TENABLE - Timer Enable
;                           Enable Timer Operations

                 LDP   #224
                 SBIT1 ADCTRL1,B0_MSK   ;Sets Bit 0 of ADCTRL1

                 CLRC  INTM          ;Enable Interrupts

END              B  END

;------------------------------------------------------------------
;Interrupt Service Routine that Changes the Compare Register
;------------------------------------------------------------------

CHG_CMPR         LDP   #224     ;DP = 224 Data Page for ADC Registers
                 LACC  ADCTRL1  ;ACC = ADCTRL1 \ Clears the ADC Int
                 SACL  ADCTRL1  ;ADCTRL1 = ACC / flag if set

                 LACC  ADCFIFO1 ;Load the converted value
                 RPT   #5       ;Shift the value to the right 6 times
                 SFR            ;since 6 LSBs are always 0

                 LDP   #232     ;DP = 232 Data Page for Event
;                                              Manager Module
                 SACL  T1CMPR   ;Store ADC Value into T1CMPR

                 LACC  EVIFRA   ;ACC = EVIFRA \ Clears the
;                                                EVIFR Int
                 SACL  EVIFRA   ;EVIFRA = ACC / Flags if set

                 CLRC  INTM     ;Enable Interrupts
                 RET

;===================================================================
; I S R  -  PHANTOM
;
; Description:   Dummy ISR, used to trap spurious interrupts.
;
; Modifies:      Nothing
;
; Last Update:   16 June 95
;===================================================================
PHANTOM          KICK_DOG         ;Resets WD counter
                    B  PHANTOM
```