A TDM Interface for the TMS320C54x DSP

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A TDM Interface for the TMS320C54x DSP

Abstract

This application report describes the hardware logic required to interface the Texas Instruments (TI™) TMS320C54x digital signal processor (DSP) buffered serial port to a T1/E1-type serial bus. This interface allows the system designer to dynamically reconfigure the DSPs to compress/decompress voice on selected time slots.

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Introduction

The Pulse Code Modulation (PCM) technique digitally transmits analog voice signals. PCM samples the original analog signal at 8000 Hz and quantifies each sample into a coded set of binary digits.

Companding is a technique used in the quantizer to improve the signal to quantizing noise (SQR) ratio. In a linear quantizing system, SQR increases with increasing signal amplitudes so that large signals have a higher SQR than smaller signals. This condition is not desirable in systems using small signals.

To remedy this, the size of the quantization intervals in the quantizer is adjusted with respect to the input signal level so that the intervals are smaller for small signals and larger for large signals. This creates a non-linear output versus input relationship, and results in the output being *compressed* with respect to the input.

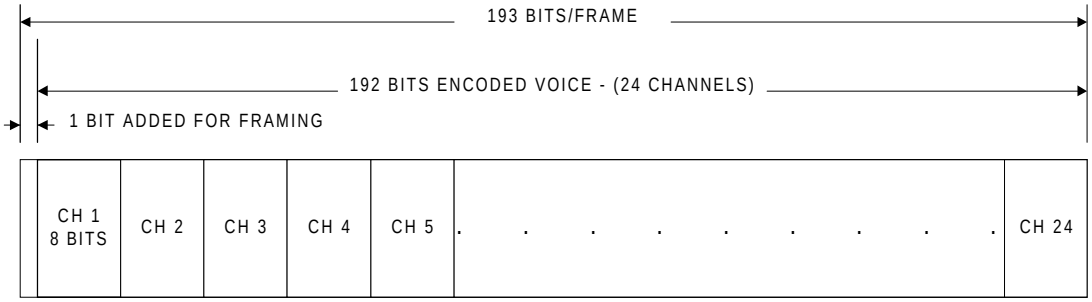
At the receiving end, the signal must be expanded to retrieve the original signal. This combination of compression and expansion techniques in a codec is called Compander COMpressor/exPANDER). When companding is used, the SQR is approximately the same across the range of input signal levels. The North American and Japanese markets use μ-255 companding, whereas the European networks use A-law companding.

After the input speech has been sampled, quantized, and encoded in digital form, it must be transmitted to its final destination. Since every speech channel occupies 64000 bits/second (= 8000 samples multiplied by 8 bits/sample), it is uneconomical to send only one encoded voice channel over a single transmission channel. A multiplexing scheme that multiplexes the transmission of multiple voice channels over a single transmission channel is used. Since the multiplexing scheme sends information separated in time, it is called Time Division Multiplexing (TDM).

To identify the beginning of each frame (that is, the start of Channel 0), the sending end of the multiplexed stream must add framing information. The framing information may consist of a single bit, a code word of the same length as the other channels in the frame, a pre-determined pattern, or a deletion or alteration of a bit in the code word. The schemes generally used in the telephone network add either one bit or one code word (8 bits) to the data stream to identify frame boundaries.

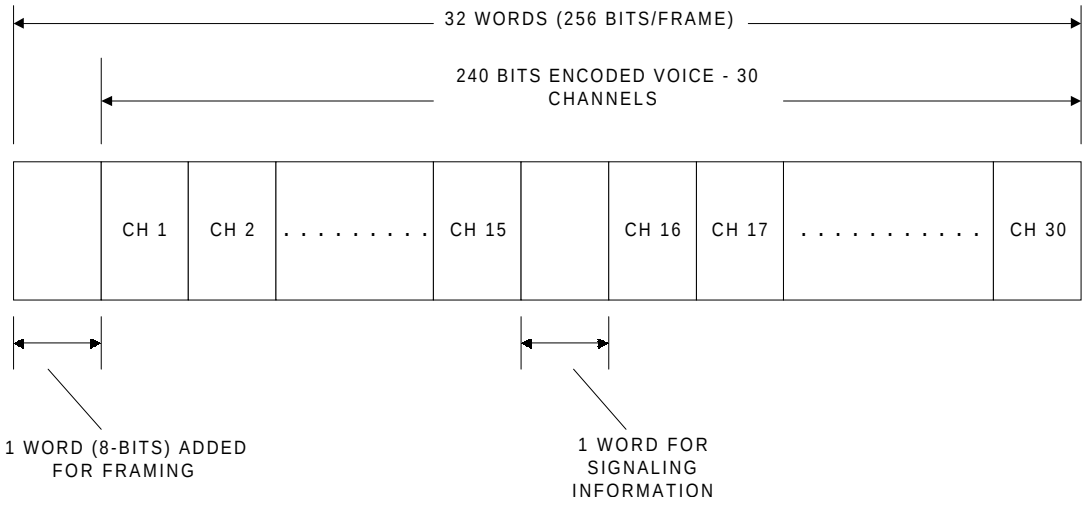
The US uses T1 as the basic digital multiplexing scheme. It is also called the Primary Rate Carrier system, or simply primary rate. A T1 line can transmit 24 digitized voice channels multiplexed over a 4-wire cable (2 wires for transmit and 2 wires for receive). The format used to frame transmitted data in the T1 system is called DS-1 and is shown in Figure 1. DS1 partitions data into 193 bits. The first bit is always interpreted as the framing synchronization bit. The remaining 192 bits represent 8-bit words from 24 channels. Since a voice channel is sampled at 8kHz (or one 8-bit sample every 125 microseconds), the T1 system must send 193 bits in 125 μseconds, which is equivalent to 1.544 Mbits/second.

Figure 1. Added Bit Framing for DS-1



The European system (a.k.a. E1) carries 30 channels of encoded voice. The format used to frame transmitted data in the E1 system is called CEPT (Conference of European Postal and Telecommunications Administration), or PCM-30. This system inserts one 8-bit word before channel 0 to signify the start of the frame, and another 8-bit word between channels 15 and 16 for signaling information (see Figure 2). This means that the length of the CEPT/PCM-30 frame is 256 bits (or 32 words). Since the sampling rate is still 8000 Hz or 125 μseconds, the data rate is 256/125 μseconds = 2.048Mbps.

Figure 2. Added Word Framing for CEPT/PCM-30



C54x Peripherals

The C54x devices support three different types of synchronous serial port interfaces:

- Standard synchronous serial port
- Buffered serial port (BSP)
- Time division multiplexed (TDM) serial port

The standard synchronous serial port provides a full-duplex communication with serial devices, such as codecs and A/D converters, and not TDM sources, such as a T1 or E1 line.

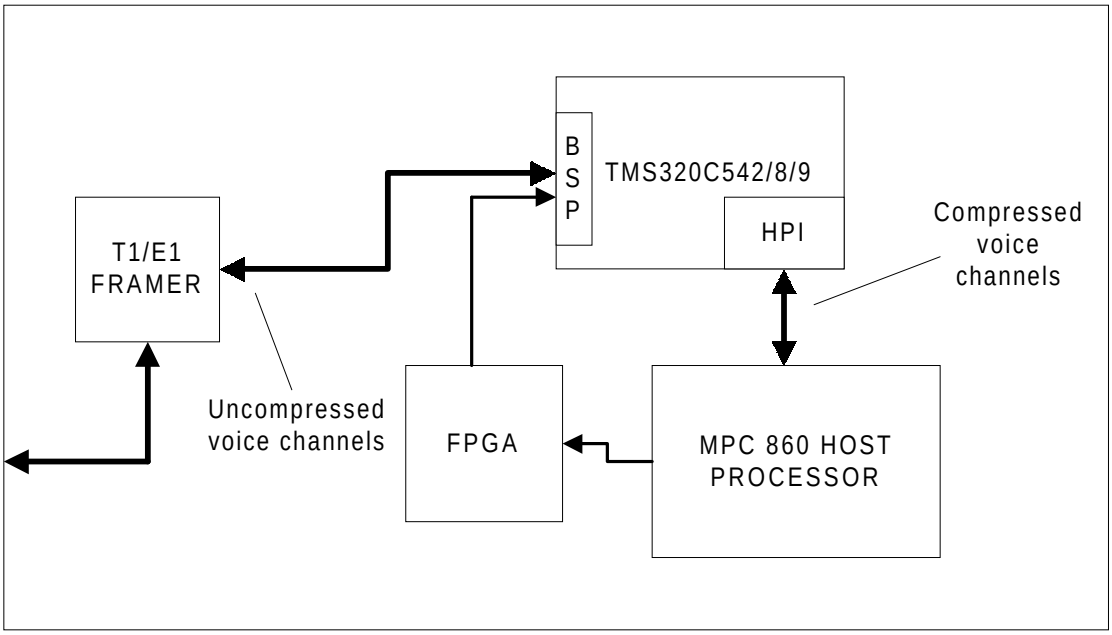
The BSP features a buffering mechanism that greatly reduces the CPU overhead in handling serial data transfers. Except for the buffering mechanism, the BSP functions in a similar manner to the synchronous serial port. Hence, the BSP is also not capable of handling TDM data sources.

The TDM serial port allows the device to communicate serially with up to 7 other devices. This port is therefore well suited for multiprocessor applications. Unfortunately, this port cannot be used to handle telephony data coming from a T1 or an E1 line.

Designing an Interface

This interface is designed to operate in a multiprocessor environment. The target system, used in a voice-over Frame Relay application, comprises multiple C54x DSPs controlled by a Motorola host processor, the MPC860 (see Figure 3). The host processor determines which voice channel will be compressed/decompressed by a DSP using a predetermined voice-coding scheme.

Figure 3. Hardware Platform



Requirements

The following is required of a TDM interface:

- Indication of start of channel 0
- Synchronization to a T1 clock (1.544 MHz) or an E1 clock (2.044 MHz)
- A means of selecting a time slot

Item a) can be achieved by connecting the T1 (or E1) frame sync (which indicates the start of channel 0) to the interrupt pin on a DSP. To maintain simplicity, we shall refer to the T1 (or E1) frame sync as the system frame sync. Since the system has to be capable of selectively enabling a specific channel/channels under control of the host processor, the system frame sync signal cannot be used to directly drive the serial port frame sync signal. Connecting the system frame sync to a hardware DSP interrupt enables the DSP to identify the beginning of any (and every) frame.

Item b) can be achieved by clocking the serial port at the correct (or appropriate) clock rate (1.544 MHz or 2.044 MHz).

Item c) can be achieved by writing the value of the time slot or channel number to a designated address in the glue logic circuit. The host processor accomplishes this function.

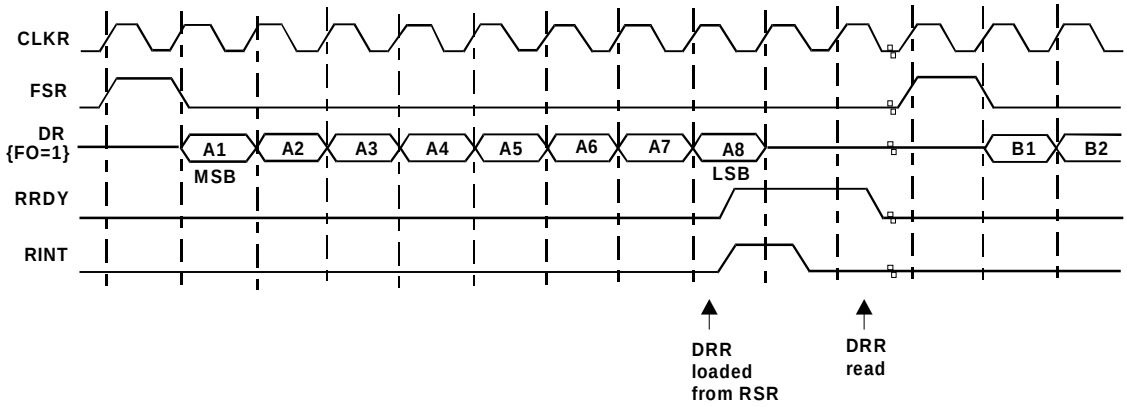
Understanding the Schematic

Appendix A shows the hardware interconnection between the C54x, MPC860, and FPGA devices. Appendix B shows a schematic of the proposed TDM interface implemented using an Altera 8000 series FPGA.

The heart of the FPGA circuit is an 8-bit counter. The two inputs to the counter are the 8 kHz system frame sync (FS) and a 2.048 MHz clock (CLKIN). The counter has 8 outputs, of which Q_D through Q_H are used to select a time slot or channel. These signals are labeled TSC0 through TSC4. These five outputs allow the user to select any one of the 2^5 (=32) channels.

Outputs Q_A through Q_C are used to generate a signal labeled Bit6. Bit6 indicates the occurrence of the sixth clock transition. Referring to Figure 4, it is evident that SPI operation starts when the frame sync signal becomes active, this event being sampled on the falling edge of the receive clock. A clock cycle later, the MSB is received at the falling edge of the receive clock sampling the frame sync pulse at low level. This implies that, to start receiving/sending data for a given channel, the frame sync has to be qualified one clock cycle earlier. This is precisely what signal Bit6 intends to achieve.

Figure 4. Buffered Serial Port in Receive Mode Timing Diagram



In the operating environment of this application, there are 6 C54x-66 DSPs per board, each capable of compressing at least two time slots.[1] The FPGA has three sets of time-slot-selection latch units into which the host processor writes the necessary time slots. Each latch is capable of generating the necessary signals to select two time slots per DSP for two DSPs. Data lines D0-D4 and address lines A2-A4 are brought in from the host processor. The outputs of the latch-pair are labeled P0CHAD0, P0CHAD1, P0CHAD2, P0CHAD3, P0CHAD4 and P0CHBD0, P0CHBD1, P0CHBD2, P0CHBD3, P0CHBD4, for time slots A and B, respectively, of the first DSP.

The outputs of the latch and the 8-bit counter are compared using a comparator circuit. The result of the comparison is ANDed with the BIT6 signal, the result of which is further combined in an AND gate with TSE0- to generate the signal labeled FS0. The last AND operation with TSE0- ensures that time slot zero is not available for selection. Signal FS0, which is a single pulse in clock cycle six of the previous frame, is clocked through a D flip-flop to generate FSC0, which is used as the frame sync for the Buffered Serial Port of the DSP.

Signal FS0 is also used to generate the gated clock signal GRCLK0 via a cascade of three D flip-flops clocked either with the CLK or CLK- signals. The clock gating control signal spans across the 8 clock cycles of the time slot of interest.

Frame sync and gated clock signals can be similarly generated for the other DSPs on the board, the schematics for which are identical to those shown in Appendix A.

[1] The capability of a DSP to handle n channels of speech depends on the voice coding scheme and other system-dependent features such as Line Echo Cancellation, Fax Relay etc.

HSEL0-, HSEL1-, HSEL2-, HSEL3-, HSEL4-, and HSEL5- are chip select signals from the host processor to the DSP and connect to the HPI chip select pins of each of the six DSPs, respectively.

Practical Usage

While the given circuit might seem like overkill for most applications, it is designed based on some of the other needs of the customer, details of which are not available. The Altera FPGA used in this circuit costs about $10.00. The authors suggest that cheaper FPGAs/PALs are available and can be used depending on the needs of individual hardware designers.

Appendix A. Hardware Interconnection Schematics

Figure 5. System Interconnection

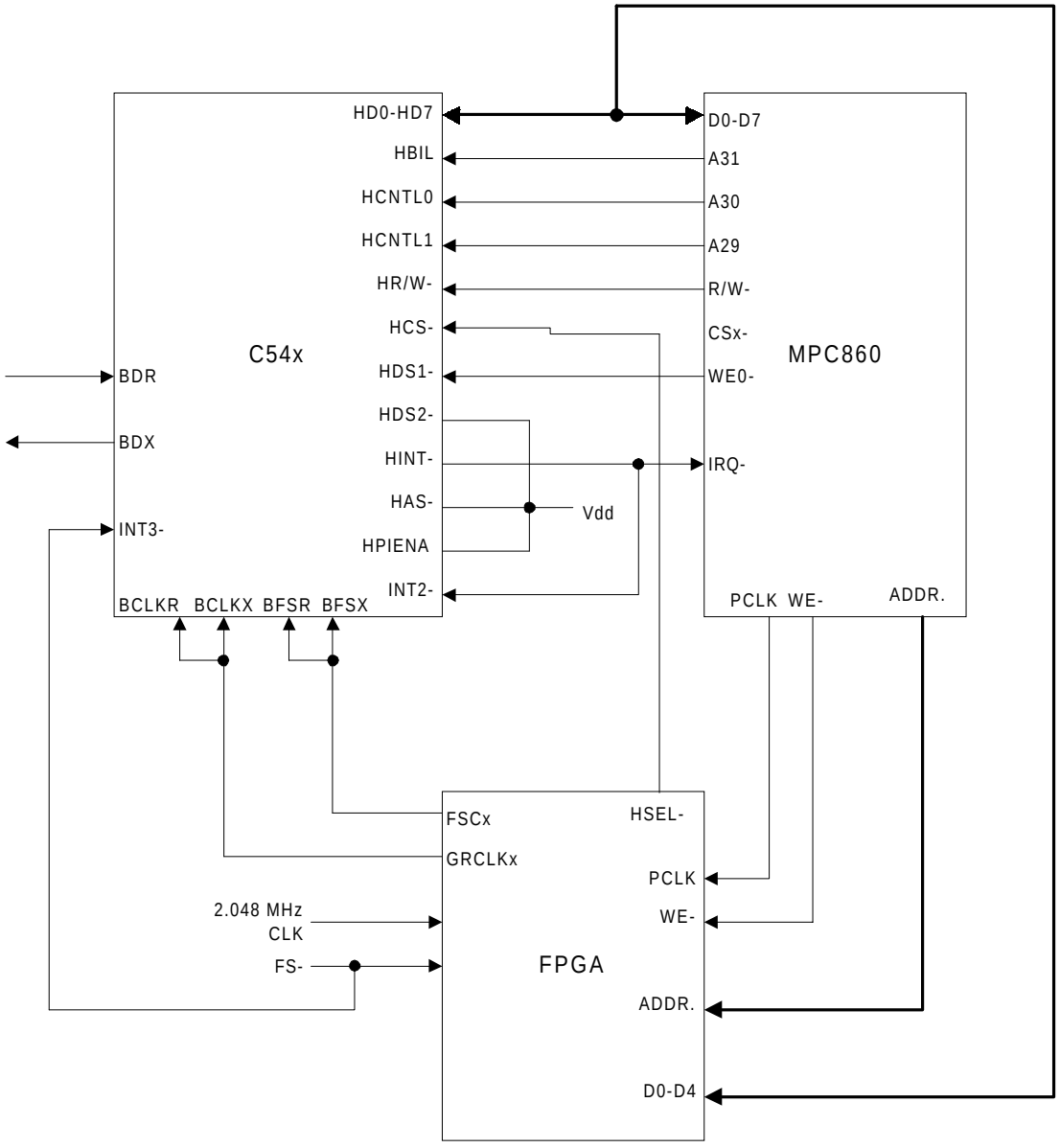


Figure 6. Generation of the BIT6 Signal

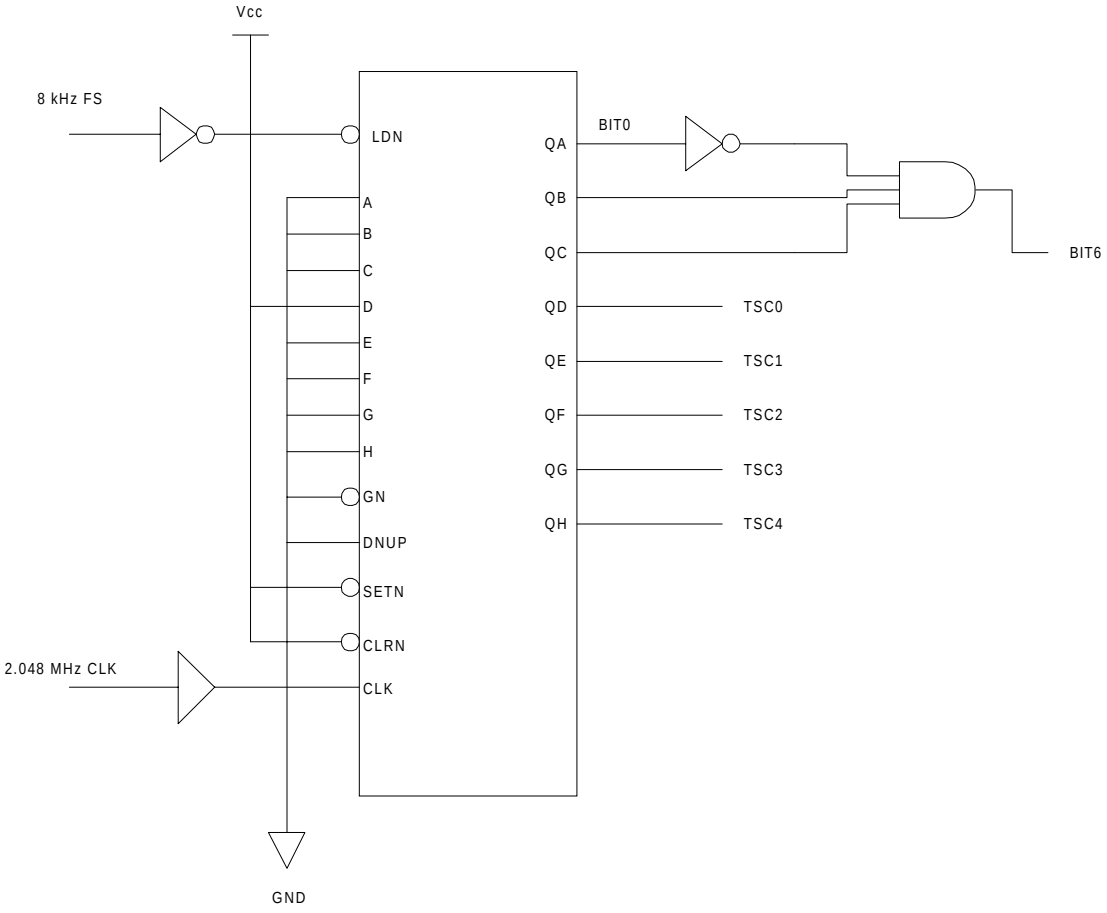


Figure 7. Time Slot Selection Latch for Two DSPs

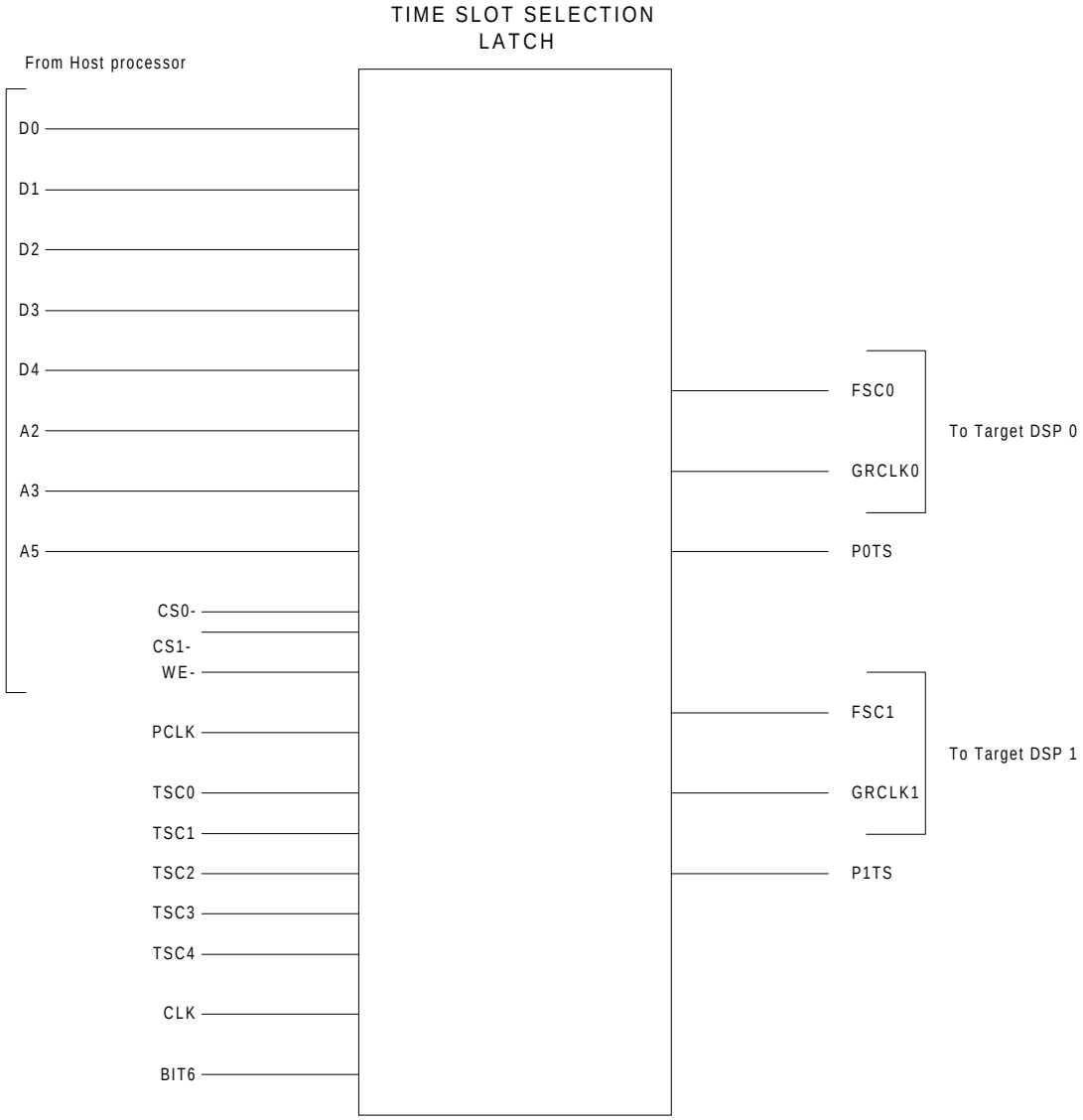


Figure 8. Inside the Time Slot Selection Latch for Slot A, DSP 0

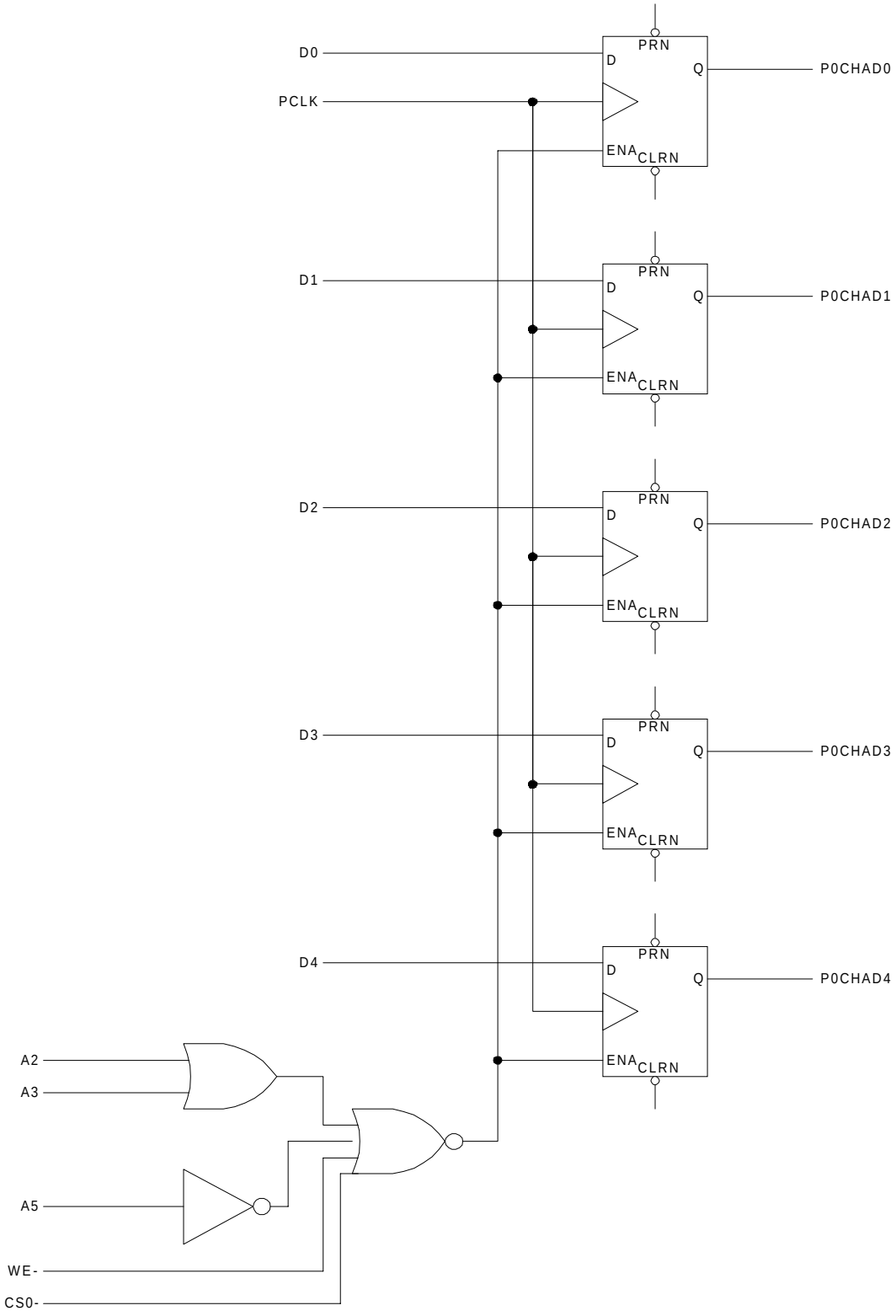


Figure 9. Inside the Time Slot Selection Latch for Slot B, DSP 0

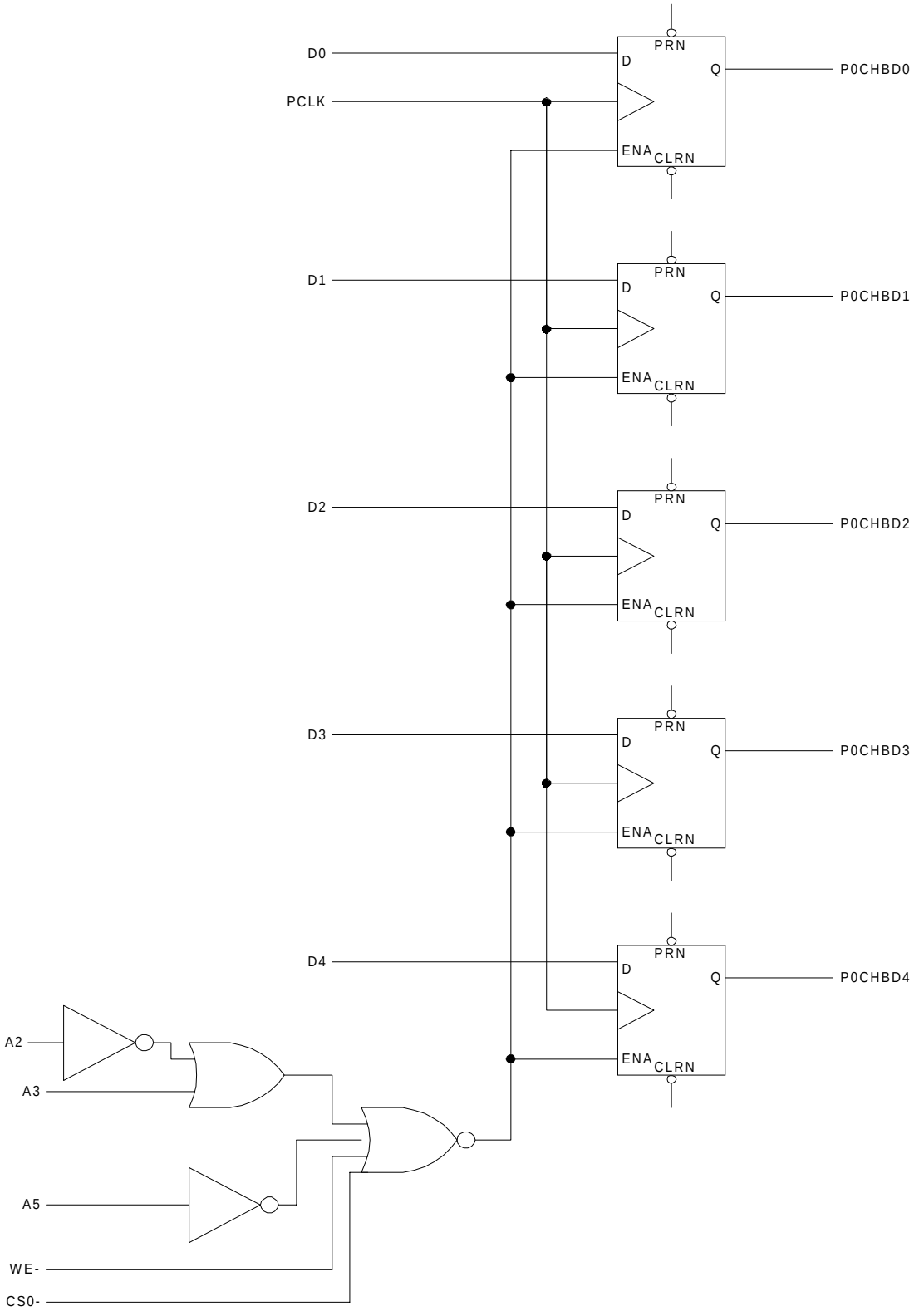


Figure 10. Generation of Frame Sync for DSP

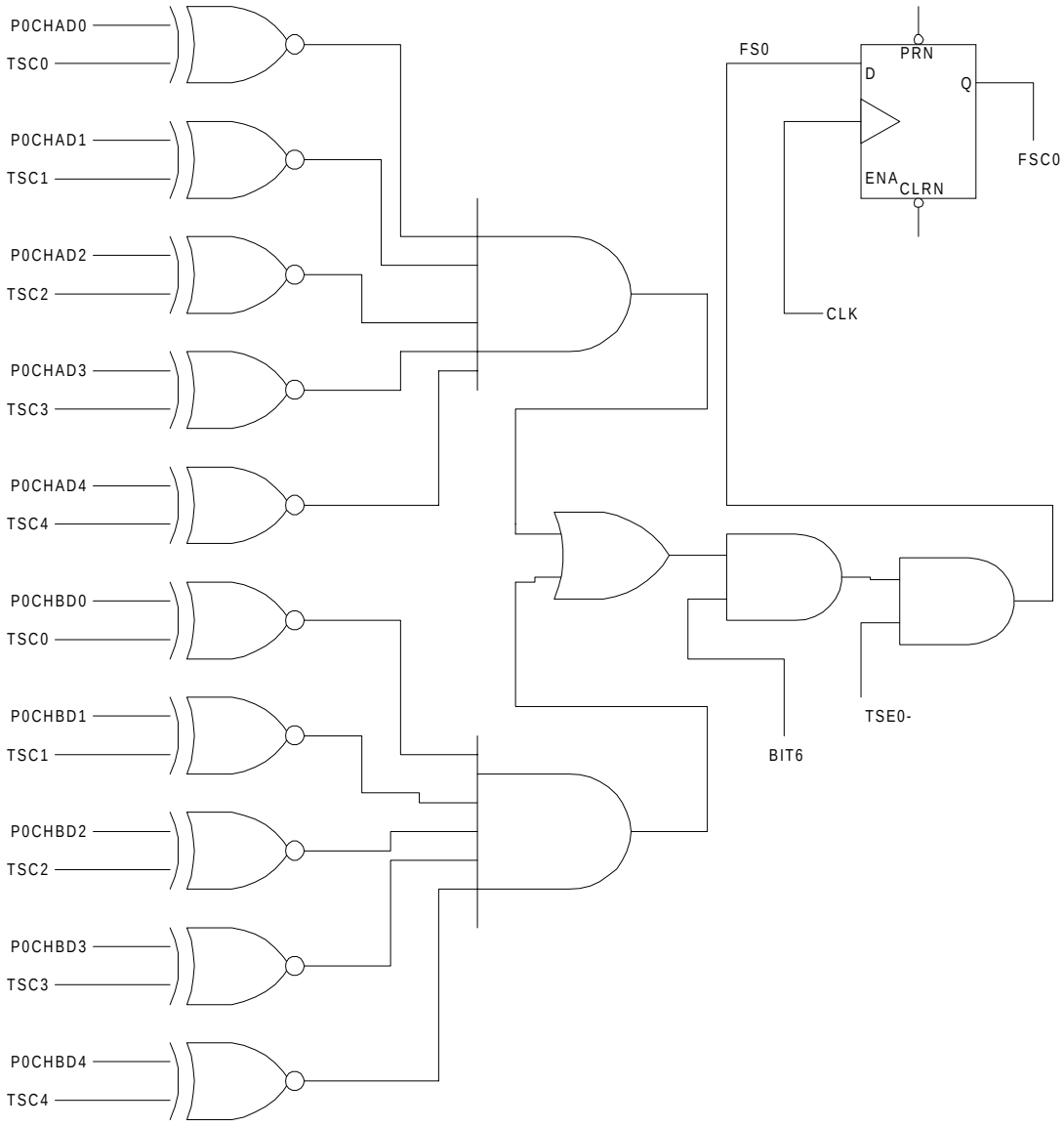


Figure 11. Generation of Gated Clock for DSP

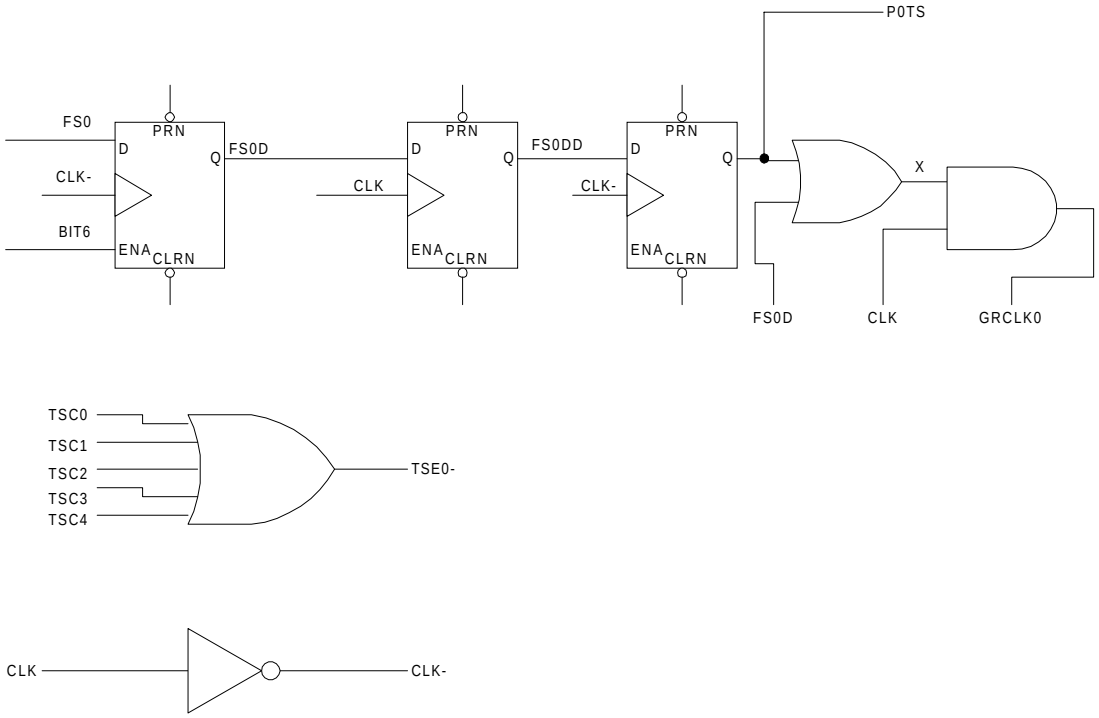


Figure 12. Combining Transmit Data from All DSPs

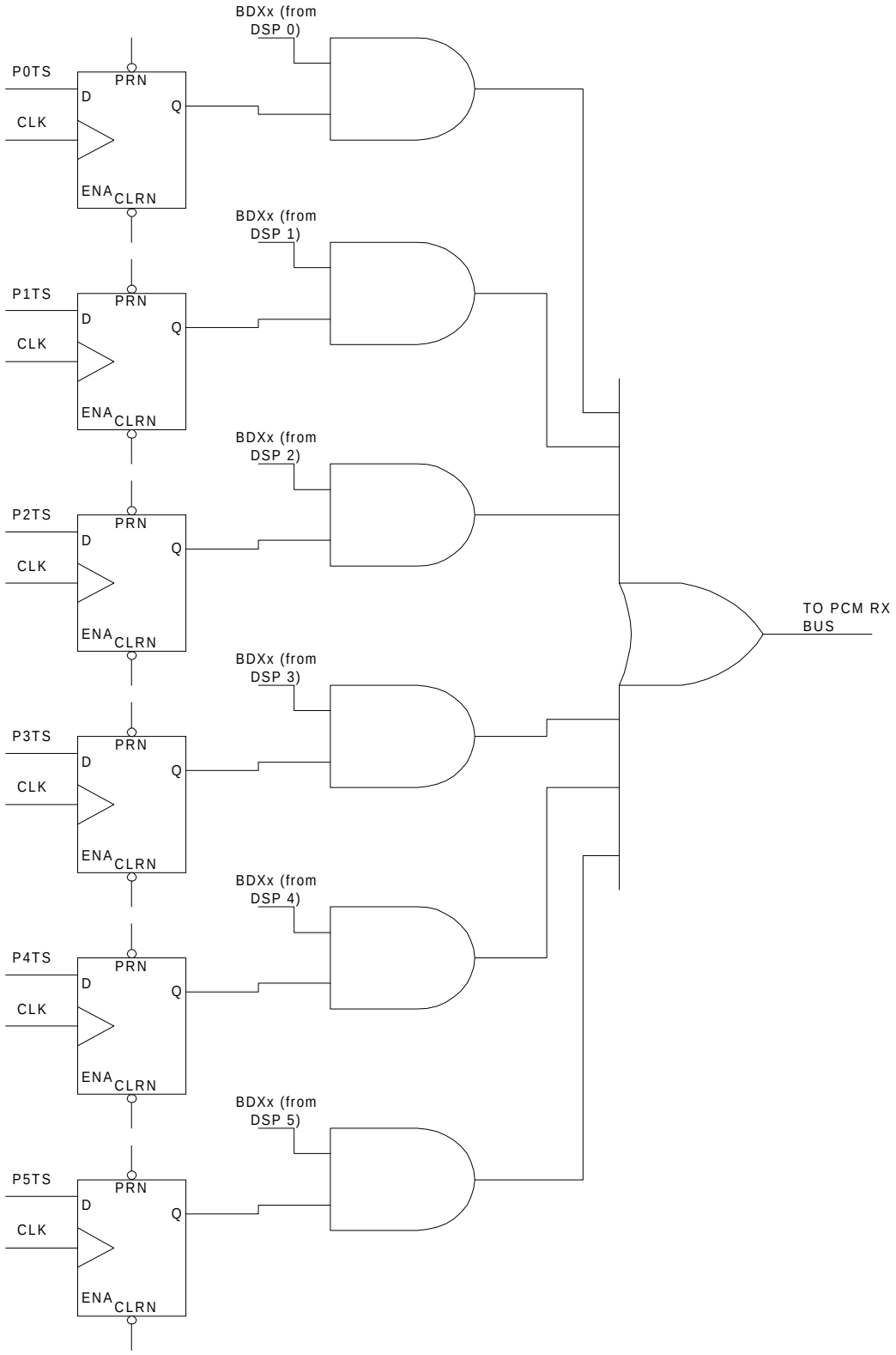
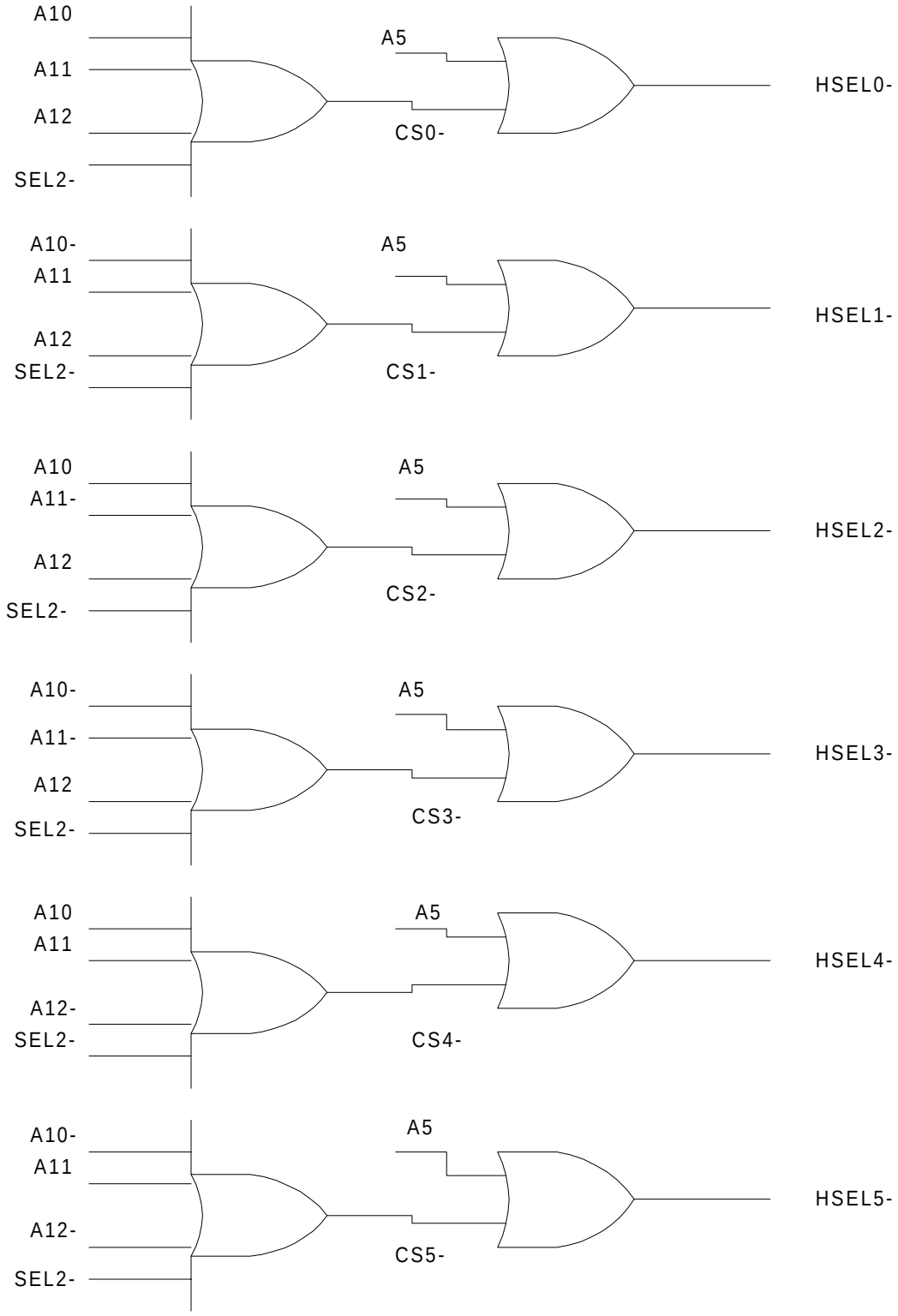
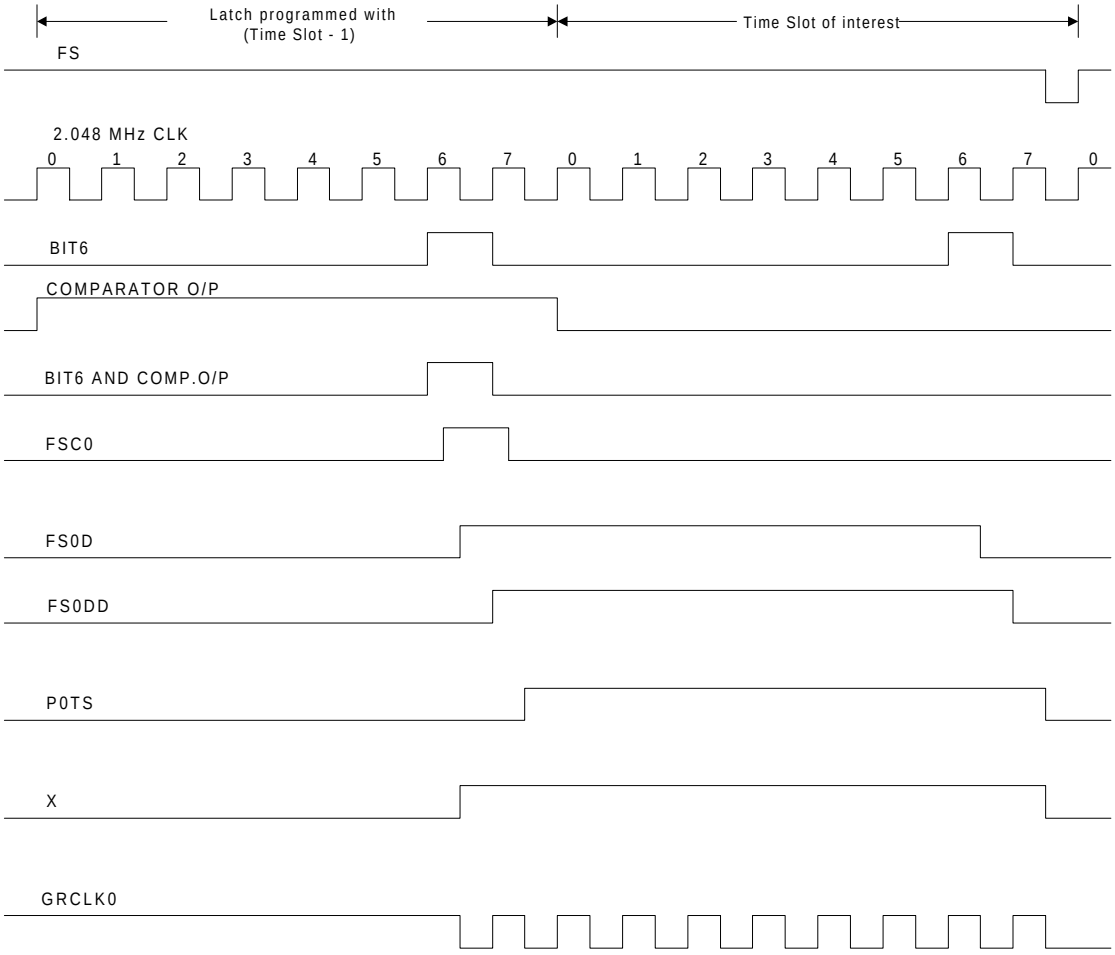


Figure 13. Generation of HPI Chip Select Signals



Appendix B. Timing Diagram for FPGA

Figure 14. Timing Diagram for FPGA



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