How to Begin Development Today and Migrate Across the TMS320C6202/02B/03B/04 DSPs

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ABSTRACT

Development can begin now for Texas Instruments TMS320C6202, C6202B, C6203B, and C6204 digital signal processor (DSP) systems.

Because of the compatibility between TMS320C6000™ generation devices, existing C6000™ tools and development platforms can be used to develop code for the current TMS320C62x™ generation and other future devices. This capability allows systems to be up and running when silicon becomes available.

This document briefly describes the similarities and differences between the C6202/02B/03B/04 digital signal processors (DSPs), and serves as a reference for designers migrating between the C6202/02B/03B/04, either for performance improvement, or improved feature set.

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1 TMS320C6000 Platform Introduction

Introduced in February 1997, the C6000 platform is based on TI's VelociTI™ architecture, an advanced, very long instruction word (VLIW) architecture for DSPs. Advanced features of VelociTI architecture include instruction packing, conditional branching, and pre-fetched branching, all of which overcome problems that were associated with previous VLIW implementations. The architecture is highly deterministic, with few restrictions on how or when instructions are fetched, executed, or stored. This architectural flexibility is key to the breakthrough efficiency levels of the C6000 compiler.

Figure 1 illustrates the roadmap for the fixed-point devices of the C62x™ generation.

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C62x is a trademark of Texas Instruments.

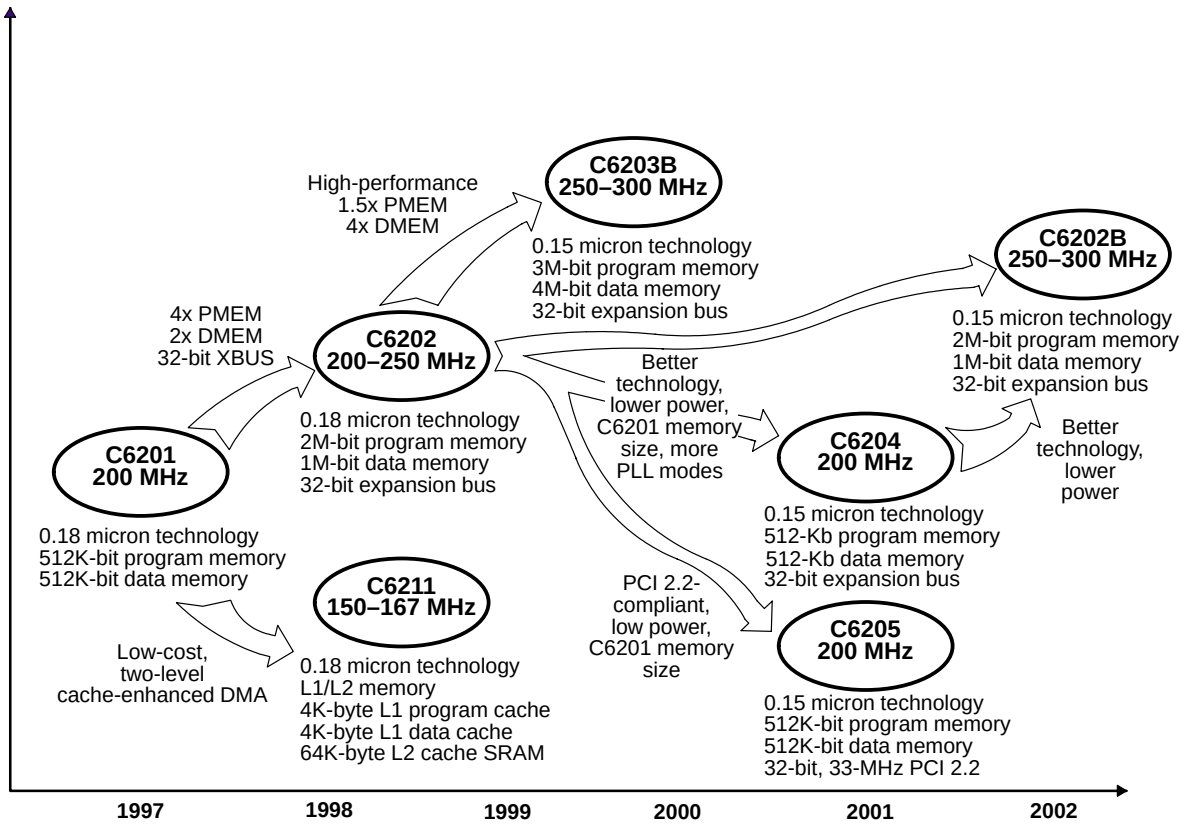

Figure 1. TMS320C6200 Fixed-Point Roadmap

2 Development With the TMS320C6202 and TMS320C6202B DSPs

The Texas Instruments TMS320C6000 platform of high-performance digital signal processors now includes the TMS320C6202B, in addition to the existing C6202.

The C6202 and C6202B are large-memory versions of the original C6000 device, C6201. Similar to the C6202, the C6202B is capable of achieving 2000 million instructions per second (MIPS) at 250 MHz, and 2400 MIPS at 300 MHz.

The 32-bit expansion bus (XB) supports interfaces to a variety of asynchronous peripherals, asynchronous or synchronous FIFOs, PCI Bridge chips, and other external masters. Thus, the XB provides additional bandwidth by complementing the EMIF. The XB also provides either a synchronous (master and slave mode) or asynchronous (slave mode similar to the C6201) host port interface (HPI). The synchronous mode provides higher throughput in the range of 133–266 megabits per second (Mbps), an improvement of four to eight times over the C6201 HPI.

The expansion bus is the main difference between the C6202 and the C6201. While the internal memories are much larger on the C6202, their functionality is equivalent to those of the C6201.

In addition to the central processing unit (CPU), many of the on-chip peripherals are common between C6000 devices.

Figure 2 illustrates a diagram of the C6202/02B DSP's roadmap. The blocks shaded gray are common to the C6201 devices and the C6202/02B.

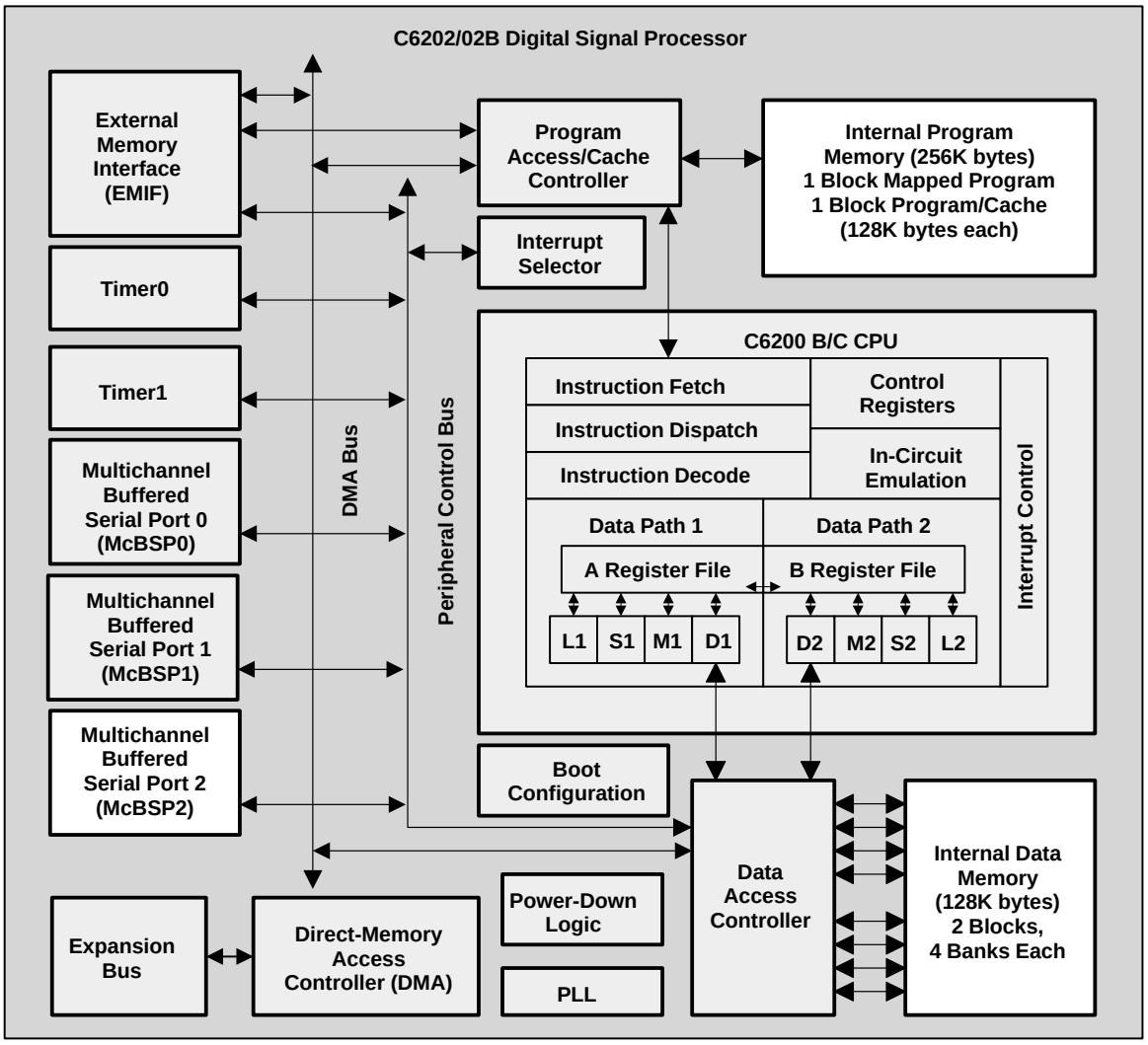

Figure 2. TMS320C6202 and C6202B Digital Signal Processors

2.1 C6202 and C6201 DSP Similarities

The C6202 is highly compatible with the first C6000 device, the C6201. The following components are identical between the devices:

- CPU: The CPU of the C6202 is identical to that of the C6201, which means that code written for the C6201 will run unmodified on the C6202.
- Multichannel Buffered Serial Ports (McBSPs): McBSP features are unchanged on the C6202.
- Direct-Memory Access (DMA) Controller: DMA is unchanged on C6202.
- 32-Bit Timers: Two timers are on the C6202.
- Interrupt Selection: There are 16 interrupt sources that may be used to interrupt the CPU or send an event to the DMA.

2.2 C6202 and C6201 DSP Differences

Several enhancements have been made to allow the C6202 greater performance capability. These include:

- Faster Clock Rate: The maximum clock frequency has been increased from 200 MHz to 250 MHz. This increased frequency allows the C6202 to achieve 2000 MIPS performance.
- Larger Internal Memory Space: The internal data and program memories have been significantly increased in size. The internal data memory has been increased two-fold, from 64K bytes on the C6201 to 128K bytes. Internal program memory has been quadrupled, with 256K bytes available. A 128K-byte block of the program memory is selectable as program cache.
- External Memory Interface (EMIF): The EMIF has been modified slightly to reduce the pin count of the C6202. Synchronous DRAM (SDRAM) and Sync-Burst SRAM (SBSRAM) share control signals on the EMIF bus. The two are mutually exclusive, so only one of the two memory types may be used in a system.
- Expansion Bus (XB): The expansion bus has been added to the C6202, to replace the Host-Port Interface (HPI) of the C6201. The C6202 offers a glueless interface to PCI bridge chips, synchronous industry-standard buses, synchronous FIFO memories, and asynchronous peripherals.
- Additional McBSPs: The C6202 has 3 McBSPs, while C6201 has only 2.

2.3 C6202 and C6202B DSP Similarities

The C6202B is highly compatible with the C6202. The following device components are identical between the devices:

- CPU: The CPU of the C6202B is identical to that of the C6202, which means that code written for the C6202 will run unmodified on the C6202B.
- Multichannel Buffered Serial Ports (McBSPs): The McBSPs are unchanged on the C6202B.
- Direct-Memory Access (DMA) Controller: The DMA transfers data between any two locations in the memory map.
- 32-Bit Timers: These are unchanged on the C6202B.
- Interrupt Selection: There are 16 interrupt sources that may be used to interrupt the CPU or send an event to the DMA.
- External Memory Interface (EMIF): The 32-bit memory interface is unchanged on the C6202B.
- Expansion Bus (XB): The 32-bit XB is unchanged on the C6202B.
- Package Options: Both C6202 and C6202B offer two package choices – 27 mm sq. and 18 mm sq. BGA. The pinout for both packages has been preserved.
- Input/Output (I/O) Voltage Level: The I/O voltage remains unchanged at 3.3 V, but the core voltage has changed, see below).

2.4 C6202 and C6202B DSP Differences

Several enhancements have been made to allow the C6202B greater performance capability. These include:

- Faster Clock Rate: The maximum clock frequency has been increased from 250 MHz to 300 MHz. This increased frequency will allow the C6202B to achieve 2400 MIPS during operation.
- More PLL Multiply Options: In addition to x1 and x4 modes that already exist on the C6202, the C6202B features six additional PLL modes (x6, x7, x8, x9, x10 and x11) on the GNY 384-pin BGA package, and two additional PLL modes (x8, and x10) on the GNZ 352-pin BGA package. The C6202 GJL package selects the PLL modes with CLKMODE[0] only, and CLKMODE[1] is internally connected to GND. On the GLS package, CLKMODE[1] and CLKMODE[2] are unconnected. Table 2, Table 3, and Table 4 give detailed explanations about CLKMODE pins.
- Lower Power Consumption: The C6202B is manufactured using an improved process resulting in a smaller die with lower power consumption.
- Core Voltage Level: The core power supply has been reduced from 1.8 V to 1.5 V, due to improved process technology. The I/O voltage remains unchanged at 3.3 V.
- Improved PLL: The PLL circuitry on the C6202B requires new component values for correct operation. These new components reduce the internal jitter. They can be found in Table 1.
- IBIS Modeling: The C6202B timing specifications take into account board-level constants, such as signal route delays. See the IBIS modeling section near the end of this application note for further details.

3 Development With the TMS320C6203B DSP

The Texas Instruments TMS320C6000 platform of high-performance digital signal processors now includes the TMS320C6203B. The C6203B provides up to 2400 million instructions per second (MIPS) at 300 MHz.

The C6203B is a larger-memory and faster-clock-speed version of its predecessor, the C6202. Due to the improved process, the higher-performance C6203B DSPs operate at lower power levels than the C6202 or the C6201. The C6203B DSP has been designed with a large on-chip memory, eliminating the need for external memory in many applications.

The 0.15 μm L-effective process technology delivers low power consumption of about 1.5 W (0.9 mA/MIPS). The two 32-bit buses (one via the EMIF and the other via the XB), similar to the C6202, maximize bandwidth.

All the features just described make the C6203 DSPs the right candidates for high performance, high density, and possibly a single-chip solution for most applications.

In addition to the CPU, many of the on-chip peripherals are common between C6000 devices.

Figure 3 illustrates a diagram of the C6203B DSP’s roadmap. Blocks shaded gray are common to the C6202 and C6203B DSPs.

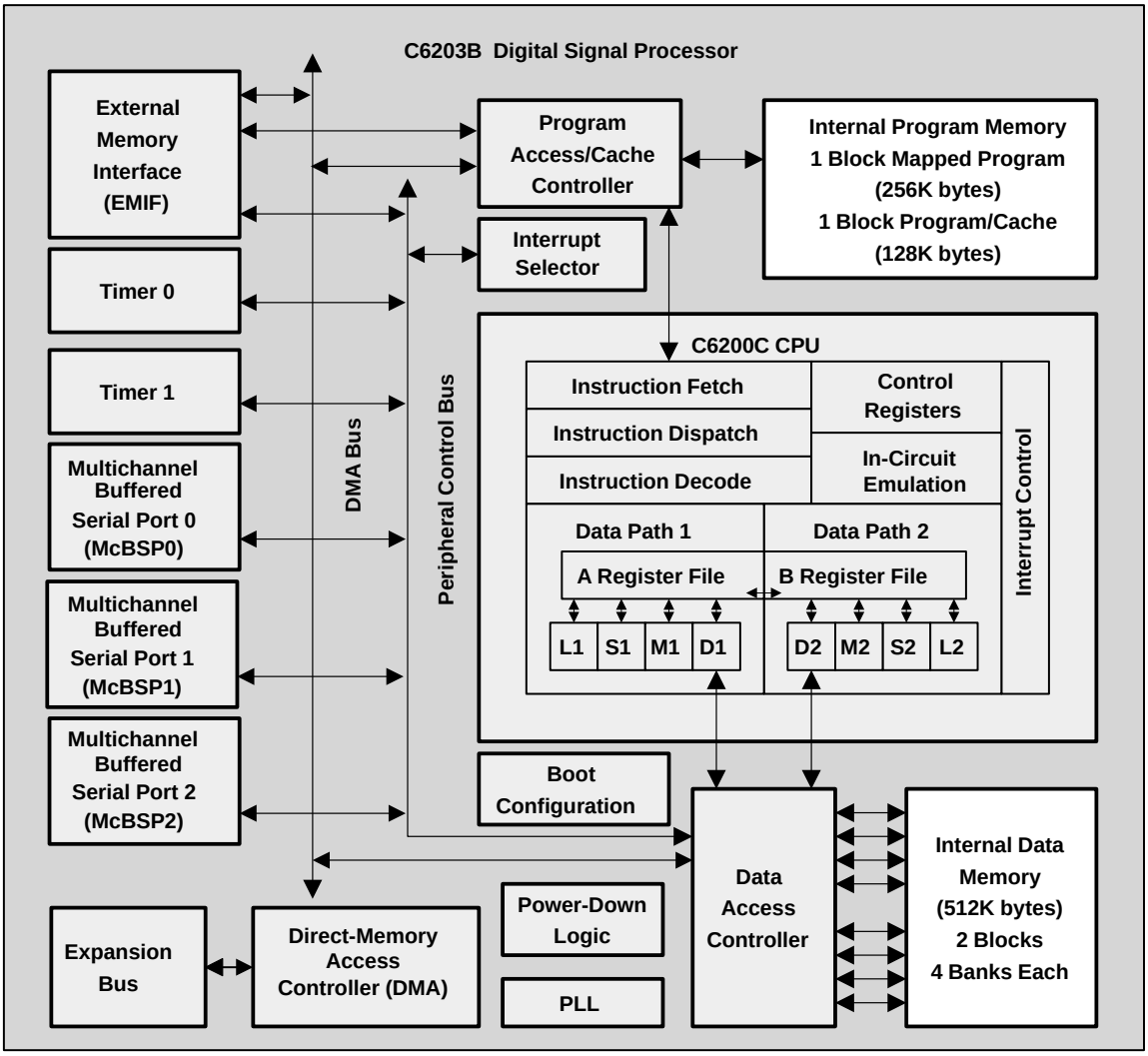

Figure 3. TMS320C6203B Digital Signal Processor

3.1 C6203B and C6202 DSP Similarities

The C6203B is highly compatible with the C6202. The following device components are identical between the devices:

- CPU: The CPU of the C6203B is identical to that of the C6202, which means that code written for the C6202 will run unmodified on the C6203B.
- Multichannel Buffered Serial Ports (McBSPs): The McBSPs are unchanged on the C6203B.
- Direct Memory Access (DMA) Controller: The DMA transfers data between any two locations in the memory map.
- 32-Bit Timers: These are unchanged on the C6203B.
- Interrupt Selection: There are 16 interrupt sources that may be used to interrupt the CPU or send an event to the DMA.
- External Memory Interface (EMIF): The 32-bit memory interface is unchanged on the C6203B.

- Expansion Bus (XB): The 32-bit XB is unchanged on the C6203B.
- Package Options: Both C6202 and C6203B offer two package choices – 27 mm sq. and 18 mm sq. BGA. The pin out for both packages has been preserved.
- Input/Output (I/O) Voltage Level: The I/O voltage remains unchanged at 3.3 V (but core voltage has changed, see section 3.2).

3.2 C6203B and C6202 DSP Differences

Several enhancements have been made to allow the C6203B for greater performance capability. These include:

- Faster Clock Rate: The maximum clock frequency has been increased from 250 MHz to 300 MHz. This increased frequency will allow the C6203B to achieve 2400 MIPS during operation.
- More PLL Multiply Options: In addition to x1 and x4 modes that already exist on the C6202, the C6203B features six additional PLL modes (x6, x7, x8, x9, x10 and x11) on the GLS 384-pin BGA package, and two additional PLL modes (x8, and x10) on the GJL 352-pin BGA package.
- Lower Power Consumption: The C6203B is manufactured using an improved process, resulting in a smaller die with lower power consumption, even as the internal memory has been increased from 3 Mb (384K bytes) to 7 Mb (896K bytes).
- Core Voltage Level: The core power supply has been reduced from 1.8 V to 1.5 V due to improved process technology. The I/O voltage remains unchanged at 3.3 V.
- Larger Internal Memory Spaces: The internal data and program memories have been significantly increased in size. The internal data memory has been increased fourfold, from 128K bytes on the C6202, to 512K bytes on the C6203B. Internal program memory has increased one and one-half times, from 256K bytes to 384K bytes. A 128K-byte block of the program memory is still selectable as program cache.
- Improved PLL: The PLL circuitry on the C6203B requires new component values for correct operation. These new components reduce the internal jitter. They can be found in Table 1.
- IBIS Modeling: C6203B Rev 3.x timing specifications take into account board-level constants, such as signal route delays. See the IBIS modeling section near the end of this application note for further details.

4 C6204 DSP

The Texas Instruments TMS320C6204 is an addition to the family of high-performance and flagship digital signal processors the TMS320C6000. (see Figure 1). The C6204 is derived from the C6202, and delivers 1600 MIPS at 200 MHz.

In addition to the CPU, many of the on-chip peripherals are common between C6000 devices. The C6204 derives its peripheral set from the C6202, and the internal memory architecture from the C6201.

Figure 4 illustrates a diagram of the C6204 DSP’s roadmap. Those blocks shaded gray are common to the C6202 and C6204.

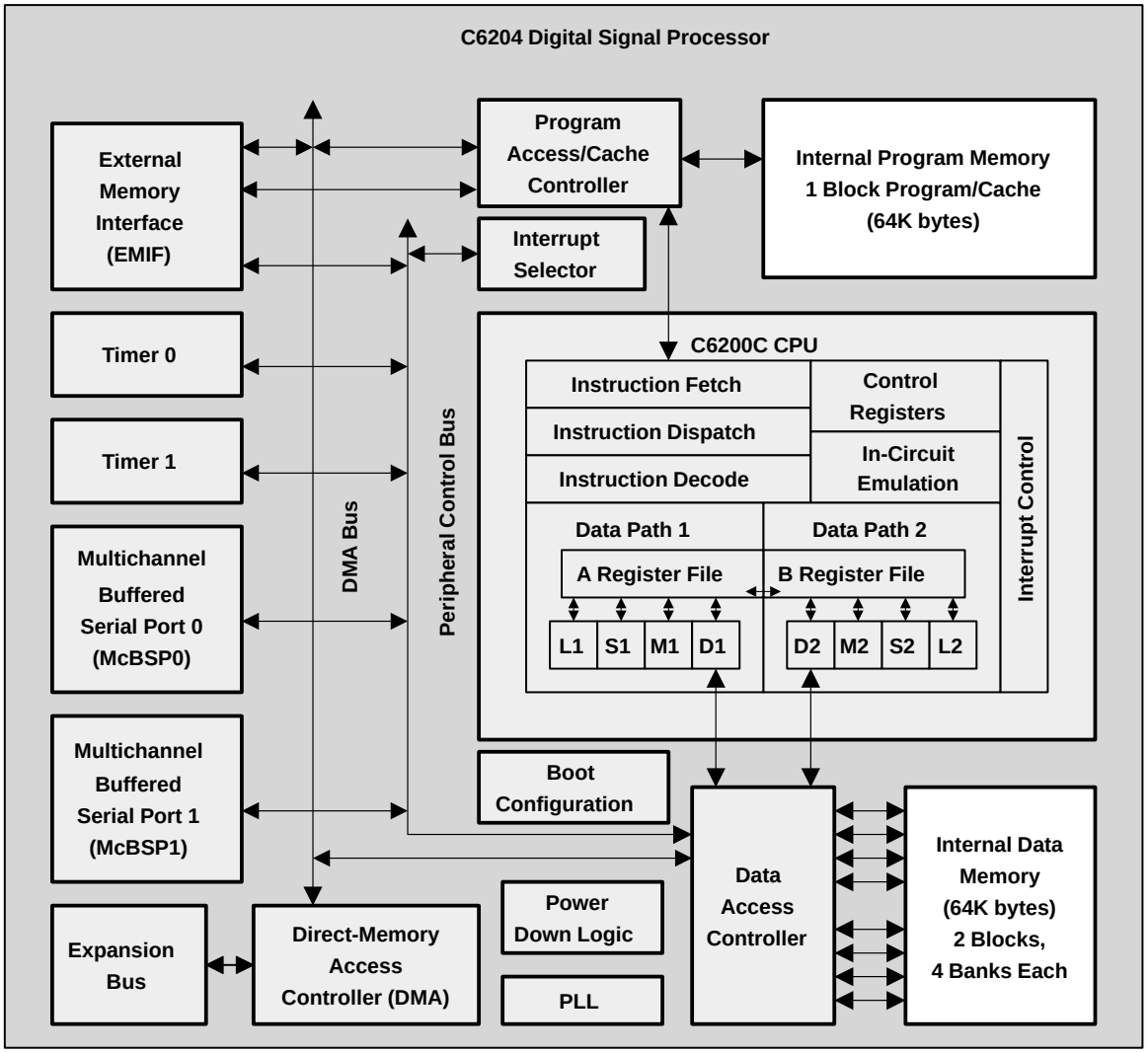

Figure 4. TMS320C6204 Digital Signal Processor

4.1 C6204 and C6202 DSP Similarities

The C6204 is highly compatible with the C6202. The following device components are identical between the devices:

- CPU: The CPU of the C6204 is identical to that of the C6202, which means that code written for the C6202 will run unmodified on the C6204.
- Direct-Memory Access (DMA) Controller: The DMA transfers data between any two locations in the memory map.
- 32-Bit Timers: These are unchanged on the C6204.
- Interrupt Selection: There are 16 interrupt sources that may be used to interrupt the CPU or send an event to the DMA.
- External Memory Interface (EMIF): The 32-bit memory interface is unchanged on the C6204.

- Expansion Bus (XB): The 32-bit XB is unchanged on the C6204.
- I/O Voltage Level: The I/O voltage remains unchanged at 3.3 V (but core voltage has changed, see section 4.2).

4.2 C6204 and C6202 DSP Differences

The following are the differences to keep in mind when migrating between the C6202 and C6204 devices.

- Internal Memory: The internal memory of the C6204 is similar to the C6201 with 64K bytes of program memory/cache and 64K bytes of data memory, organized as two blocks.
- Multichannel Buffered Serial Ports (McBSPs): The McBSP features are unchanged on the C6204. There are two McBSPs in C6204, whereas the C6202 has three.
- Package Options: The C6204 is available in the 18 mm sq. BGA package as well as a 16 mm sq. BGA package. The C6204 is pin-compatible with the 18 mm C6202 device. Note the different voltage levels on internal power supply – see below.
- Lower Power Consumption: The C6204 is manufactured using the improved 0.15 μm process, resulting in a smaller die with lower power consumption.
- Lower Core Voltage: The C6204 core voltage is 1.5 V, since it is manufactured in a smaller process technology (0.15 μm) than the C6202. The I/O supply remains unchanged at 3.3 V.

5 TMS320C6000 Code Compatibility

All C6000 devices are code-compatible with one another, the only exception being that there are some floating-point instructions that are only valid on the floating-point (TMS320C67x™) members. All of the TMS320C62x fixed-point devices are based on the same CPU core, designed to achieve high performance through increased instruction-level parallelism.

Surpassing the throughput of traditional superscalar designs, VelociTI™ provides eight execution units, including two multipliers and six arithmetic logic units (ALUs). These units operate in parallel, and can perform up to eight instructions during a single clock cycle—up to 2400 MIPS at 300 MHz.

VelociTI's advanced features include instruction packing, conditional branching, variable-width instructions, and pre-fetched branching, all of which eliminate problems that were previously associated with VLIW implementations. The architecture is highly deterministic, with few restrictions on how or when instructions are fetched, executed, or stored. This architectural flexibility is key to the breakthrough efficiency levels of the C6000 compiler.

This common architecture allows designers to begin development with existing C6000 software tools for those devices currently in development. This also allows for migration from one C6000 processor to another, as design requirements necessitate.

TMS320C67x is a trademark of Texas Instruments.

5.1 Writing Code for the C6202/02B/03B/04

The identical CPUs in the C620x devices allow for code to be written for the C6202/02B/03B/04 using existing C6000 tools. C6201 CPU code will require no modification to use on the C6202, C6202B, C6203B, and C6204. All peripheral-specific code, with the exception of the expansion bus, will also be able to run unchanged on the C6202.

Note that the C6202, C6202B, C6203B, and C6204 share the same peripheral set (except that the C6204 has one less McBSP); therefore, the peripheral-specific code is also compatible between these devices.

The C6000 compiler may be used for all members of the C6000 device platform. Fixed-point devices are object-code compatible, so code written for the C6201 may be used for the new devices.

Code development for the C6000 family may begin using the fast C6000 simulator. The simulator provides a cycle-accurate accounting of device performance, assuming that all on-chip memory is used for code and data. The simulator provides a good environment to learn the C6000 VLIW architecture.

The standard C6000 simulator may be used to incorporate peripheral support. C6000 designs may be worked out in detail on the simulator prior to purchasing actual silicon, with cycle-accurate accounting of peripherals' performance.

For a development start in hardware, the C6201 EVM may be used to understand the C6000 functionality. With the exception of the expansion bus, all of the peripherals on the C6202, C6202B, C6203B, and C6204 are identical to those of the C6201, so the EVM is a good tool to understand how to incorporate the peripherals into a real-time system.

Performance will significantly improve when migrating from the C6201 to the C6202, C6202B, C6203B, and C6204, due to the combination of increase in on-chip memory locations, faster clock, more advanced process technology, and the addition of the 32-bit expansion bus (XB).

For systems that have already been designed using the C6202, the same code can be used to run on the newer C6202B, C6203B, and C6204. Note that the C6204 has an internal memory size (64-KB Program and 64-KB Data memory) similar to the C6201 and, hence, the code that may have occupied the complete memory space of the C6202 may have to be partly placed in external memory.

Using these development platforms, as well as the C6000 literature currently available, will enable C6202, C6202B, C6203B, C6204 systems to be completed in a timely manner.

5.2 Designing C6203 Software for Memory-Map Compatibility

While the address ranges of the added program and data memory to the C6203B completely overlap the corresponding smaller C6202 blocks, the block assignments within the larger memory ranges have changed. Memory locations previously located in one block on the C6202 can now end up in another block if the same software is executed on the C6203B .

To review, each internal program and data space is split between two blocks. This feature allows the CPU to be executing program from one of the blocks, while the DMA is simultaneously loading the next segment of the code into the other block, with an assurance of no memory conflicts and resulting lost cycles. Similarly, both sides of the CPU assure simultaneous access of internal data, without any conflicts, provided each side uses a different memory block.

Since the C6203B memory map is a superset of the C6202 memory, the C6202 code will run on the C6203B without modification. However, if the original code used blocking to minimize memory-access conflicts, in order to preserve the original blocking intent, the logical to physical memory mapping must be changed at the linker level. Depending on the application, this may not be necessary, as any cycles lost due to increased memory conflicts may be negated by the higher operating frequency of the C6203B devices.

5.3 Designing C6204 Software for Memory-Map Compatibility

The internal memory configuration of the C6204 is similar to the C6201, so any programs written for the C6201 do not require any changes, and no special considerations are necessary.

When migrating from C6202/02B/03B to C6204, a revision of memory locations is required because the C6204 internal memory-map size has been reduced in different sections when compared to these other members of the C6000 platform.

6 TMS320C6202/03/04 Hardware Compatibility

The C6202, C6202B, C6203B, and C6204 are pin-compatible devices, thus making new system designs easier and providing faster time to market. As a quick reference, Table 1 lists the differences between these devices.

Table 1. TMS320C6202/02B/03B/04 Comparison Chart

Hardware Feature	C6202	C6202B	C6203B	C6204
Package	27 mm x 27 mm (352-pin BGA (GJL)) 18 mm x 18 mm (384-pin BGA (GLS))	27 mm x 27 mm (352-pin BGA (GNZ)) 18 mm x 18 mm (384-pin BGA (GNY))	27 mm x 27 mm (352-pin BGA (GNZ)) 18 mm x 18 mm (384-pin BGA (GLS) and GNY)	16 mm x 16 mm (288-pin BGA (GHK)) 18 mm x 18 mm (384-pin BGA (GLW))
Peripheral	3 McBSPs	3 McBSPs	3 McBSPs	2 McBSPs
On-chip memory	256-KB Program, 128-KB Data	Same as C6202	384-KB Program, 512-KB Data	64-KB Program, 64-KB Data
Speed (MHz)	200–250	250–300	250–300	200
Core/(I/O) voltage	1.8 V/3.3 V	1.5 V/3.3 V	1.5 V/3.3 V	1.5 V/3.3 V
PLL options	GJL: Bypass, x4 GLS: Bypass, x4	GNZ: Bypass, x4, x8, x10 GNY: Bypass, x4, x6, x7, x8, x9, x10, x11	x4 GNZ: Bypass, x4, x8, x10 GNY: Bypass, x4, x6, x7, x8, x9, x10, x11	Bypass, x4
PLL components	R1 → 60.4 Ω C1 → 27 nF C2 → 560 pF	R1 → 45.3 Ω C1 → 47 nF C2 → 10 pF	Rev 1.x: Same as C6202 Rev 2.x and 3.x: Same as C6202B	Same as C6202
JTAG ID	2005602F	2005602F	3005D02F	1005E02F
CPU ID	0002	0003	0003	0003

6.1 PLL Options on the TMS320C6202/02B/03B/04

Various PLL options exist for the TMS320C6202/02B/03B/04 devices depending on the packages. Table 2 shows which pins select the various PLL modes for the different packages.

It is important that the crystals have sockets in your board design, so that moving to any of the C6202, C6202B, C6203B, or C6204 makes it easier to utilize the benefits of the different PLL multiply options. The new multiply options such as the x6, x7, x8, x9, x10, and x11 makes the design cheaper, by allowing the use of low-frequency crystals.

Table 2. TMS320C6202/02B/03B/04 PLL Multiply and Bypass (x1) Options

Device	GJL or GNZ Package (27 mm sq. 352-pin BGA)		GLS or GNY Package (18 mm sq. 384-pin BGA)		GHK Package (16 mm sq. 288-pin BGA)
C6202 (GJL and GLS)	CLKMODE[0]	Mode	CLKMODE[2:0]	Mode	Not applicable
	0	x1	XX0	x1	
	1	x4	XX1	x4	
C6202B (GNZ and GNY)	CLKMODE[1:0]	Mode	CLKMODE[2:0]	Mode	Not applicable
	0	x1	000	x1	
	1	x4	001	x4	
	10	x8	010	x8	
	11	x10	011	x10	
			100	x6	
			101	x9	
			110	x7	
			111	x11	
C6203B (GNZ and GNY) (see Notes 1, 3)	CLKMODE[1:0]	Mode	CLKMODE[2:0]	Mode	Not applicable
	00	x1	000	x1	
	01	x4	001	x4	
	10	x8	010	x8	
	11	x10	011	x10	
			100	x6	
			101	x9	
			110	x7	
			111	x11	

Table 2. TMS320C6202/02B/03B/04 PLL Multiply and Bypass (x1) Options (Continued)

Device	GJL or GNZ Package (27 mm sq. 352-pin BGA)	GLS or GNY Package (18 mm sq. 384-pin BGA)		GHK Package (16 mm sq. 288-pin BGA)	
		CLKMODE[0]	Mode	CLKMODE[0]	Mode
C6204 (GLS and GHK) (see Note 2)	Not applicable	0	x1	0	X1
		1	x4	1	X4

NOTES: 1. The C6202B and C6203B come in a GNY package. The GNY package is an 18 mm plastic, molded package with the same pin configuration as the GLS package.
2. C6204 GLW package is a subset of the GLS package used on the C6202 devices. The GLW package is compatible with the GLS package, with the inner row of core supply and ground pins removed (see TMS320C6204 data sheet for more details).
3. The GNZ package is a 27 mm plastic molded package, with the same pin configuration as the GJL package.

The 18 mm x 18 mm GLS and GNY packages for the C6202/02B/03B/04 are fully pin-compatible. The pins that select the new PLL modes on the C6202B, and C6203B are unconnected (UC), or don't cares, on the C6202 and C6204. This is shown in Table 3. Thus, a C6202B/C6203B will have the capability of selecting between the x1 and x4 modes if placed in a C6202-based board. The C6202B and C6203B have similar PLL modes for each package type, as shown in Table 4. The converse is also true. An 18 mm sq. GLS package C6202 can be placed in a similar package C6202B/03B board for full operation.

Table 3. TMS320C6202/02B/03B/04 CLKMODE Pin Compatibility for GLS Package (GNY Package for C6203B, GLW Package for C6204) (18 mm sq. 384-pin BGA)

PLL Selection Pins	C6202	C6202B	C6203B	C6204
CLKMODE[0] Pin B12	√	√	√	√
CLKMODE[1] Pin A9	UC	√	√	UC
CLKMODE[2] Pin A14	UC	√	√	UC

Table 4. TMS320C6202/02B/03B CLKMODE Pin Compatibility for GJL and GNZ Packages (27 mm sq. 352-pin BGA)

PLL Selection Pins	C6202	C6202B	C6203B
CLKMODE[0] Pin B15	√	√	√
CLKMODE[1] Pin C11	GND	√	√
CLKMODE[2]	Does not exist	Does not exist	Does not exist

For the case of 27 mm sq. GJL package, the CLKMODE[1] pin that selects the additional new modes (see Table 2) on C6202B. It is a ground pin on the C6202, as shown in Table 4. Thus a C6202B will have the capability of selecting between the x1 and x4 modes if placed in a C6202 socket.

CAUTION:

If a C6202 is placed in a C6202B/03B board with the CLKMODE[1] pin pulled to the non-default state (default is GND), there will be current drawn through the pullup (3.3 V/20K or 165 uA). If a C6202 is placed in a C6202B/03B board with the pins directly to the V_{CC} plane for the new modes, there will be a ground/power short through the package.

6.2 Power Supply Considerations

All C6000 devices require two voltage levels to power the device. They are the core voltage and I/O voltage. The I/O voltage remains the same at 3.3 V across all these devices. The core voltage reduces as better process technologies are used for fabrication. The core voltage of the C6202 is 1.8 V, since it uses the 18C05 or 0.18 μm process technology. Because the C6203B/04 is manufactured using a better (0.15 μm) process technology (15C05), it requires a 1.5 V core voltage.

An existing C6202 board can easily be migrated to the C6202B, C6203B, or C6204 by changing/removing (as applicable) the resistors of the power supply module used, or if a programmable power supply module is used, the output voltage of such a module can be changed by programming the pins to a 1 or 0, as required. Some example application notes for power sequencing and power supply design can be found on the TI web site at http://www.ti.com

7 Designing to Achieve Performance With the C6202/02B

The enhancements made to the design of the C6201 allow the C6202 to offer twice the system I/O, and 25 percent higher performance in fixed-point MIPS. The improved performance of the CPU comes in part from the increased device clock rate of 250 MHz, allowing for 2000 MIPS, but primarily from the additional internal memory and the new expansion bus.

The C6202 offers three times the internal memory space of the C6201, with 256K bytes of program memory and 128K bytes of data memory. By providing more on-chip memory, designers will be able to keep more critical code sections and data in fast, quick-access memories. This will allow the CPU to maintain its high performance capability of 2000 MIPS over a wide range of applications.

The internal program memory of the C6202 is divided into two 128K-byte blocks. One block is configured as either mapped RAM or as cache, with the other fixed as mapped RAM. This option allows for critical code to stay in internal memory, while still having the added performance and flexibility of cache. If the program space is configured entirely as RAM, the dual-block structure allows for the DMA to transfer new sections of code into one block while the CPU is running from the other. This provides system designers with a means to easily schedule their own program-paging scheme.

The internal data memory of the C6202 is configured as it is on the C6201, with two blocks of four 16-bit banks each. Each bank is accessible by either the CPU or the DMA during each cycle. The dual-bank structure of the data memory allows the CPU to operate on a set of data in one block while the DMA transfers new data into and old data out of the other block. This reduces the opportunity of contention between the CPU and DMA for data memory resource.

The 32-bit expansion bus replaces the host port interface (HPI) of the C6201 and provides the C6202 with an additional interface to peripheral I/O devices. There are four separate memory spaces, as in the EMIF, each of which is independently configured using space control registers. The expansion bus has two host-interface modes: synchronous and asynchronous. The asynchronous mode is simply a 32-bit version of the C6201 HPI. The synchronous mode allows the expansion bus to interface to several industry-standard bus protocols. The expansion bus may run at speeds up to one-fourth the CPU speed (62.5 MHz, in the case of a 250 MHz–6202) when servicing a synchronous host. Possible synchronous host interfaces include:

- Master/slave interface to PCI bridge
- Slave interface to industry-standard synchronous bus protocols

The asynchronous memory interface of the expansion bus is identical to that of the EMIF, with the exception that the addressable space is limited. The expansion bus has the advantage over the EMIF of also supporting a glueless synchronous FIFO interface. The advantage here is that slower peripheral I/O devices are decoupled from the faster memories that are typically attached to the EMIF, and by splitting the external devices between two buses, system loading is minimized.

The expansion bus is independent of the EMIF, so both may be accessed simultaneously. It is possible to have the CPU making program fetches from SDRAM via the EMIF while the DMA is continuously servicing a synchronous FIFO on the expansion bus. This feature significantly increases the possible data throughput of the device.

8 Designing to Achieve Performance With the C6203B

The enhancements made to the successful design of the C6202 allow the C6203B to offer 20 percent higher performance in fixed-point MIPS. The improved performance by the CPU comes in part from the increased device clock rate of 300 MHz, and from the additional internal program and data memory.

The C6203B offers more than double the internal memory space of the C6202, with 384K bytes of program memory and 512K bytes of data memory. By providing more on-chip memory, designers will be able to keep more critical code sections and data in fast, quick-access memories. This will allow the CPU to maintain its high performance capability.

The 384K-byte internal program memory of the C6203B is divided into a 256K-byte, memory-mapped block and a 128K-byte direct-mapped block. The 128K-byte block can be configured as either RAM or cache, and the 256K-byte block fixed as RAM. This option allows for critical code to stay in internal memory, while still having the added performance and flexibility of cache. If the program space is configured entirely as RAM, the dual-block structure allows for the DMA to transfer new sections of code into one block, while the CPU is running from the other. This will provide system designers with a means to easily schedule their own program-paging scheme.

Note that while the address ranges of the added program and data memory to the C6203B completely overlap the corresponding smaller C6202 blocks, the block assignments within the larger memory ranges have changed. Memory locations previously located in one block on the C6202 can now end up in another block, if the same software is executed on the C6203B.

The internal program memory is split into two blocks. This feature allows the CPU to be executing program from one of the blocks, while the DMA is simultaneously loading the next segment of the code into the other block, ensuring no memory conflicts and resulting lost cycles. Similarly, both sides of the CPU ensure simultaneous access to internal data without any conflicts, as long as each side uses a different memory block.

Since the C6203B memory map is a superset of the C6202 memory, the C6202 code will run on the C6203B without any modifications. However, if the original code used blocking to minimize memory access conflicts, in order to preserve the original blocking intent, the logical to physical memory mapping may have to be changed at the linker level. Depending on the application, this may not be necessary, as any cycles lost due to increased memory conflicts may be negated by the higher operating frequency of the C6203B device.

9 Designing to Achieve Performance With the C6204

Enhancements and modifications to the design of the C6202 provide for a low-cost C6204. The C6204 provides performance on the order of 1600 MIPS at 200 MHz. Since the C6204 is a low-cost device among the C620x generation, it offers the memory architecture of the C6201, but with a better process (15C05) technology. In addition, it provides a two-fold increase in bandwidth compared to the C6201, due to the 32-bit expansion bus.

The internal program memory of the C6204 contains 64K bytes of RAM, which can be configured as either mapped RAM, or as cache similar to the C6201. The internal data memory of the C6204 is again configured as it is on the C6201, with two blocks of four 16-bit banks. Each bank is accessible by either the CPU or the DMA during each cycle. The dual-bank structure of the data memory allows the CPU to operate on a set of data in one block, while the DMA transfers new data into and old data out of the other block. This reduces the opportunity of contention between the CPU and DMA for data memory resource.

The 32-bit expansion bus replaces the Host Port Interface (HPI) of the C6201, and provides the C6204 with an additional interface to peripheral I/O devices. There are four separate memory spaces, as in the EMIF, each of which is independently configured using space-control registers. The expansion bus has two host-interface modes: synchronous and asynchronous. The asynchronous mode is simply a 32-bit version of the C6201 HPI. The synchronous mode allows the expansion bus to interface to several industry-standard bus protocols. The expansion bus may run at speeds up to one-fourth the CPU speed (in the case of the C6204, 50 MHz) when servicing a synchronous host. Possible synchronous host interfaces include:

- Master/slave Interface to PCI bridge
- Slave interface to industry-standard synchronous bus protocols

The asynchronous memory interface of the expansion bus is identical to that of the EMIF, with the exception that the addressable space is limited. The expansion bus has the advantage over the EMIF of also supporting a glueless synchronous FIFO interface. The advantage here is that slower peripheral I/O devices are de-coupled from the faster memories that are typically attached to the EMIF, and by splitting the external devices between two buses, system loading is minimized.

The expansion bus is independent of the EMIF, so both may be accessed simultaneously. It is possible to have the CPU making program fetches from SDRAM via the EMIF while the DMA is continuously servicing a synchronous FIFO on the expansion bus. This feature significantly increases the possible data throughput of the device.

10 C6203B AC Timing Changes

The C6203B revision 3.x and C6202B EMIF timing parameters have been improved, eliminating possible speed issues observed on former revisions. They provide the capability to transfer data to the latest high-speed memories with excellent throughput.

C6203B/C6202B offer high-performance communication with external SDRAMs and SBSRAMs, as well as other asynchronous memories.

The C6203B revision 3.x and C6202B EMIF timings were generated based on IBIS models as well as real application board routings. These timings more accurately represent typical setup and hold times generated from board layout. IBIS models should be used to verify that board trace length/routings do not cause setup and hold time requirements to go beyond the device specifications.

11 IBIS Modeling for the C6202B and C6203B Revision 3

Care must be taken when routing clock, control, and data lines between high-speed interfaces on the DSP. IBIS models should be used to account for board topology. In order to meet the requirements of the latest high-speed memories and other I/O devices, C6202B and C6203B Revision 3 timings were designed to account for these board-level constants.

Constraints are placed on the distance that trace lengths can be. This constraint on trace length results in an increased window between setup and hold times. Figure 5 shows how to determine the required setup and hold times based on board route delays.

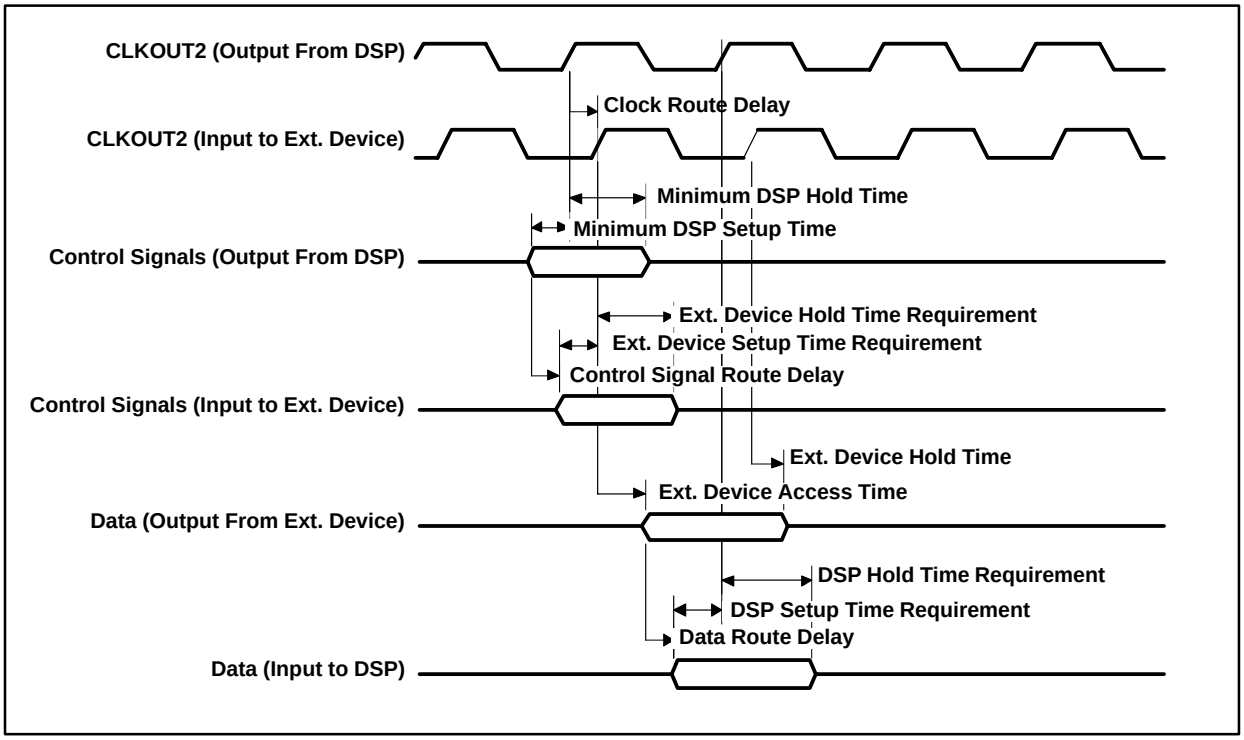

Figure 5. DSP Target Device Perception of Board Delays

Route delays are caused by a combination of trace impedance and trace length. Signals, depending on medium, have typical propagation times on the order of 180 pS/inch. Other factors, such as driver characteristics and loading also impact the route delays seen at the EMIF interface. Typical loading for a single SDRAM is on the order of 5pF. Lighter loading results in faster rise/fall times; conversely, heavier loading produces slower rise/fall times. The more devices on the EMIF bus, the higher the loading.

To assist in the design of C6202B and C6203B Revision 3-based systems, board-level issues were taken into account when specifying EMIF timing parameters. By using typical board impedances and trace lengths, critical timing windows (the period from setup to hold) more accurately reflect real operating conditions. The application report, *Using IBIS Models for Timing Analysis* (SPRA839), presents a detailed explanation how to use the IBIS models in order to perform accurate timing analysis for a given system. This methodology is valid for all C6000 platform devices. This application report includes an example of how to compute margins for setup and hold timings.

12 C620x Important Considerations

The *TMS320C6000 Peripherals Reference Guide* (SPRU190) includes several recommended usage conditions for C6000 devices. If these considerations are not followed on a design, the DSPs will behave unpredictably.

In the case of the C620x devices, specifically the C6202B, as well as the C6203B on revisions 2.5 and 3.0, if the devices are programmed outside of the conditions stated on the PRG, they will not operate correctly.

Typical exampes of these rules that need to be followed are:

- External host accesses the last two words in internal data RAM (IDRAM)

  When the XBUS is in auto-increment mode (AINC=0), if an external host attempts to access the last two word locations (0x8007FFF8 and 0x8007FFFC) in the Internal Data RAM, the operation is undefined. This is due to the DSP trying to pre-fetch data from reserved memory locations .See the *TMS320C6000 Peripherals Reference Guide* (SPRU190).

- DMA accesses only one RAM block at a time

  For the C6202B/03B, the DMA can only access one of the two blocks of RAM at a time. The CPU and DMA can access the internal RAM, without interference, as long as each accesses a different block. The DMA cannot cross between Block 0 and Block 1 in a single transfer. Separate DMA transfers must be used to cross block boundariies. See the *TMS320C6000 Peripherals Reference Guide* (SPRU190).

TI encourages our customer base to follow the PRG recommendations to ensure the operational features of the C620x DSPs.

13 C6000 Tools Support

C6000 tools are available now for use in all C6000 designs. The C6000 development tools available today are:

- Code Composer Studio™, which includes Code Composer Studio Compile Tools and Code Composer Studio Debug Tools
- C6000 Simulator Software
- C6000 Optimizing C Compiler/Assembler
- TMS320C6201 Evaluation Module (EVM)
- XDS510™ C6000 C Source Debugger Software
- XDS510 Emulator Hardware With JTAG Emulation Cable

14 C6000 Literature Available

A great deal of literature is available today for the C6000 devices:

1. *TMS320C6000 CPU and Instruction Set Reference Guide* (SPRU189).
2. *TMS320C6000 Peripherals Reference Guide* (SPRU190).
3. *TMS320C6000 Technical Brief* (SPRU197).
4. *TMS320C6000 Programmer's Guide* (SPRU198).
5. *TMS320C62x Multichannel Evaluation Module Reference Guide* (SPRU308).
6. *TMS320C6x Peripheral Support Library Programmer's Reference* (SPRU273).
7. *TMS320C6000 Assembly Language Tools User's Guide* (SPRU186).
8. *TMS320C6000 Optimizing C Compiler User's Guide* (SPRU187).
9. *TMS320C6x C Source Debugger User's Guide* (SPRU188).
10. *TMS320C6x C Source Debugger For SPARC* (SPRU224).
11. *Using IBIS Models for Timing Analysis* (SPRA839).

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