TMS320C6474 DDR2 Implementation Guidelines

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ABSTRACT

This document provides implementation instructions for the DDR2 interface contained on the C6474 DSP.

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1 Prerequisites

1.1 High Speed Design

While the goal of the C6474 collateral is to make system implementation easier for the customer by providing the system solution, it is still expected that the PCB design work is to be supervised by a knowledgeable high-speed PCB designer as an assumption is made that the PCB designer is using established high-speed design rules. Ground plane cuts should be avoided, if at all possible, as they are tricky to do correctly. Due to PCB design, crosstalk and EMI impacts should be evaluated as the PCB design progresses because it can be difficult to go back and fix issues later. Thorough planning aids in the design cycle.

1.2 Familiarity With the JEDEC DDR2 Specification

The DDR2 interface on the C6474 device is designed to be compatible with the JEDEC JESD79-2B DDR2 specification. It is assumed that the reader is familiar with this specification and the basic electrical operation of the interface. In addition, several memory manufacturers provide detailed application reports on DDR2 operation.

2 C6474 DDR2 Supported Devices

The C6474 DDR2 interface supports JEDEC DDR2 ×16 devices. Supported densities are 256 Mb, 512 Mb, 1 Gb, and 2 Gb in the ×16 device width. Any JEDEC DDR2-667 speed grade device at these densities in the ×16 width should work with the C6474 device's DDR2 controller at 333-MHz clock speed/667-M data rate.

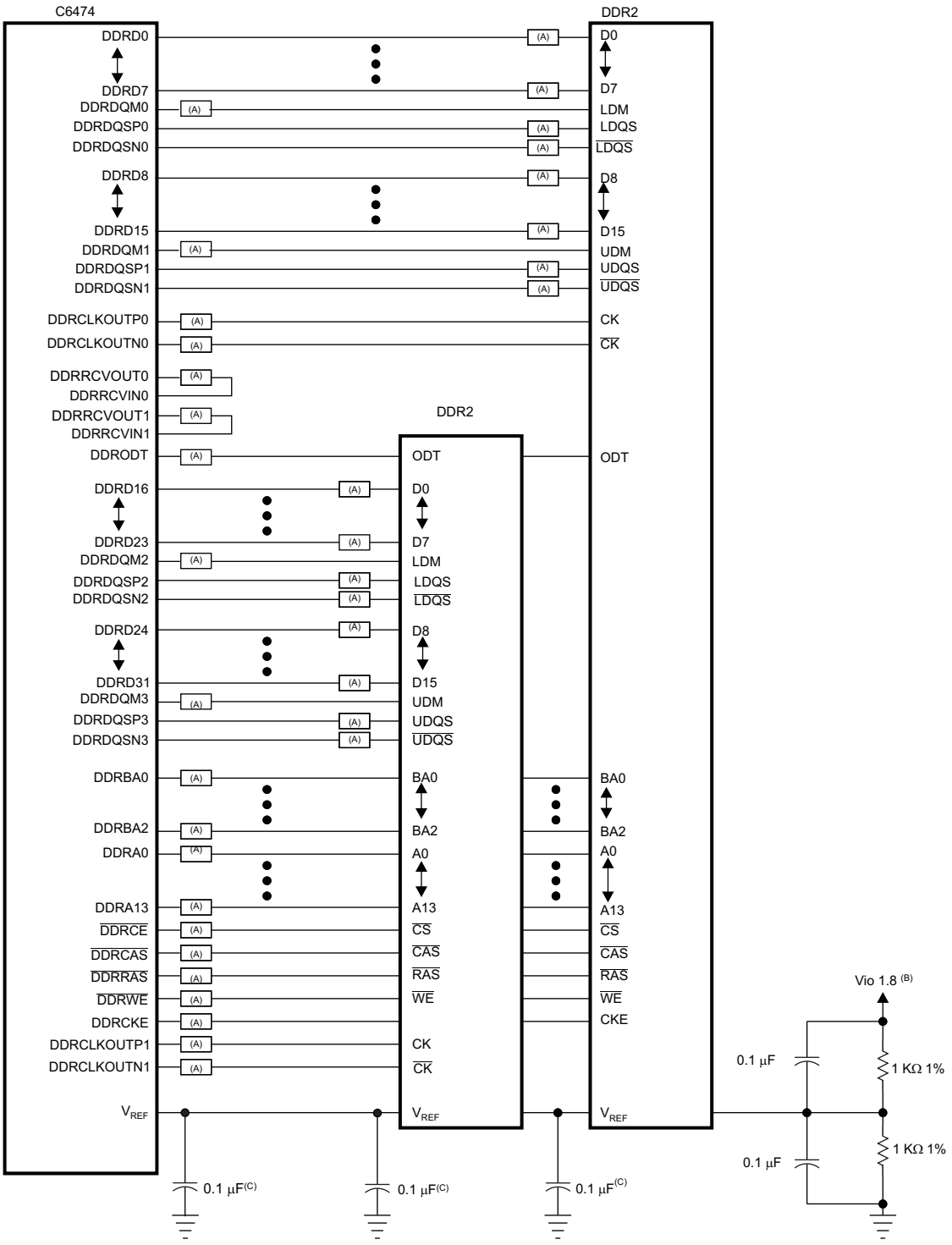
TI is working with specific DDR2 manufacturers/devices. The following JEDEC DDR2 compatible devices are recommended:

- MT47H64M16BT-3 – Micron 1 Gb DDR2-533 92-ball package
- MT47H128M16HG-3 - Micron 2 Gb DDR2-533 84-ball package
- MT47H32M16CC-3 – Micron 512 Mb DDR2-533 84-ball package
- MT47H16M16BG-3 – Micron 256 Mb DDR2-533 84-ball package

Note that the 84- and 92-ball DDR2 BGA packages are electrically compatible. The additional 8 balls on the 92-ball package are support balls only. The provided DDR2 layout provides room for these support balls.

3 Schematics and Electrical Connections

Figure 1 shows a high-level schematic of the DDR2 interface. The 32-bit DDR2 interface of the C6474 device is connected to two 16-bit DDR2 devices; therefore, the address and control connections are three-point nets and the data lines are point-to-point nets. Two sets of clock outputs are provided to support a single load for clocks. These two sets of outputs are identical.



A Terminator, if desired. See terminator comments.

B Vio 1.8 is V_{REF} the power supply for the DDR2 memories and DSP DDR2 interface.

C One of these capacitors can be eliminated if the divider and its capacitors are placed near a device pin.

Figure 1. C6474 DDR2 High-Level Schematic

3.1 DDR2 Power Supplies

The power supply for the DDR2 interface is 1.8 V ±5%. This power supply is used for the C6474 DDR2 power pins (DV_{DD18}) as well as the JEDEC DDR2 devices. V_{REF} is derived from the DDR2 power supply via a resistive divider (1% or better tolerance components).

3.2 EMI-Limiting Signal Terminations

Series terminations on the PCB (as shown in note A of Figure 1 above) allow the DDR2 signals to be tuned to meet EMI certification requirements. A PCB that fails EMI certification without series terminations likely has to be re-spun in order to address the EMI shortcomings. It can take multiple PCB spins to correct EMI issues. Note that re-spinning a dense non-terminated PCB layout to include terminators can be a very difficult effort because physical room must be made for the terminations. This means an entire PCB design may have to be redone. It is much easier to remove terminations rather than adding them after the PCB has been found to fail EMI.

Customers who are sensitive to the cost/schedule issues with respect to EMI may wish to include terminations on their boards even though they plan not to have terminations on the final product. This way, the terminations can easily be replaced with zero-Ω resistors and checked for EMI compliance. If the PCB fails EMI, it is then possible to install the necessary terminations without re-spinning the PCB. Once the termination scheme has been verified to pass EMI, the remaining zero-Ω terminations can be carefully removed from the PCB layout in a single PCB design spin.

Simulations have been completed with 22-Ω series terminations and these are currently recommended for all systems that operate at full speed (DDR2-667).

The C6474 DDR2 interface does not require series terminations to meet overshoot requirements, but the DDR2 memories must be operated in reduced strength mode to guarantee this. Reduced strength mode is described in Section 3.5.

3.3 Slew Rate Control

The C6474 device has two slew rate settings that are controlled by the DDRSLRATE input pin. This pin needs to be pulled low or high at all times (it is not latched). Pulling the DDRSLRATE input pin low selects the normal slew rate. If DDRSLRATE is pulled high, the slew rate is reduced by 33%. For normal, full-speed operation, the DDRSLRATE should be pulled low.

3.4 PTV-Compensated Output Impedance

The C6474 device has programmable process, voltage, and temperature (PVT) compensated DDR2 I/O impedances, similar in concept to the ODT implemented in the attached DDR2 memory devices. These PVT buffers are dynamically compensated across process, voltage, and temperature to provide a stable I/O impedance across all operating conditions.

The C6474 devicehas a training resistor of 45.3-Ω 1% tolerance and must be attached to the RSV03 pin and GND for the PVT-compensated DDR2 I/O to function properly. Along with this PVT training resistor, the C6474 device DDR2 PVT Control Register (DDR2PVTCNTL) must be programmed to 0x1, or "half-termination" for the PVT-compensated DDR I/O to function properly.

For more information about the DMCCTL register, see *TMS320C6474 DSP DDR2 Memory Controller User's Guide* (SPRUG19).

The PVT-compensated impedance (when correctly set to the "half" setting) results in close to 90 Ω of impedance on the DDR2 I/O during a READ cycle (SDRAM → DSP). Otherwise, the terminations on the C6474 device are disabled.

3.5 Memory Device ODT Settings

On-die terminations (ODT) should be enabled for the attached DDR2 memory devices. The DDR2 memory devices ODT should be set to 75 Ω. The DDRODT signal goes logic "high" to enable the ODT in attached DDR2 memory devices during memory write cycles to the attached DDR2 memory. The DDRODT signal goes logic "low" to disable the ODT in attached DDR2 memory devices during memory read cycles to the attached DDR2 memory.

The memory device's ODT settings are programmed through the DDR2_TERM[1:0] bits of the SDCFG register on the C6474 device. For more details on the DDR2 memory device ODT configuration, see the *TMS320C6474 DSP DDR2 Memory Controller User's Guide* (SPRUG19).

3.6 Memory Device Drive Strength

DDR2 memory devices have two drive strength settings: normal and reduced (60%) drive strength. The reduced drive strength setting should be used to help meet EMI regulations. For details on how to set the memory device drive strength, see the *TMS320C6474 DSP DDR2 Memory Controller User's Guide* (SPRUG19).

4 Stack Up

TI has simulated, and recommends, single-ended controlled impedance traces with a nominal characteristic impedance of 50 Ω ±10% for all DDR2 signals.

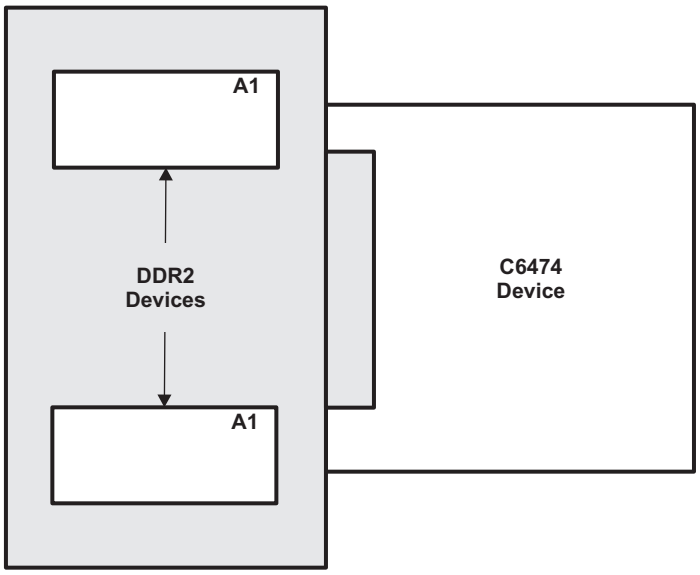
4.1 Ground Reference Planes

It is critical that all signal routing layers have a ground reference plane; meaning that there is a full, contiguous ground plane next to every DDR2 routing layer. Two routing layers can share a ground plane (one signal layer above and one signal layer below the ground plane). Ground plane cuts are not allowed in the DDR2 region. These cuts are generally a bad idea. They should be done very carefully and only if absolutely necessary on other areas of the PCB. The purpose of the ground plane is to provide a path for return currents to minimize crosstalk and EMI. Power planes cannot be used as signal returns for the DDR2 interface. *Improper ground plane stack up will likely cause the DDR2 interface to fail or operate unreliably.*

5 Placement

5.1 DDR2 Placement and Keep Out Region

Figure 2 shows an example DDR2 placement with a keep-out region. This keep-out region varies with the individual design. Its purpose is to ensure that other signals do not interfere with the DDR2 interface. The only signals allowed in the region of the DDR2 signal layers are those for this interface. The 1.8-V power partial plane should encompass at least the entire DDR2 keep out region.



A Example DDR2 keep-out region: Region should encompass all DDR2 circuitry and varies depending on placement. Non-DDR2 signals can be routed in this region provided they are routed on layers separated from DDR2 signal layers by a ground layer. No breaks are allowed in the reference ground layers in this region. In addition, the 1.8-V power plane should cover the entire keep out region.

Figure 2. DDR2 Placement and Keep Out

5.1.1 Resistors and Resistor Packs

The C6474 DDR2 interface uses resistors for V_{REF} generation and can use resistors or resistor packs for signal terminations. Specific placement requirements for these components are specified by the routing rules for V_{REF} and the other net classes of the interface. These routing rules are presented in Section 6.2.

Generally speaking, termination resistors can be either discrete resistors or resistor packs and they are placed between the DDR2 memories and the C6474 device. The V_{REF} divider resistors are placed somewhere between the DDR2 devices and the C6474 device.

6 Routing

6.1 Required PCB Feature Sizes

The minimum PCB feature sizes referenced in this document are the largest that can be accommodated in order to physically route the PCB due to the size of the BGA packages. Smaller feature sizes can also be used to improve PCB density as long as the routing rules are followed.

The PCB routing rules in this document assume a minimum PCB route width and spacing of 5 mils. The PCB route trace width is defined as w for the purposes of defining minimum trace separation for the various net classes discussed later in the routing rules. Therefore, if the PCB is designed with the widest possible traces, then the trace width is w = 5 mils.

Recommended pad stacks for the DDR2 and C6474 BGA pads are 14-mil diameter copper with 20-mil diameter solder masks (non-solder mask defined pads). For escape and general DDR2 routing vias, 8-mil holes with 18-mil pads are recommended. BGA escape is accomplished by the typical dog-bone method.

It is also a good idea to maximize the size of the vias used for decoupling capacitors and power pins. This is done to minimize via inductance. It is the via and decoupling capacitor stray inductance that limits the performance of the decoupling capacitors. Use care to ensure that vias are not sized so large as to cut off a portion of a plane.

6.2 V_{REF}

V_{REF} is used by the input buffers of the DDR2 memories as well as the C6474 device's DDR2 interface to determine logic levels. V_{REF} is specified to be ½ the power supply voltage and is created using a voltage divider constructed from two 1-K Ω, 1% tolerance resistors (see Figure 1). V_{REF} is not a high current supply, but it is important to keep it as quiet as possible with minimal inductance. The minimum nominal trace width for V_{REF} is 20 mils. Necking down V_{REF} to accommodate BGA escape and localized via congestion is acceptable, but care should be taken to keep V_{REF} 20 mils wide as much as possible. V_{REF} is a DC net and, as such, trace delay is not critical; however, overall trace length should be kept to a minimum. The four or five decoupling capacitors on the V_{REF} net are intended to reduce AC noise. Two are used at the divider and one each is used near the V_{REF} input of the three loads (two DDR2s and the C6474 device) (see Figure 3).

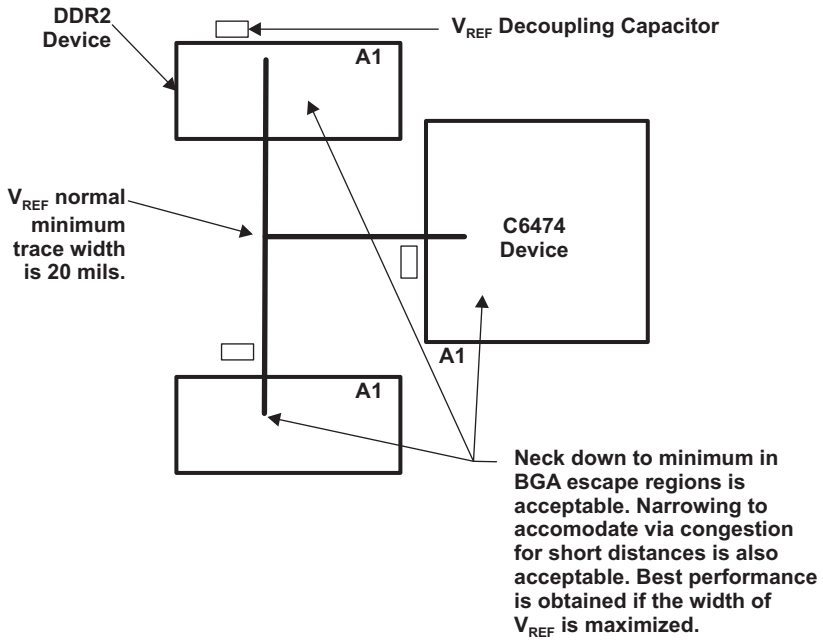


Figure 3. V_{REF} Routing

6.3 DDR2 Routing

This section describes the specific guidelines for placement used to drive the trace routes used in DDR2 simulations. This placement assumes logic analyzer connectors in order to analyze what is considered a worst-case implementation. The customer's DDR2 topology should be the same or better (shorter, fewer vias) than this topology.

The trace lengths and number of vias used in simulations are given in Table 3. RCVOUT to RCVIN should match the delay of DQS plus the delay of CLOCK. The last column gives the range of length matching. The AC timing analysis assumed the worst-case matching. Not included in this table is a 0.2-in. stub on each trace to account for the connection to a logic analyzer pad.

6.3.1 Net Classes

6.3.1.1 Clock Domain Net Classes

Net classes are used to associate the assorted groups of nets in the DDR2 interface with their clock domain. These net classes are used in the DDR2 routing rules. The DDR2 interface has five clock domains, four of which are bi-directional. The clock domain net classes are shown in Table 1.

All of the clock signals in the C6474 DDR2 interface are differential signals. Each clock domain net class needs to be routed as a differential signal with matched lengths for the non-inverting and inverting signals. Differential impedance should also be controlled.

Table 1. Clock Domain Net Classes

Clock Net Class	Description	DSP Pin Names
CK	DDR2 Interface Clock	DDRCLKP[1:0], DDRCLKN[1:0]
DQSB0	DQS for byte 0	DDRDQS0P, DDRDQS0N
DQSB1	DQS for byte 1	DDRDQS1P, DDRDQS1N
DQSB2	DQS for byte 2	DDRDQS2P, DDRDQS2N
DQSB3	DQS for byte 3	DDRDQS3P, DDRDQS3N

6.3.1.2 Signal Net Classes

Table 2 shows the seven additional net classes that use the clock net classes as their reference. Generally speaking, the nets within a net class and their associated clock domain should be skew matched to each other. The goal is to minimize the skew within each clock domain and crosstalk between signals — especially between signals of differing clock domains.

Table 2. Signal Net Classes

Net Class	Clock Domain	Description	DSP Pin Names
ADDR_CTRL	CK	Bank Address, Address, Control	DDRBA0-A2, DDRA00-DDRA13, $\overline{\text{DDRCE}}$, $\overline{\text{DDRCAS}}$, $\overline{\text{DDRRAS}}$, $\overline{\text{DDRWE}}$, DDRCKE
DQB0	DQSB0	DQs for byte 0	DDRD00-DDRD07, DDRDQM0
DQB1	DQSB1	DQs for byte 1	DDRD08-DDRD15, DDRDQM1
DQB2	DQSB2	DQs for byte 2	DDRD16-DDRD23, DDRDQM2
DQB3	DQSB3	DQs for byte 3	DDRD24-DDRD31, DDRDQM3
RCV0	CK, DQSB0-1	DQ gate timing loop for lower word	DDRRCVIN0, DDRRCVOUT0
RCV1	CK, DQSB2-3	DQ gate timing loop for upper word	DDRRCVIN1, DDRRCVOUT1

6.3.1.3 A Word About Trace Separation and BGA Escapes

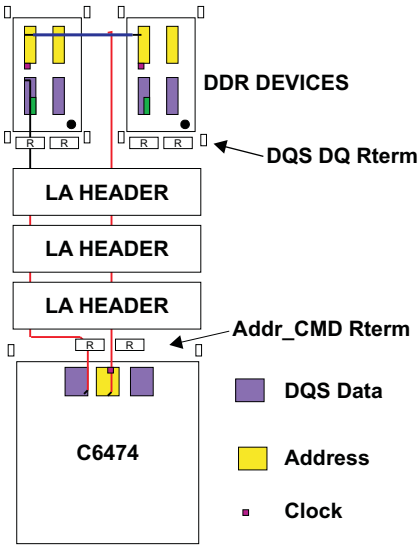
The net class routing rules in the next section give minimum trace separation requirements for the respective net class. It is understood that in the region near the BGA devices the traces have to be routed very close together, often at minimum trace separation. Minimum separation routing should be kept to a minimum and the total minimum separation routed length should not exceed 500 mils for each net.

6.4 Net Class Routing Rules

6.4.1 Routing Rules Overview

In order to define the routing rules, a worst-case placement is used. Trace routes are created based on this and comprehensive simulations and timing analysis are done to guarantee timing is met for these conditions. As long as the actual placement and routing are the same or better than these rules, the signal integrity and timings requirements are met.

The assumed placement is shown in Figure 4 and includes connections for logic analyzer headers. The stubs for the logic analyzer pads can be no more than 0.2 inches. The rest of the maximum routing rules derived from this placement and included in the analysis are described in Table 3 and in the following sections.



LA Header refers to the logic analyzer header. This is typically not present, nor recommended, in production applications as it may impact memory performance.

Figure 4. Worst-Case Placement Reference

Table 3. Summary of Routing Guidelines

Net Class	Series Resistor Location (near)	Maximum # of Vias	Maximum Length	Maximum Allowable Length Mismatch
CK	DSP	5	3.1 inches	Each pair matched within 10 mils
ADDR_CTRL	DSP	5	3.1 inches	±100 mils relative to CK
DQSBn	Memory Device	5	2.5 inches	±10 mils within a pair
DQBn (DDRDn)	Memory Device	5	2.5 inches	±50 mils relative to DQSBn
DQBn (DDRDQMn)	DSP	5	2.5 inches	±50 mils relative to DQSBn
RCVn	DSP	7	5.6 inches	±100 mils relative to CK + DQSBn(1)

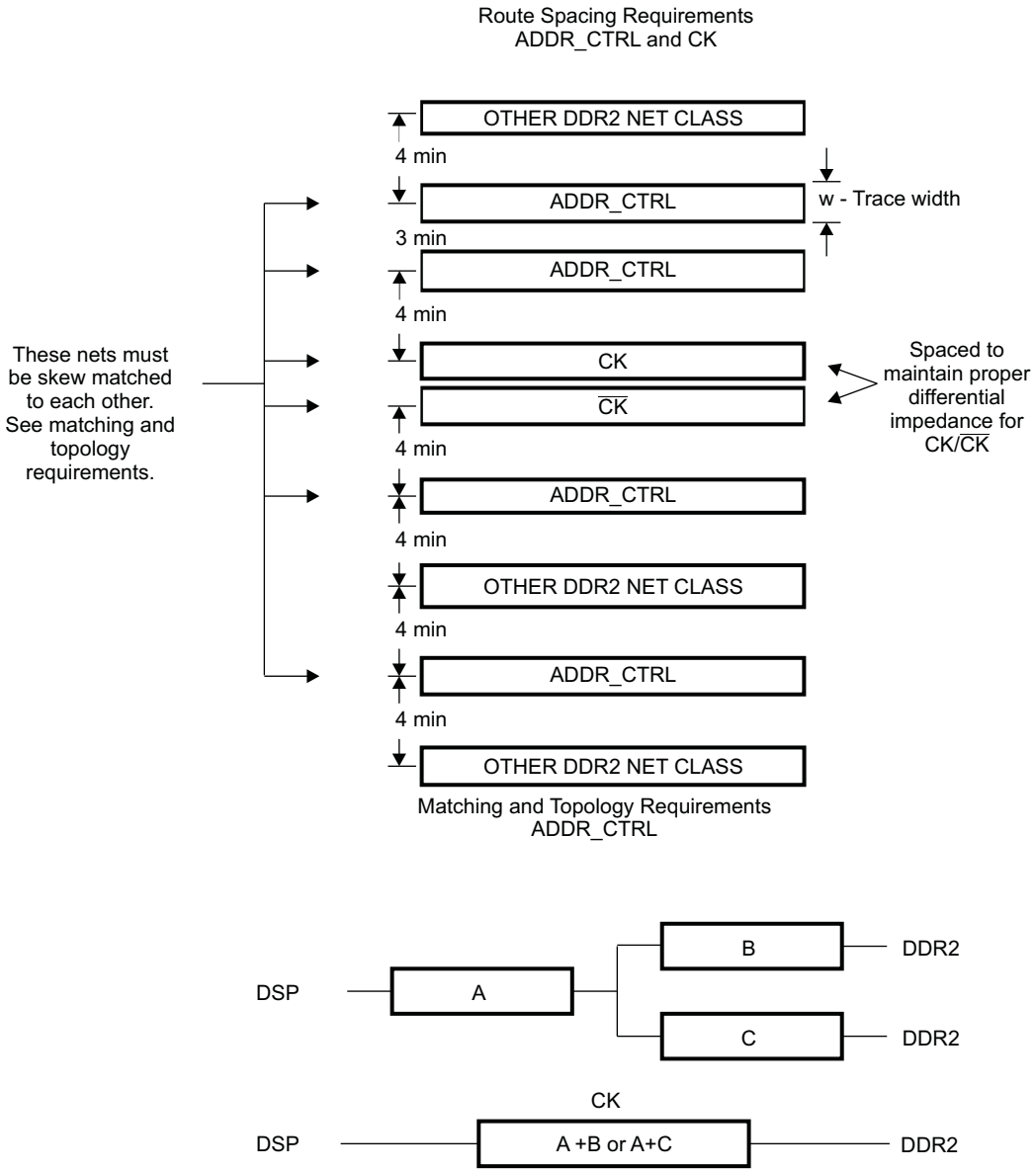
(1) For additional details, see Section 6.4.4.

The number of vias defined in the table are maximums, but fewer vias means more margin. The number of vias within a net class should be matched within 1 via.

The remaining sections provide more details on these requirements as well as spacing requirements.

6.4.2 CK and ADDR_CTRL

For this section, refer to Figure 5. This net class is completely sourced by the C6474 DSP to the DDR2 devices. The ADDR_CTRL nets are balanced "T" routes. Ideally, the PCB delay of the CK net class is identical to the delay for the ADDR_CTRL net class. All nets in the CK and ADDR_CTRL net class should be matched in length to each other within 100 mils. The nets in the CK net class must be laid out as a differential pair. The trace separation between the differential pair of net class CK should be such as to maintain the desired differential impedance. Other traces should be kept away from the CK net class traces by at least 4w center to spacing (recall that w = minimum trace width/space). Traces within the ADDR_CTRL net classes should be spaced at least 3w center-to-center from each other. Traces of other net classes should be kept 4w away from the ADDR_CTRL net class. The length of segment A should be maximized and the overall length from A to B or A to C should be minimized.



A Length B should match length C within 100 mils.

B Length A should be maximized while meeting the above specifications.

C For CK: The length of CK should match the length of net $\overline{CK}$ within 10 mils.

D For ADDR_CTRL and CK: Total lengths of A + B and A + C should be no more than 3.1 inches and use no more than 5 vias.

E For ADDR_CTRL and CK: Length A + B and A + C should match within 100 mils for ADDR_CTRL net class and CK net class.

F For ADDR_CTRL and CK: If desired, series terminating resistor should be located as close to the DSP as possible.

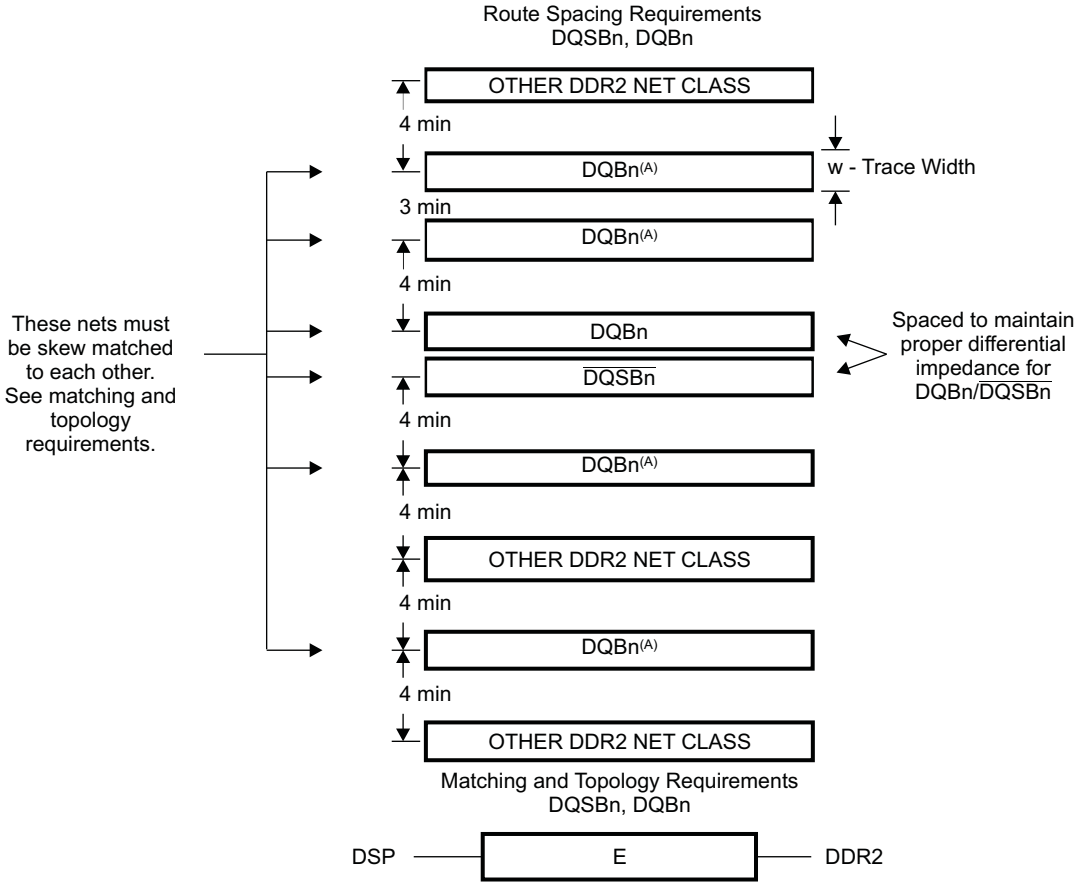
Figure 5. CK and ADDR_CTRL Routing Requirements

6.4.3 DQSBn and DQBn

For this section, refer to Figure 6. The 8-net classes that make up the 4 DQSs and 4 DQ bytes have the same routing rules. Note that the individual byte net classes do not have to be matched to each other. Skew matching is only required between the DQBn net class and its associated DQSBn net class. The length of the DQSBn classes need to be within 750 mils of the CK class nets. Figure 6 shows the topologies for the DQSBn and DQB nets.

These net classes are sourced by the C6474 device during writes and are sourced by the DDR2 devices during reads. The DQS acts as the data strobe as it is always sourced with the DQs. For write cycles, the DQS transitions in the middle of the bits cells on DQ. For read cycles, the DQS transitions at the same time as the DQS. The interface is more sensitive to DQS ↔ DQ crosstalk during reads. The data mask bits (DDRDQMn) are static during reads; therefore, they can be used as shields between the DQ and DQS to improve read crosstalk performance.

Ideally, the PCB delay of the DQSBn net class is identical to the delay for the DQBn net class. All nets in the DQSBn and DQBn net class should be matched in length to each other within 100 mils, centered about the length of DQSBn signals. The nets in the DQSBn net class must be laid out as a differential pair. The trace separation between the differential pair of net class DQSBn should be such as to maintain the desired differential impedance. Other traces should be kept away from the DQSBn net class traces by at least 4w center to spacing (recall that w = minimum trace width/space). Traces within the DQBn net classes should be spaced at least 3w center-to-center from each other. Traces of other net classes should be kept 4w away from the DQBn net class.



A For DQBn and DQSBn: Length E for DQB0 should match within ± 50 mils of DQSB0.

B Length E for DQB1 should match within ±50 mils of DQSB1.

C Length E for DQB2 should match within ±50 mils of DQSB2.

D Length E for DQB3 should match within ±50 mils of DQSB3.

E Total length of E should be no more than 2.5 inches and use no more than 5 vias.

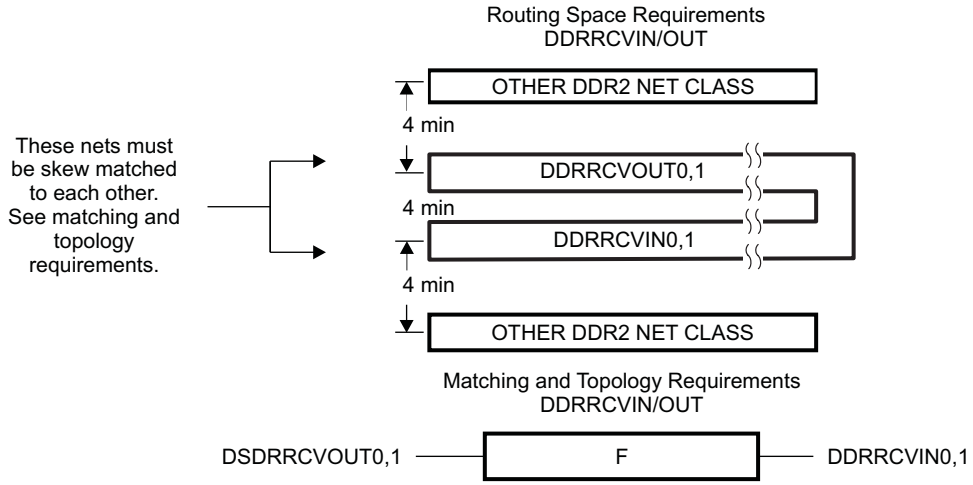
F If desired, series terminating resistor should be located as close to the DDR2 as possible except for DDRDQMn that should be located close to the DSP.

G In addition, for DQSBn: The length of DQSBn should match the length of net $\overline{\text{DQSBn}}$ within 10 mils.

Figure 6. DQSBn and DQBn Routing Requirements

6.4.4 RCV0 and RCV1

For this section, refer to Figure 7. These two net classes are used by the C6474 device to predict the round trip delay of the PCB layout. The result is two out and back PCB traces that match the delay of the clock net plus the DQS.



A Length F (combined DDRRCVIN/DDRRCVOUT) should be within ±100 mils to the total combined length for CLK0 plus the average of DQSB0 and DQSB1.

B Length F (combined DDRRCVIN/DDRRCVOUT) should be within ±100 mils to the total combined length for CLK1 plus the average of DQSB2 and DQSB3.

C The total number of vias used for the combined RCVIN/OUT net shall not exceed 7 and shall match the total number of vias used for the CLK + DQSBn nets combined (e.g., if RCVIN + RCVOUT = total 5 vias, then the total vias for CLK + DQSBn must = 5 vias). At no time shall the total number of vias exceed 7.

D If desired, series terminating resistor should be located as close to DSP DDRRCVOUT0, 1 as possible.

Figure 7. RCV0 and RCV1 Routing Requirements

7 References

TMS320C6474 DSP DDR2 Memory Controller User's Guide (SPRUG19)