PRU Read Latencies

ABSTRACT

This application report discusses the hardware latencies associated with PRU-initiated memory reads.

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1 Introduction

The PRU is a scalar processor, processing each instruction sequentially. With the exception of memory read instructions, all PRU instructions execute in a single cycle. However, the execution time of PRU read instructions varies based on memory access latencies. Subsequent instructions will not execute until the completion of the read instruction and may impact time-sensitive operations and applications.

2 PRU Instruction Execution Time Comparison

2.1 PRU Write Instruction

The PRU write instruction is a fire-and-forget command that executes in approximately 1 cycle.

2.2 PRU Read Instruction

The PRU read instruction executes in ~2 cycles, plus additional latencies due to traversing through interconnect layers and variable processing loads.

For "best case" read latency values on each device, see Appendix A. These read latencies account for the 2 cycle read instruction and interconnect introduced latency. As discussed in Section 3, MMRs that are "closer" to the PRU (within the PRU Subsystem) will have lower access latencies. Also, memory accesses outside of the PRU Subsystem are not deterministic.

2.3 Other PRU Instructions

All other PRU instructions execute in a single cycle.

3 ARM + PRU SoC Architecture

The PRU Subsystem is a master initiator with access to local subsystem resources, in addition to all SoC resources. Figure 1 shows a generic view of the SoC architecture, highlighting how the PRU subsystem fits into the overall SoC.

3.1 Local PRU Subsystem Resources

The PRU accesses local subsystem resources using a Local Memory Map. This Local Memory Map only uses the local 32-bit Interconnect Bus located inside the subsystem to access local resources. Therefore, the close proximity of these resources to the PRU core, coupled with the PRU Local Memory map that ensures the access path is confined to the PRU Subsystem, minimizes access latencies.

3.2 SoC Resources

To access SoC resources outside of the PRU Subsystem, the PRU accesses must go through external layer(s) of interconnects. In other words, the PRU must go through the local 32-bit Interconnect Bus and varying levels of L3/L4 interconnects external to the subsystem before reaching the resource. This access path is much longer than the PRU's access path to local subsystem resources, causing longer access latencies. Additionally, the access latency for external resources will be indeterministic, as they varies based on system processing loads.

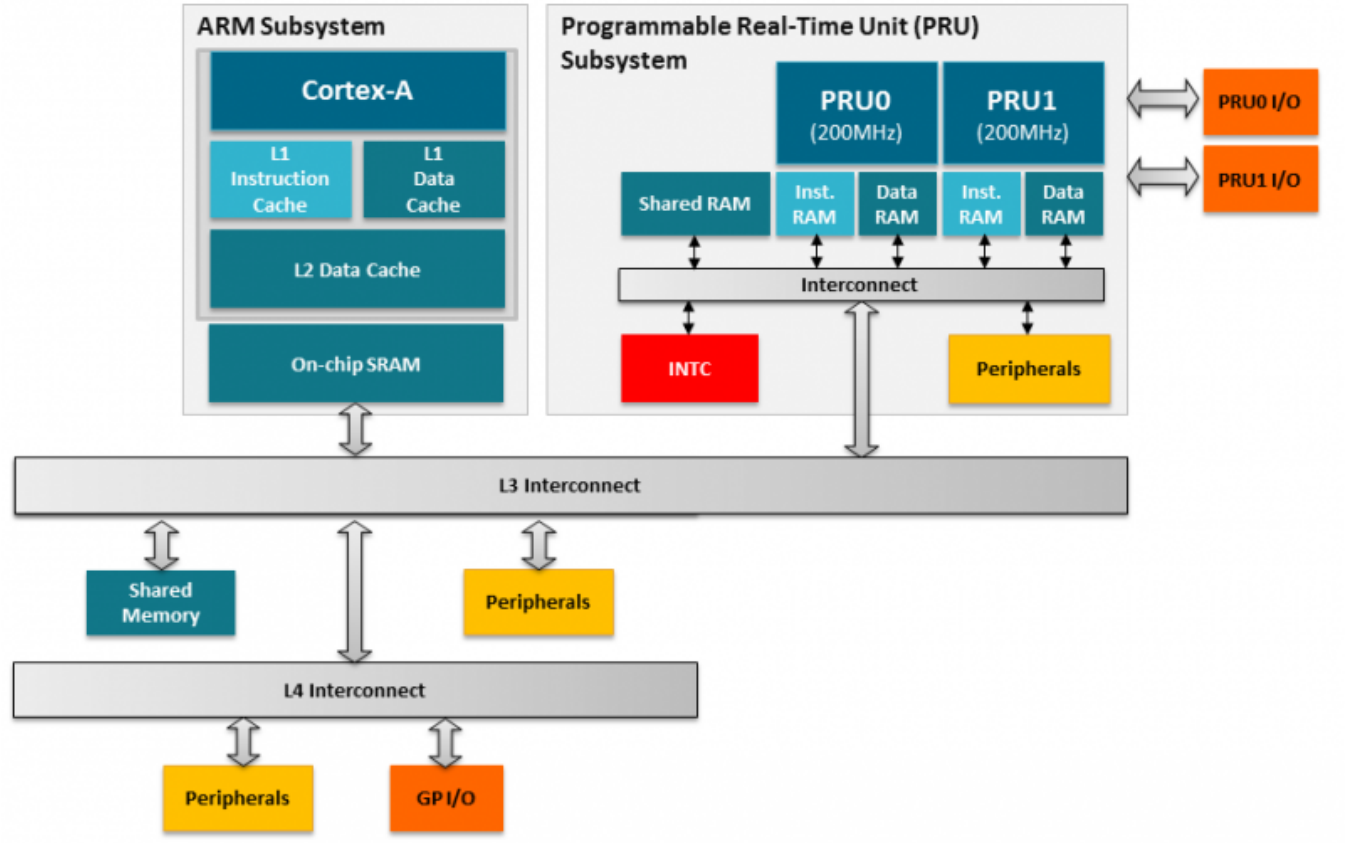

Figure 1. Programmable Real-Time Unit (PRU) Subsystem

Device-Specific PRU Read Latency Values

The read latency values provided in this appendix are considered "best-case," accounting for the 2 cycle instruction and interconnect introduced latency. Note, memory accesses outside of the PRU Subsystem are not deterministic.

A.1 AM335x

Table 1 through Table 3 are considered "best-case" read latency values for the PRU on AM335x.

Table 1. AM335x PRU Read Latencies - Local PRU Subsystem Resources

MMRs	Read Latency (PRU cycles @ 200 MHz)
PRU CTRL	4
PRU CFG	3
PRU INTC	3
PRU DRAM	3
PRU Shared DRAM	3
PRU ECAP	4
PRU UART	14
PRU IEP	12
PRU R31 (GPI)	1

Table 2. AM335x PRU Read Latencies - Global SoC Resources

MMRs	Read Latency (PRU cycles @ 200 MHz)
L3F Interconnect	
EMIF	36
TPTC0-2 (EDMA3TC0-2)	34
TPCC (EDMA3CC)	41
OCMC RAM	27
L3S Interconnect	
GPMC	38
McASP0-1	38
ADC/TSC	42
L4_PER Interconnect	
DCAN0-1	40
DMTIMER2-7	38
PWMSS	38
ELM	34
GPIO1-3	34
I2C1-2	34
LCDC	38
Mailbox	38
MMCSD0-1	34

Table 2. AM335x PRU Read Latencies - Global SoC Resources (continued)

MMRs	Read Latency (PRU cycles @ 200 MHz)
McSPI0-1	34
Spinlock	38
UART1-5	34
L4_FAST Interconnect	
CPSW/GEMAC	41
L4_WKUP Interconnect	
ADC/TSC	41
Control Module	41
DMTIMER0	38
DMTIMER1_1MS	38
GPIO0	38
I2C0	38
UART0	38
WDT1	38
PRCM	88
RTC	62

Table 3. PRU Data Transfer Latencies

Source	Destination	Size (bytes)	Latency (PRU cycles @ 200 MHz)
PRU Shared RAM	DDR	4	5
		32	19
		128	65
DDR	PRU Shared RAM	4	47
		32	62
		128	107

A.2 AM437x

Table 4 through Table 7 are considered "best-case" read latency values for the PRU on AM437x.

Table 4. AM437x PRU Read Latencies - Local PRU-ICSS Resources

MMRs	Read Latency (PRU cycles @ 200 MHz)
PRU CTRL	4
PRU CFG	3
PRU INTC	3
PRU DRAM	3
PRU Shared DRAM	3
PRU ECAP	4
PRU UART	10
PRU R31 (GPI)	1

Table 5. AM437x PRU Read Latencies - Other PRU-ICSS Resources

MMRs	Read Latency (PRU cycles @ 200 MHz)
PRU CTRL	8
PRU CFG	7
PRU INTC	7
PRU DRAM	7
PRU Shared DRAM	7
PRU ECAP	8
PRU UART	14

Table 6. AM437x PRU Read Latencies - Global SoC Resources

MMRs	Read Latency (PRU cycles @ 200 MHz)
L3F Interconnect	
EMIF	28
EDMA3TC (TPTC) CFG	34
EDMA3CC (TPCC) CFG	34
OCMC RAM	27
SRAM_INT (MPUSS L2 RAM)	38
L3S Interconnect	
GPMC	40
McASP	43
QSPI	39
ADC0	78
MMCSD	36
L4_PER Interconnect	
DCAN	39
DMTIMER(2-11)	39
PWMSS	39
ELM	39
GPIO(1-5)	39
I2C(1-2)	39
DSS	39
HDQ1W	37
USB	35

Table 6. AM437x PRU Read Latencies - Global SoC Resources (continued)

MMRs	Read Latency (PRU cycles @ 200 MHz)
Mailbox	39
McASP CFG	39
MMCSD	36
McSPI	39
Spinlock	39
UART(1-5)	39
VPFE	41
ADC1	37
L4_FAST Interconnect	
CPSW/GEMAC	27
L4_WKUP Interconnect	
Control Module	78
DMTIMER0	72
DMTIMER1_1MS	72
GPIO0	72
I2C0	72
UART0	80
WDT1	72
PRCM	110
SYNCTIMER32K	72
RTC	122
ADC0	80

Table 7. PRU Data Transfer Latencies

Source	Destination	Size (bytes)	Latency (PRU cycles @ 200 MHz)
PRU Shared RAM	DDR	4	5
		32	19
		124	65
DDR	PRU Shared RAM	4	30
		32	44
		124	90

A.3 AM57x

Table 8 through Table 11 are considered "best-case" read latency values for the PRU on AM57x.

Table 8. AM57x PRU Read Latencies - Local PRU-ICSS Resources

MMRs	Read Latency (PRU cycles @ 200 MHz)
PRU CTRL	4
PRU CFG	3
PRU INTC	3
PRU DRAM	3
PRU Shared DRAM	3
PRU IEP	11
PRU UART	13
PRU ECAP	4
PRU R31 (GPI)	1

Table 9. AM57x PRU Read Latencies - Other PRU-ICSS Resources

MMRs	Read Latency (PRU cycles @ 200 MHz)
PRU CTRL	30
PRU CFG	30
PRU INTC	30
PRU DRAM	30
PRU Shared DRAM	30
PRU IEP	38
PRU UART	40
PRU ECAP	30

Table 10. AM57x PRU Read Latencies - Global SoC Resources

MMRs	Read Latency (PRU cycles @ 200 MHz)
L3 Interconnect	
OCMC_RAM1	33
OCMC_RAM(2-3)	38
EDMA_TPCC	34
EDMA_TC0	35
MCASP(1-3)_DATA	28
EMIF1	49
DMM	37
GPMC	33
PCIE_SS1	31
DSS	36
EMIF1_SDRAM_CS0	60
L4_CFG Interconnect	
DMA_SYSTEM	39
MAILBOX1	37
SPINLOCK	35
SATA	39
L4_WKUP Interconnect	
COUNTER_32K	122
GPIO1	112

Table 10. AM57x PRU Read Latencies - Global SoC Resources (continued)

MMRs	Read Latency (PRU cycles @ 200 MHz)
WD_TIMER2	112
TIMER(1, 12)	112
KBD	122
UART10	112
DCAN1	112
L4_PER1 Interconnect	
UART(1-3)	60
UART(4-6)	40
TIMER(2-4, 9-11)	37
GPIO(2-8)	37
I2C(1-5)	37
ELM	37
MCSPI(1-4)	37
MMC(1-4)	37
HDQ1W	40
L4_PER2 Interconnect	
UART(7-9)	38
MCASP(4-5)	38
PWMSS(1-3)	38
MCASP_DAT(6-8)	38
MCASP_CFG(1-8)	38
DCAN2	38
GMAC_SW	55
L4_PER3 Interconnect	
TIMER(5-8, 13-16)	37
RTC_SS	37
MAILBOX(2-13)	35
VIP(1-3)	50
VPE	52
CAL (AM571x only)	48

Table 11. PRU Data Transfer Latencies

Source	Destination	Size (bytes)	Latency (PRU cycles @ 200 MHz)
PRU Shared RAM	DDR	4	5
		32	19
		124	65
DDR	PRU Shared RAM	4	62
		32	79
		124	134

A.4 K2G

Table 12 through Table 15 are considered "best-case" read latency values for the PRU on 66AK2G02.

Table 12. 66AK2G02 PRU Read Latencies - Local PRU-ICSS Resources

MMRs	Read Latency (PRU cycles @ 200 MHz)
PRU CTRL	4
PRU CFG	3
PRU INTC	3
PRU DRAM	3
PRU Shared DRAM	3
PRU ECAP	4
PRU UART	13
PRU IEP	11
PRU MII_RT	3
PRU MDIO	3

Table 13. 66AK2G02 PRU Read Latencies - Other PRU-ICSS Resources

MMRs	Read Latency (PRU cycles @ 200 MHz)
PRU CTRL	13
PRU CFG	12
PRU INTC	12
PRU DRAM	12
PRU Shared DRAM	12
PRU ECAP	13
PRU UART	23
PRU IEP	20
PRU MII_RT	12
PRU MDIO	12

Table 14. 66AK2G02 PRU Read Latencies - Global SoC Resources

MMRs	Read Latency (PRU cycles @ 200 MHz)
TeraNet_DMA	
GPMC_0_SLV	39
MSMC_SRAM	30
SPI_(0-3)_SLV	48
MCASP_(0-2)_SLV	39
MCBSP_0_SLV	34
MMCSD_(0-1)_S	36
TeraNet_CFG	
UART_(0-3)_CFG	65
ELM_0_CFG	35
ASRC_0_CFG	30
QSPI_0_CFG	73
CIC_0_CFG	39
PCIE_0_PHY_CFG	55
PCIE_0_ECC_CFG	33
SEMAPHORE_0_CFG	34
TIMER_(0-5)_CFG	55

Table 14. 66AK2G02 PRU Read Latencies - Global SoC Resources (continued)

MMRs	Read Latency (PRU cycles @ 200 MHz)
I2C_(1-2)_CFG	55
MPU_(3-13,15-16)	28
MPU_14	39
USB_(0-1)_CFG	57
EPWM_(0-5)_CFG	53
EQEP_(0-2)_CFG	53
ECAP_(0-1)_CFG	53
MCASP_(0-2)_CFG	43
MCBSP_0_CFG	38
MCBSP_0_FIFO_CFG	38
MLB_0_CFG	35
EDMA_(0-1)_CC_CFG	34
EDMA_0_TC(0-1)_CFG	34
EDMA_1_TC(0-1)_CFG	34
DSSUL_0_CFG	48
TeraNet_AON	
PSC_0_CFG	38
BOOTCONFIG_0_CFG	46
DCAN_(0-1)_S	48
GPIO_(0-1)_CFG	50
PMMC_0_SLV	38
PBIST_COM_0_CFG	38
PBIST_CTL_0_CFG	38
TIMER_6_CFG	50
I2C_0_CFG	50
MPU_(1-2)_CFG	38
OTP_0_CFG	38
MESSAGE_MANAGER_0_CFG	38

Table 15. PRU Data Transfer Latencies

Source	Destination	Size (bytes)	Latency (PRU cycles @ 200 MHz)
PRU Shared RAM	DDR	4	5
		32	19
		124	68
DDR	PRU Shared RAM	4	57
		32	108
		124	380

A.5 AM65x

Table 16 and Table 17 are considered "best-case" read latency values for the PRU and RTU_PRU on AM65x.

Table 16. AM65x PRU/RTU_PRU Read Latencies - Local PRU_ICSSG Resources

MMRs	Read Latency (PRU cycles)	
	IEP CLK Async Mode	IEP CLK Sync Mode
PRU_ICSSG PRUn_CTRL (1)	6	
PRU_ICSSG RTU_PRUn_CTRL (1)	6	
PRU_ICSSG CFG	3	
PRU_ICSSG ICSSG_CFG	3	
PRU_ICSSG INTC	3	
PRU_ICSSG DRAMn (1)	3	
PRU_ICSSG Shared DRAM	3	
PRU_ICSSG IEPn (1)	13	3
PRU_ICSSG ECAP0	4	
PRU_ICSSG UART0	16	
PRU_ICSSG MII_RT_CFG	3	
PRU_ICSSG MDIO	3	
PRU_ICSSG TM_CFG_PRUn (1)	3	
PRU_ICSSG TM_CFG_RTUn (1)	3	
PRU_ICSSG RAT_SLICEn (1)	3	
PRU_ICSSG PROTECT	3	
PRU_ICSSG PA_STATS_QRAM	9	
PRU_ICSSG PA_STATS_CRAM	9	
PRU_ICSSG PA_STATS_CFG	4	

(1) n = 0 or 1

Table 17. AM65x PRU/RTU_PRU Read Latencies - Other PRU_ICSSG Resources

MMRs	Read Latency (PRU cycles)	
	CORE CLK Async Mode	CORE CLK Sync Mode
PRU_ICSSG PRUn_CTRL (1)	51	48
PRU_ICSSG RTU_PRUn_CTRL (1)	51	48
PRU_ICSSG CFG	51	48
PRU_ICSSG ICSSG_CFG	51	48
PRU_ICSSG INTC	48	
PRU_ICSSG DRAMn (1)	48	
PRU_ICSSG Shared DRAM	48	
PRU_ICSSG IEPn (1)	48	
PRU_ICSSG ECAP0	48	
PRU_ICSSG UART0	59	
PRU_ICSSG MII_RT_CFG	48	
PRU_ICSSG MDIO	48	
PRU_ICSSG TM_CFG_PRUn (1)	48	
PRU_ICSSG TM_CFG_RTUn (1)	48	
PRU_ICSSG RAT_SLICEn (1)	48	
PRU_ICSSG PROTECT	48	
PRU_ICSSG PA_STATS_QRAM	48	
PRU_ICSSG PA_STATS_CRAM	48	

Table 17. AM65x PRU/RTU_PRU Read Latencies - Other PRU_ICSSG Resources (continued)

MMRs	Read Latency (PRU cycles)	
	CORE CLK Async Mode	CORE CLK Sync Mode
PRU_ICSSG PA_STATS_CFG	53	51
PRU_ICSSG PA_STATS_CRAM	53	51
PRU_ICSSG PA_STATS_CFG	48	
PRU_ICSSG PRUn_DBG (1)	51	48
PRU_ICSSG RTU_PRUn_DBG (1)	51	48

(1) n = 0 or 1

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2018) to A Revision	Page
• Added new Section A.5	12

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