Application Note

AM62Ax/AM62Px LPDDR4 Board Design and Layout Guidelines

ABSTRACT

This application report contains material applicable to the LPDDR4 interface of AM62Ax/AM62Px processor board designs.

Table of Contents

List of Figures

List of Tables

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1 Overview

The AM62Ax/AM62Px processors support LPDDR4 SDRAMs. This document contains material applicable to board designs containing LPDDR4 memories. For supported data rates/speed grades, see the device-specific data manual.

Note

To facilitate software configuration of the DDR subsystem, use the DDR Subsystem Register Configuration Tool in SysConfig (*https://dev.ti.com/sysconfig*)

1.1 Board Designs Supported

In order to achieve the high frequency targets of the LPDDR4 interfaces supported by the AM62Ax/AM62Px family of devices, an optimal PCB implementation is required. TI highly recommends that customer designs copy the TI AM62A LP SK EVM or AM62P-LP SK EVM PCB layout exactly, and in every detail (PCB material, routing, spacing, vias, and so forth) in order to achieve the full specified interface frequency/data rate. If the design does not or cannot copy the TI solution, TI's EVM should still be used as a starting point, and simulations must be performed. The customer design may need to constrain the interface frequency/data rate based on the PCB implementation.

The goal of this document is to define a set of layout and routing and simulation rules that allow designers to successfully implement a robust design for the topologies that TI supports. It is also required that the PCB design be simulated to ensure the design targets are achieved. TI will limit debug/support for boards that have not been designed and simulated according to the steps defined in this document. Systems that do not follow the TI EVM implementation and/or do not have valid simulation results will likely need to run at a reduced DDR frequency.

This document provides reference eye masks as guidance for validation of the simulations results. It is still expected that the PCB design work (design, layout, and fabrication) is performed and reviewed by a highly knowledgeable high-speed PCB designer. Problems such as impedance discontinuities when signals cross a split in a reference plane can be detected visually by those with the proper experience.

TI only supports board designs that follow the guidelines in this document. These guidelines are based on well-known transmission line properties for copper traces routed over a solid reference plane. Declaring insufficient PCB space does not allow routing guidelines to be discounted. TI will limit debug/support for designs that have not been simulated according to the steps defined in this document.

1.2 General Board Layout Guidelines

To ensure good signaling performance, the following general board design guidelines must be followed:

- All signals need ground reference (strongly suggest on both sides).
- Avoid crossing plane splits in the signal reference planes.
- Use the widest trace that is practical between decoupling capacitors and memory modules.
- Minimize inter-symbol interference (ISI) by keeping impedances matched.
- Minimize crosstalk by isolating sensitive signals, such as strobes and clocks, and by using a proper PCB stack-up.
- Avoid return path discontinuities by adding vias or capacitors whenever signals change layers and reference planes.
- Minimize reference voltage noise through proper isolation and proper use of decoupling capacitors on the reference input pins on the SDRAMs.
- Keep the signal routing stub lengths as short as possible.
- Add additional spacing for clock and strobe nets to minimize crosstalk.
- Maintain a common ground (also called VSS) reference for all bypass and decoupling capacitors.
- Consider the differences in propagation delays between microstrip and stripline nets when evaluating timing constraints.
- Via-to-via coupling can be significant part of PCB-level crosstalk. Dimension and pitch of vias is important. For high speed interfaces, consider GND shielding vias.
- Via stubs affect signal integrity. Via back-drilling can improve signal integrity, and may be required in some instances.

For more information, see the *High-Speed Interface Layout Guidelines*. It provides additional general guidance for successful routing of high-speed signals.

1.3 PCB Stack-Up

The recommended stack-up for routing the DDR interface is a ten or twelve layer stack up. However, this can only be accomplished on a board with routing room with large keep-out areas. Additional layers are required if:

- The PCB layout area for the DDR Interface is restricted, which limits the area available to spread out the signals to minimize crosstalk.
- Other circuitry must exist in the same area, but on layers isolated from the DDR routing.
- Additional planes layers are needed to enhance the power supply routing or to improve EMI shielding.

Board designs that are relatively dense may require more layers to properly allow the DDR routing to be implemented such that all rules are met.

All DDR signals must be routed adjacent to a solid VSS reference plane. When multiple VSS reference planes exist in the DDR routing area, stitching vias must be implemented nearby wherever vias transfer signals to a different VSS reference plane. This is required to maintain a low-inductance return current path.

It is strongly recommended all DDR signals be routed as strip-line. Some PCB stack-ups implement signal routing on two adjacent layers. This is not recommended as crosstalk occurs on any trace routed parallel to another trace on an adjacent layer, even for a very short distance. It is recommended to route LPDDR4 signals on PCB layers closer to the SoC within the stackup, giving the signal a shorter travel time through the via. The PCB layers farther from the SoC will have longer travel times through the via, which can increase coupling between vias. Both signal and via coupling can lead to smaller timing margins.

Note a shorter via travel could mean a longer via stub (if using standard drill vias), so that is to be considered as well. Simulation can be used to determine if via stub length is an issue.

PCB material is another important factor. Depending on the design specifics, it may be required to use a higher frequency material such as ISOLA I-Speed or equivalent/better to achieve highest data rates. For supported data rates/speed grades, see the device-specific data manual. Standard FR4 products like 370HR can be used for lower data rates. In specific cases, it is sufficient for higher data rates as well.

Table 1-1. PCB Stack-up Specifications

Number	Parameter[6]	MIN	TYP	MAX	UNIT
PS1	PCB routing plus plane layers		10 or 12		
PS2	Signal routing layers		6		
PS3	Full VSS reference layers under DDR routing region [1]	1			
PS4	Full VDDS_DDR power reference layers under the DDR routing region [1]	1			
PS5	Number of reference plane cuts allowed within DDR routing region [2]			0	
PS6	Number of layers between DDR routing layer and reference plane [3]			0	
PS7	PCB routing feature size		4		Mils
PS8	PCB trace width, w	3			Mils
PS9	Point-to-Point, single-ended impedance		40		Ω
PS10	Point-to-Point, differential impedance		80		Ω
PS11	T-Branch, single-ended impedance [5]		35/70		Ω
PS12	T-branch, differential impedance [5]		70/140 [7]		Ω
PS13	Impedance control [4]	Z-10%	Z	Z+10%	Ω

(1) Ground reference layers are preferred over power reference layers. Return signal vias need to be near layer transitions.
(2) No traces should cross reference plane cuts within the DDR routing region. High-speed signal traces crossing reference plane cuts create large return current paths, which can lead to excessive crosstalk and EMI radiation. Beware of reference plane voids caused by via antipads, as these also cause discontinuities in the return current path.
(3) Reference planes are to be directly adjacent to the signal layer, to minimize the size of the return current loop.
(4) Z is the nominal singled-ended or differential impedance selected for the PCB specified by PS9-PS12.
(5) Balanced T traces (also referred to as T-branch traces) are split traces from source to multiple end points. The target impedance of the split trace should be twice that of the non-branched impedance. See routing topologies. The maximum trace impedance is typically

limited by the minimum trace width achievable. Reduction of the non-branched impedance may be necessary to maintain the 2:1 trace impedance ratio.

(6) These specifications are to be used as a starting point for designs. It is recommended each design be extracted and simulated to ensure all requirements are met.

(7) These values can be relaxed to 60/120 to facilitate fabrication, but it is recommended to prove eye margins are still adequate with simulations.

1.4 Bypass Capacitors

1.4.1 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR SDRAMs and other circuitry. Table 1-2 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Table 1-2 only covers the bypass needs of the SoC's DDR PHY. Additional bulk bypass capacitance may be needed for other circuitry. For any additional decoupling requirements for the SDRAM devices, see the manufacturer's data sheet

Table 1-2. Bulk Bypass Capacitors

Number	Parameter	MIN	MAX	UNIT
1	VDDS_DDR bulk bypass capacitor count(1)	1 (2)		Devices
2	VDDS_DDR bulk bypass total capacitance	10 (2)		µF

(1) These devices should be placed near the devices they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass capacitors and DDR signal routing.

(2) The capacitor recommendations in this guide reflect only the needs of this processor. For determining the appropriate decoupling capacitor arrangement for the memory device itself, see the memory vendor's guidelines.

1.4.2 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass capacitors to VDDS_DDR and the associated ground connections. Table 1-3 contains the specification for the HS bypass capacitors and for the power connections on the PCB. Generally speaking, TI recommends:

- Fitting as many HS bypass capacitors as possible.
- Minimizing the distance from the bypass capacitor to the pins and balls being bypassed.
- Using the smallest physical sized ceramic capacitors possible with the highest capacitance readily available.
- Connecting the bypass capacitor pads to their vias using the widest traces possible and using the largest via hole size possible.
- Minimizing via sharing. Note the limits on via sharing shown in Table 1-3.
- Using three-terminal capacitors instead of two-terminal capacitors. Three-terminal capacitors provide lower loop inductance , and one three-terminal capacitor could take the place of multiple two-terminal capacitors, further optimizing loop inductance. For examples, see the *AM62A Low-Power SK EVM User's Guide* (SPRUJ66) or the *AM62P SK EVM User's Guide* (SPRUJA2).

For any additional SDRAM requirements, see the manufacturer's data sheet.

Table 1-3. High-Speed Bypass Capacitors

Number	Parameter	MIN	TYP	MAX	UNIT
1	HS bypass capacitor package size (1)		0201	0402	10 Mils
2	Distance, HS bypass capacitor to processor being bypassed (2) (3) (4)			400	Mils
3	Processor HS bypass capacitor count per VDDS_DDR rail (5)	12			Devices
4	Processor HS bypass capacitor total capacitance per VDDS_DDR rail	3.7			µF
5	Number of connection vias for each device power/ground ball	1			Vias
6	Trace length from processor power/ground ball to connection via (2)		35	70	Mils
7	Distance, HS bypass capacitor to DDR device being bypassed (6)			150	Mils
8	DDR device HS bypass capacitor count (5) (7)	12			Devices
9	DDR device HS bypass capacitor total capacitance (7)	0.85			µF
10	Number of connection vias for each HS capacitor (8) (9)	2			Vias
11	Trace length from bypass capacitor to connection via (2) (9)		35	100	Mils
12	Number of connection vias for each DDR device power/ground ball	1			Vias
13	Trace length from DDR device power/ground ball to connection via (2)		35	60	Mils

(1) LxW, 10-mil units, that is, a 0402 is a 40 x 20-mil surface-mount capacitor.
(2) Closer/shorter is preferable.
(3) Measured from the nearest processor power or ground ball to the center of the capacitor package.
(4) Five of these capacitors should be located underneath the processor, among the cluster of VDDS_DDR balls.
(5) Low-ESL/multi-terminal capacitors may further reduce number of bypass capacitors required.
(6) Measured from the DDR device power or ground ball to the center of the capacitor package. For more information, see the guidance from the SDRAM manufacturer.
(7) Per DDR device. For more information, see the guidance from the SDRAM manufacturer.
(8) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board. No sharing of vias is permitted on the same side of the board.
(9) An HS bypass capacitor may share a via with a DDR device mounted on the same side of the PCB. A wide trace should be used for the connection, and the length from the capacitor pad to the DDR device pad should be less than 150 mils.

1.5 Velocity Compensation

For a PCB design, portions of the DDR signal traces are microstrip (BGA break-out segments), but majority of the trace segments are stripline (internal layers). Even though there is a wide variation in the proportion of track length routed as microstrip or stripline, the length/delay matching process should include a mechanism for compensating for the velocity delta between these two types of PCB interconnects. A compensation factor of 1.1 has been specified for this purpose by JEDEC. All microstrip segment lengths are to be divided by 1.1 before summation into the length matching equation. The resulting compensated length is termed the 'stripline equivalent length'. While some amount of residual velocity mismatch skew remains in the design, the process is a substantial improvement over simple length matching.

2 LPDDR4 Board Design and Layout Guidance

2.1 LPDDR4 Introduction

LPDDR4 is an SDRAM device specification governed by the JEDEC standard JESD209-4, Low Power Double Data Rate 4 (LPDDR4). This standard strives to reduce power and improve signal integrity by implementing a lower voltage I/O power rail, employing ODT on the Command/Address bus, and reducing the overall width of the Command/Address bus, among other features. Unlike other DDR types, LPDDR4 has been organized into 2 × 16-bit channels. ECC is supported inline, thus a dedicated SDRAM for ECC is not required.

LPDDR4X is a variant of LPDDR4, with the difference of additional power savings by reducing the I/O voltage from 1.1 V to 0.6 V. LPDDR4X is not supported with the AM62Ax/AM62Px device.

The maximum supported rows for LPDDR4 devices is 17. The JEDEC standard was ratified in 2020, and increased the max number of rows from 17 to 18. As a result, certain high density parts that use byte-mode die and require 18 row bits are not supported.

ECC is supported on the LPDDR4 interface. Unlike traditional ECC interfaces which require dedicated memory pins and devices, ECC is supported inline. The ECC system impact is in interface bandwidth and overall memory density, as ECC data is stored alongside non-ECC data.

The following sections detail the routing specification and layout guidelines for an LPDDR4 interface.

2.2 LPDDR4 Device Implementations Supported

There are different LPDDR4 SDRAM combinations supported by the DDR subsystem. Table 2-1 lists the supported device combinations.

Table 2-1. Supported LPDDR4 SDRAM Combinations

LPDDR4 SDRAM Count	Channels	Die	Ranks	LPDDR4 Channel Width	DDRSS Data Width
1 (1) (2)	1	1	1	16 bits	16 bits
1 (3)	2	1	1	16 bits	32 bits
1 (3)	2	2	1	16 bits	32 bits
1 (4)	2	2	2	16 bits	32 bits
1 (4)	2	4	2	16 bits	32 bits

(1) See 16-Bit, Single Rank LPDDR4 Implementation.
(2) 16 bit DDRSS data width implementations are non-standard, but supported on select devices. See device-specific data manual if supported for a particular processor.
(3) See 32-Bit, Single Rank LPDDR4 Implementation.
(4) See 32-Bit, Dual-Rank LPDDR4 Implementation.

2.3 LPDDR4 Interface Schematics

The LPDDR4 interface schematics vary, depending upon the number of ranks implemented. General connectivity is straightforward and consistent between the implementations. Figure 2-1 illustrates a 32-bit, single-rank LPDDR4 implementation. If dual rank is required, the additional chip select is included. Figure 2-2 illustrates a 32-bit, dual-rank LPDDR4 implementation. On select devices, 16-bit single-rank LPDDR4 implementation are support, see Figure 2-3.

Note

Though LPDDR4 SDRAMs pin out two separate channels, independent channel use is not supported by this processor.

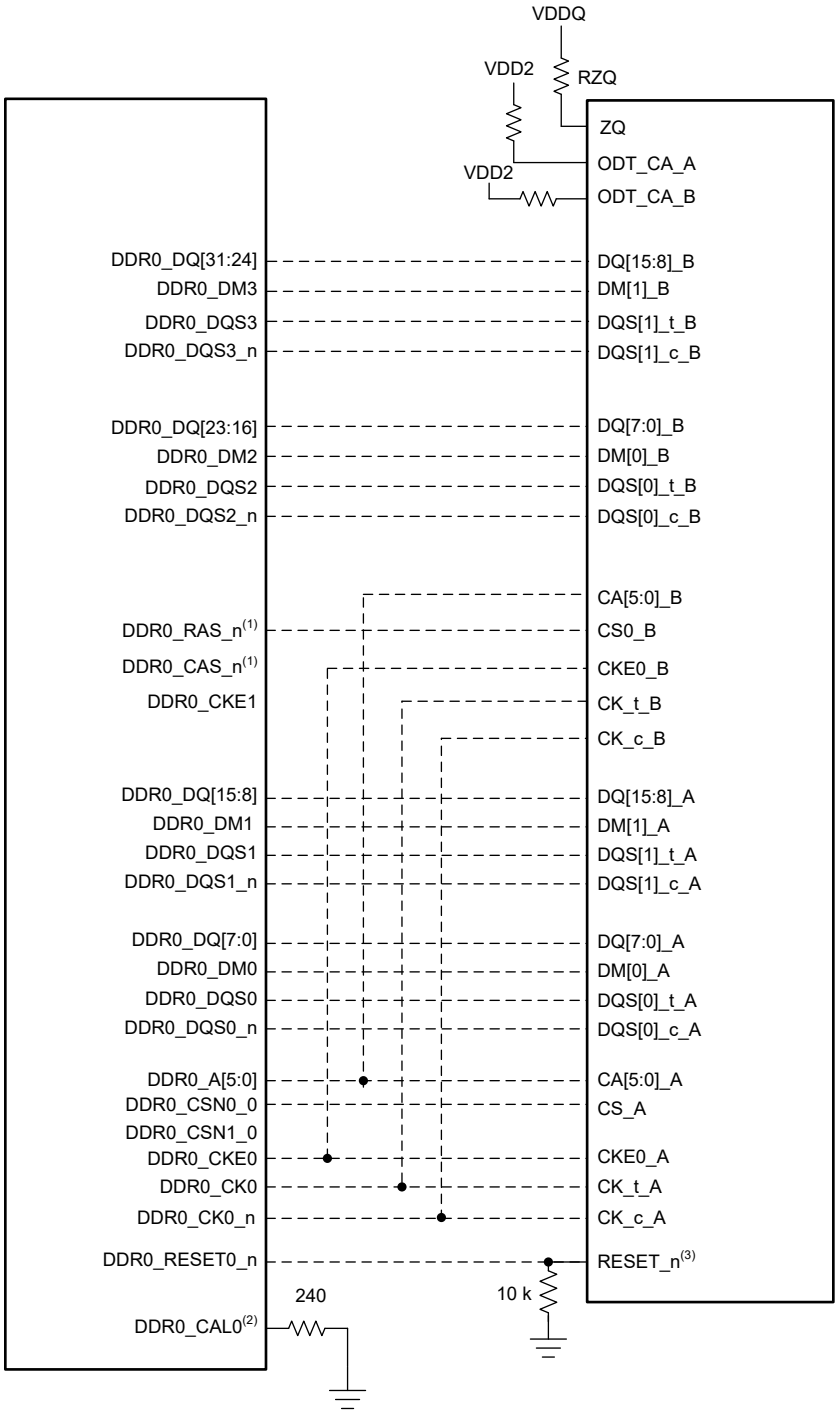

Figure 2-1. 32-Bit, Single-Rank LPDDR4 Implementation

1. When used with LPDDR4, the DDR0_CAS_n and DDR0_RAS_n pins output copies of the chip selects to support point to point connections to Channel B chip selects on the LPDDR4 device. DDR0_CAS_n = copy of CS1 for LPDDR4_CS1_B, DDR0_RAS_n = copy of CS0 for LPDDR4_CS0_B.
2. An external 240 Ω ±1% resistor must be connected between this pin and VSS. The maximum power dissipation for the resistor is 5.2mW. No external voltage should be applied to this pin. Tolerance of ±1% required throughout life of component/product.
3. RESET_n shall have an external 10k pull-down resistor to control RESET low until the DDR controller drives the signal. RESET_n has no length matching requirement.

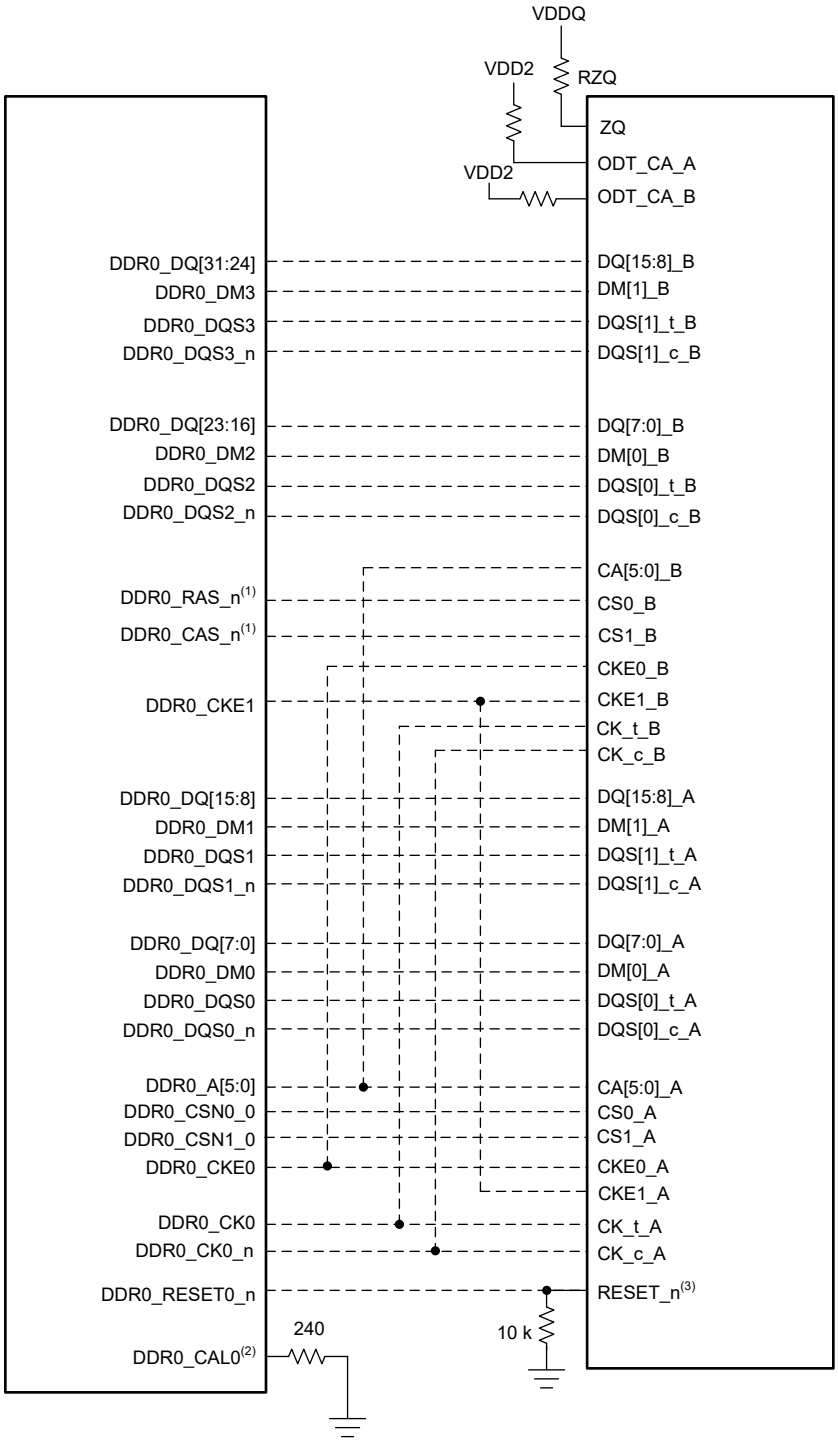

Figure 2-2. 32-Bit, Dual Rank LPDDR4 Implementation

1. When used with LPDDR4, the DDR0_CAS_n and DDR0_RAS_n pins output copies of the chip selects to support point to point connections to Channel B chip selects on the LPDDR4 device. DDR0_CAS_n = copy of CS1 for LPDDR4_CS1_B, DDR0_RAS_n = copy of CS0 for LPDDR4_CS0_B.
2. An external 240 Ω ±1% resistor must be connected between this pin and VSS. The maximum power dissipation for the resistor is 5.2mW. No external voltage should be applied to this pin. Tolerance of ±1% required throughout life of component/product.
3. RESET_n shall have an external 10k pull-down resistor to control RESET low until the DDR controller drives the signal. RESET_n has no length matching requirement.

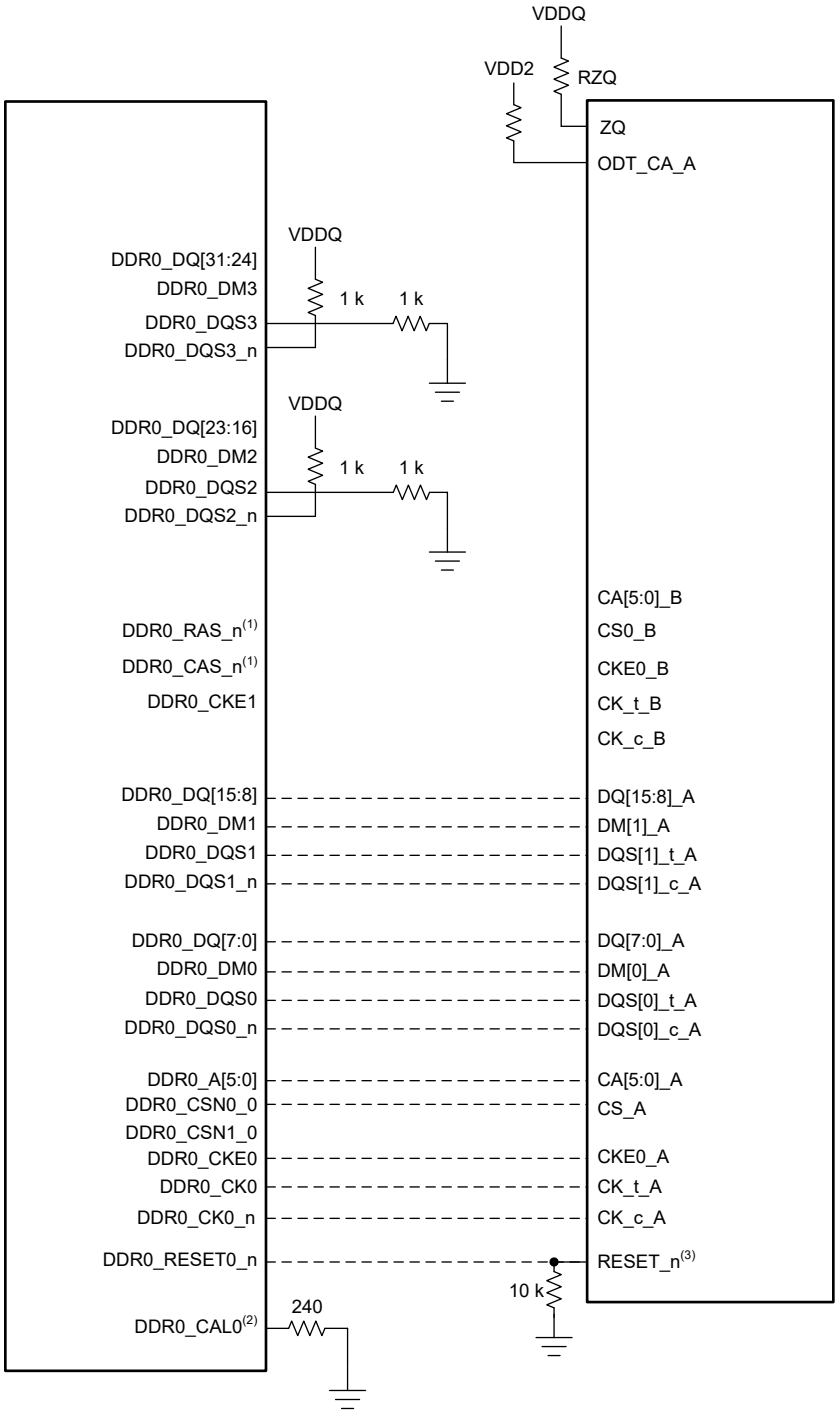

Figure 2-3. 16-Bit, Single Rank LPDDR4 Implementation

1. When used with LPDDR4, the DDR0_CAS_n and DDR0_RAS_n pins output copies of the chip selects to support point to point connections to Channel B chip selects on the LPDDR4 device. DDR0_CAS_n = copy of CS1 for LPDDR4_CS1_B, DDR0_RAS_n = copy of CS0 for LPDDR4_CS0_B.
2. An external 240 Ω ±1% resistor must be connected between this pin and VSS. The maximum power dissipation for the resistor is 5.2 mW. No external voltage should be applied to this pin. Tolerance of ±1% required throughout life of component/product.
3. RESET_n shall have an external 10k pull-down resistor to control RESET low until the DDR controller drives the signal. RESET_n has no length matching requirement.

2.4 Compatible JEDEC LPDDR4 Devices

Table 2-2 shows the parameters of the JEDEC LPDDR4 devices compatible with this interface.

Table 2-2. Compatible JEDEC LPDDR4 Devices

Number	Parameter	MIN	MAX	UNIT
1	Data Rate(1) (2)		4266	MT/s
2	Channel Bit Width	x16	x16	Bits
3	Channels	1	2	-
4	Ranks	1	2	-
5	Die	1	4	-
6	Device Count	1	1	-

(1) For supported data rates/speed grades, see the device-specific data manual.
(2) SDRAMs in faster speed grades can be used, provided they are properly configured to operate at the supported data rates. Faster speed grade SDRAMs may have faster edge rates, which may affect signal integrity. SDRAMs with faster speed grades must be validated on the target board design.

2.5 Placement

Figure 2-4 shows an example placement for the AM62Ax/AM62Px processor and the LPDDR4 memory device. The recommended spacing parameters for the AM62Ax/AM62Px device and the LPDDR4 device are defined in Table 2-3. The placement does not restrict the side of the PCB on which the devices are mounted. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space.

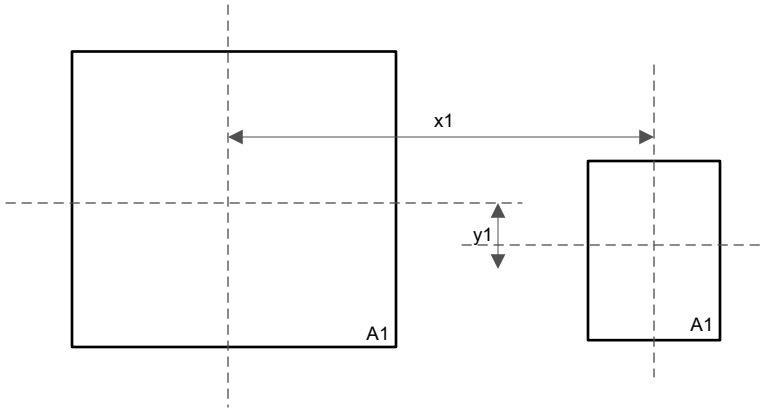

Figure 2-4. AM62Ax/AM62Px and LPDDR4 Example Placement (Top View)

Table 2-3. LPDDR4 Placement Recommendations

Number	Parameter	MIN	MAX	UNIT
1	x1		1200	Mils
2	y1		250	Mils

2.6 LPDDR4 Keepout Region

The region of the PCB used for LPDDR4 circuitry must be isolated from other signals. The LPDDR4 keepout region is defined for this purpose and example is shown in Figure 2-5. The size of this region varies with the placement and DDR routing. Non-LPDDR4 signals should not be routed on the DDR signal layers within the LPDDR4 keepout region. Non-LPDDR4 signals may be routed in this region only if they are routed on other layers separated from the DDR signal layers by a ground layer. No breaks are allowed in the reference ground layers in this region. In addition, a solid VDDS_DDR power plane should exist across the entire keepout region.

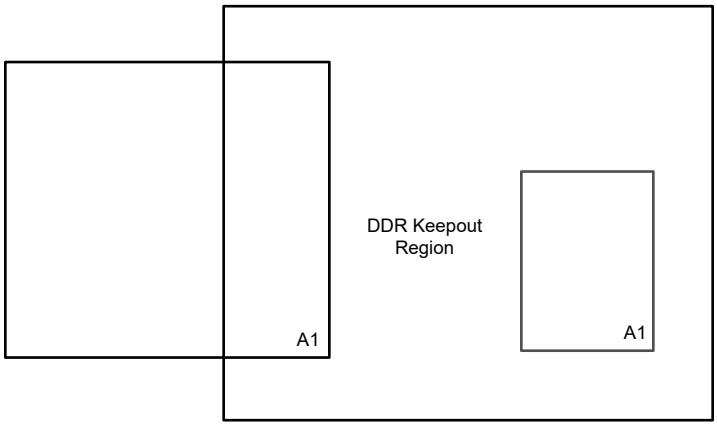

Figure 2-5. Example LPDDR4 Keepout Region for AM62Ax/AM62Px (Top View)

2.7 Net Classes

Routing rules are applied to signals in groups called net classes. Each net class contains signals with the same routing requirements. This simplifies the implementation and compliance of these routes. Table 2-4 lists the clock net classes for the LPDDR4 interface. Table 2-5 lists the signal net classes, and associated clock net classes, for signals in the LPDDR4 interface. These net classes are then linked to the termination and routing rules that follow.

Table 2-4. Clock Net Class Definitions

Clock Net Class	Processor Pin Names
CK0	DDR0_CK0 / DDR0_CK0_n
DQS0	DDR0_DQS0 / DDR0_DQS0_n
DQS1	DDR0_DQS1 / DDR0_DQS1_n
DQS2	DDR0_DQS2 / DDR0_DQS2_n
DQS3	DDR0_DQS3 / DDR0_DQS3_n

Table 2-5. Signal Net Class Definitions

Signal Net Class	Associated Clock Net Class	Processor Pin Names
ADDR_CTRL	CK0	DDR0_A[5:0], DDR0_CS0_n, DDR0_CS1_n, DDR0_CKE0, DDR0_CKE1, DDR0_CAS_n(1), DDR0_RAS_n(1)
BYTE0	DQS0	DDR0_DQ[7:0], DDR0_DM0
BYTE1	DQS1	DDR0_DQ[15:8], DDR0_DM1
BYTE2	DQS2	DDR0_DQ[23:16], DDR0_DM2
BYTE3	DQS3	DDR0_DQ[31:24], DDR0_DM3

(1) When used with LPDDR4, the DDR0_CAS_n and DDR0_RAS_n pins output copies of the chip selects to support point to point connections to Channel B chip selects on the LPDDR4 device. DDR0_CAS_n = copy of CS1 for LPDDR4_CS1_B, DDR0_RAS_n = copy of CS0 for LPDDR4_CS0_B

2.8 LPDDR4 Signal Termination

LPDDR4 memories have software configurable on-die termination for both the data group nets. The DDR subsystem also contains software configurable on-die termination for the address/control group nets. Thus, termination is not required on any DDR signals for an LPDDR4 configuration.

2.9 LPDDR4 VREF Routing

LPDDR4 memories generate their own VREFCA and VREFDQ internally for the address / command bus and data bus, respectively. Similarly, the DDR PHY also provides its own reference voltage for the data group nets during reads. Thus unlike DDR3 and DDR4, VREF does not need to be generated on the board, and there is no required VREF routing for an LPDDR4 configuration.

2.10 LPDDR4 VTT

Unlike DDR3 and DDR4, there is no required termination on the PCB of the address/control bus of an LPDDR4 configuration. All termination is handled internally (on-die). Thus, VTT does not apply for LPDDR4.

2.11 CK and ADDR_CTRL Topologies

The CK and ADDR_CTRL net classes are routed similarly, and are skew matched from the DDR controller in the processor to the LPDDR4 SDRAM to ensure that the ADDR_CTRL signals are properly sampled at the SDRAM. The CK0 net class requires more care because it runs at a higher transition rate and are differential. The CK and ADDR_CTRL topology is balanced 'T'.

Figure 2-6 shows the topology of the CK0 net class. Figure 2-7 and Figure 2-8 shows the topologies for the corresponding ADDR_CTRL_A net class. Note some of the signals within the group are shared between the memory channels, while other signals are dedicated for each channel. Skew matching requirements for the routing segments are detailed in Table 2-6.

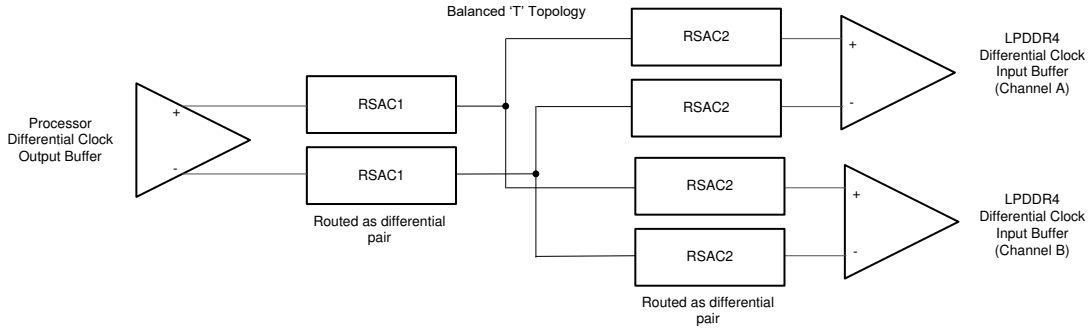

Figure 2-6. LPDDR4 CK Topology

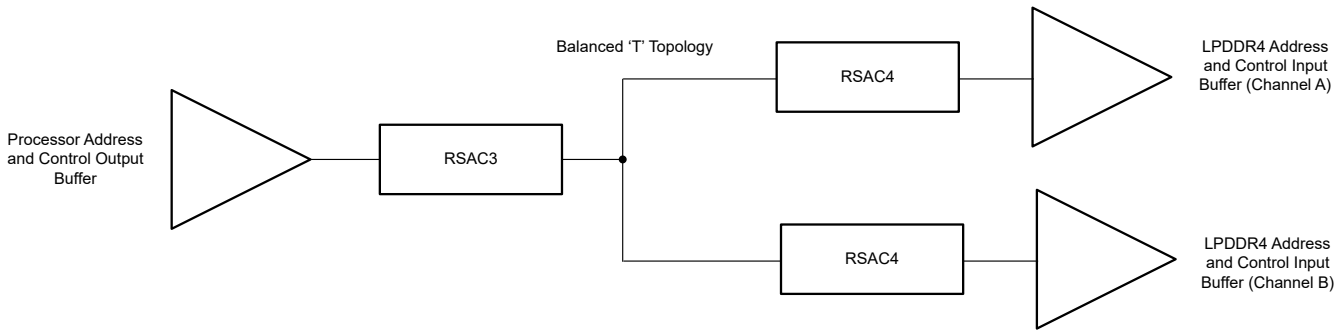

Figure 2-7. LPDDR4 ADDR_CTRL Topology/Branched Signals

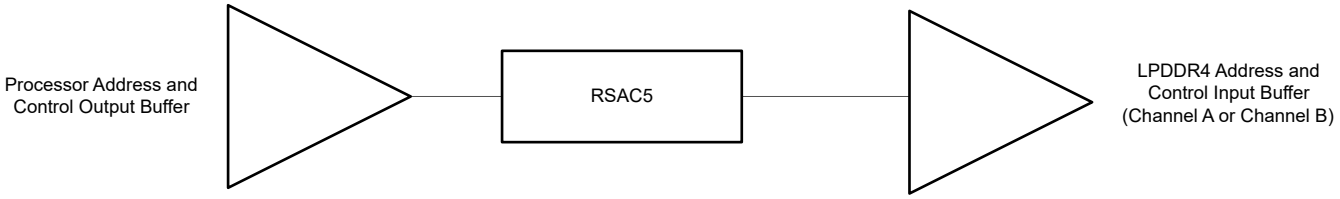

Figure 2-8. LPDDR4 ADDR_CTRL Topology/Point-to-Point Signals

It is recommended to minimize layer transitions during routing. If a layer transition is necessary, it is preferable to transition to a layer using the same reference plane. If this cannot be accommodated, ensure there are nearby stitching vias to allow the return currents to transition between reference planes. The goal is to minimize the size of the return current path thus minimizing the inductance in this path. Lack of these stitching vias results in impedance discontinuities in the signal path that increase crosstalk and signal distortion.

There are no stubs or termination allowed on the nets of the CK and ADDR_CTRL group topologies. All test and probe access points must be in line without any branches or stubs.

2.12 Data Group Topologies

The data line topology is always point-to-point for LPDDR4 implementations, and is broken up into four different byte lanes. It is recommended to minimize layer transitions during routing. If a layer transition is necessary, it is better to transition to a layer using the same reference plane. If this cannot be accommodated, ensure there are nearby ground vias to allow the return currents to transition between reference planes. The goal is to provide a low inductance path for the return current. To optimize the skew matching, TI recommends routing all nets within a single data routing group on one layer where all nets have the exact same number of vias and the same via barrel length.

DQSP and DQSN lines are point-to-point signals routed as a differential pair. Figure 2-9 illustrates the DQSP/N connection topology.

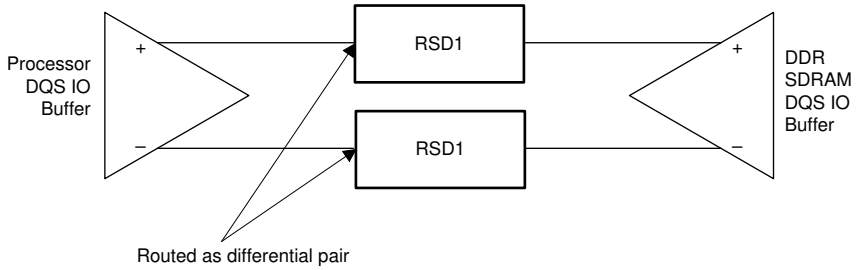

Figure 2-9. LPDDR4 DQS Topology

DQ and DM lines are point-to-point signals routed as single-ended. Figure 2-10 illustrates the DQ and DM connection topology.

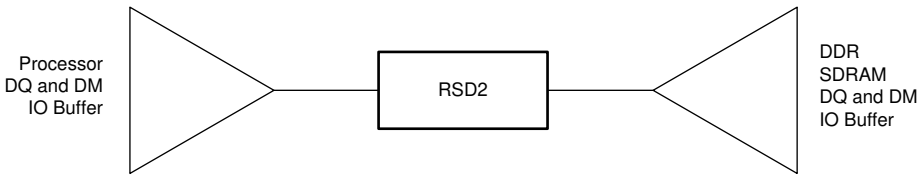

Figure 2-10. LPDDR4 DQ/DM Topology

There are no stubs or termination allowed on the nets of the data group topologies. All test and probe access points must be in line without any branches or stubs.

2.13 CK0 and ADDR_CTRL Routing Specification

Skew within the CK0 and ADDR_CTRL net classes directly reduces setup and hold margin for the ADDR_CTRL nets. Thus, this skew must be controlled. The routed PCB track has a delay proportional to its length. Thus, the delay skew must be managed through matching the lengths of the routed tracks within a defined group of signals. The only way to practically match skew on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. Consider Z-axis delays (VIAs) with accurate stackup information during analysis.

The DDR PHY includes a per-bit deskew feature, enabled by default. This capability allows signal routing with looser delay matching tolerance as specified in Table 2-6. If this feature is disabled, skews must be tightly matched. Measure the propagation delay of each signal from the SoC die to the DRAM device pin. The designer is free to length match using smaller tolerance than values shown in the table. Refer to Appendix: SOC Package Delays during the initial PCB design phase. Perform a simulation and generate a delay report to confirm skews are within the specified tolerance.

Table 2-6 lists the limits for the individual segments that comprise the routing from the processor to the SDRAM. These segment lengths coincide with the CK0 and ADDR_CTRL topology diagram shown previously in Figure 2-6, Figure 2-7, and Figure 2-8. By controlling the routed lengths for the same segments of all signals in a routing group, the signal delay skews are controlled. Most PCB layout tools can be configured to generate reports to assist with this validation. If this cannot be generated automatically, this must be generated and verified manually.

Delay reports from PCB layout tools use a simplified calculation based on a constant propagation velocity factor. To get the design close to success prior to simulation, TI recommends initially skew matching in PCB layout tool to a target less than 20% of the limit in Table 2-6. To ensure the PCB design meets all requirements, it is required the design be simulated and those results compared with the simulation results defined in Section 3. Simulations must be power-aware and consider the entire system IO buffers, SOC package, PCB traces, memory package(s), on-die decoupling circuits, and number of die.

Table 2-6. CK0 and ADDR_CTRL Routing Specifications

Number	Parameter	MIN	TYP	MAX	UNIT
LP4_ACRS1	Propagation delay of net class CK0 (RSAC1 + RSAC2)			250 (1)	ps
LP4_ACRS2	Propagation delay of net class ADDR_CTRL (RSAC3 + RSAC4, RSAC5)			250 (1)	ps
LP4_ACRS3	Skew within net class CK0 (Skew of DDR0_CK0 and DDR0_CK0_n) (RSAC1 + RSAC2)			0.75 (2) (3)	ps
LP4_ACRS5	Skew between each T-branch signal pair RSAC2 or RSAC4 Skew (4)	-0.1	0	0.1	ps
LP4_ACRS6	Skew across ADDR_CTRL and CK0 clock net class, relative to propagation delay of CK0 net class (RSAC1 + RSAC2) - (RSAC3 + RSAC4), (RSAC1 + RSAC2 - RSAC5)(5)	-75 (3) (6)		75 (3) (6)	ps
LP4_ACRS7	VIAs per trace			4 (1)	VIAs
LP4_ACRS8	VIA Stub Length		20 (7)		Mils
LP4_ACRS9	VIA count difference			0 (8)	VIAs
LP4_ACRS10	Center-to-center CK0 to other LPDDR4 trace spacing	5w(9)			
LP4_ACRS11	Center-to-center ADDR_CTRL to other LPDDR4 trace spacing	5w(9)			
LP4_ACRS12	Center-to-center ADDR_CTRL to self or other ADDR_CTRL trace spacing	3w(9)			
LP4_ACRS13	CK0 center-to-center spacing (10)	See note below			
LP4_ACRS14	CK0 spacing to non-DDR net	5w(9)			

(1) Max value is based upon conservative signal integrity approach. FR4 material assumed with Dk ~ 3.7 - 3.9 & Df ~ 0.002. This value could be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.
(2) Recommendation for PCB layout tool design. Required to be verified by simulation(11), confirm JEDEC defined Vix_DQS_ratio (20%) and Vix_CK_ratio (25%) are satisfied, also need to have good eye margins - refer to Section 3.5.3.1.
(3) Consider the delays from SOC die pad to the DRAM pin (ie. delays of SOC package + delays of PCB upto the DRAM pin. DRAM package delays are omitted). Consider one leg of any T-branch trace segments when delay matching. Refer to Appendix: SOC Package Delays.

(4) Recommended skew control on T-branch trace segments (Balanced-T) is intended to optimize signal integrity (waveform reflections). It is not required nor recommended to match skew across all T-branch trace segments, just for each branch of a specific signal.
(5) Recommend routing net classes CK0 and ADDR_CTRL on same signal layer for better skew control.
(6) Simulation(11) must be performed and the delay report analyzed to ensure skew is within the limit. Delay reports from PCB layout tools use a simplified calculation based on a constant propagation velocity factor. TI recommends initially skew matching in PCB layout tool to a target less than 20% of the limit.
(7) VIA stub control (micro VIA or backdrilling) may be required if operating LPDDR4 above 3200 Mbps depending on simulation(11) results.
(8) VIA count difference may increase by 1 only if accurate 3-D modeling of the signal flight times – including accurately modeled signal propagation through VIAs – has been applied to ensure skew maximums are not exceeded.
(9) Center-to-center spacing is allowed to fall to minimum 2w for up to 500 mils of routed length (only near endpoints). Spacing minimums may be relaxed if simulations(11) accurately capture crosstalk between neighboring victim and aggressor traces and show good margin. Consider also VIA spacing. Signals with adjacent VIAs near SOC should not also have adjacent VIAs near the DRAM.
(10) P to N spacing set to ensure proper differential impedance. The designer must control the impedance so that inadvertent impedance mismatches are not created. Generally speaking, center-to center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the single-ended impedance, Zo, on that layer. Refer to impedance targets in Table 1-1.
(11) Simulation refers to a power-aware IBIS Signal Integrity (SI) simulation. Simulate across process, voltage, and temperature (PVT). Refer to Section 3.

2.14 Data Group Routing Specification

Skew within the Byte signal net class directly reduces the setup and hold margin for the DQ and DM nets. As described with the ADDR_CTRL signal net class and associated CK0 clock net class, this skew must be controlled. The data byte skew must be managed through controlling the lengths of the routed tracks within a defined group of signals. The only way to practically match skews on a PCB is to lengthen the shorter traces up to the length of the longest net in the net class and its associated clock. Consider Z-axis delays (VIAs) with accurate stackup information during analysis.

The DDR PHY includes a per-bit deskew feature, enabled by default. This capability allows signal routing with looser delay matching tolerance as specified in Table 2-7. If this feature is disabled, skews must be tightly matched. Measure the propagation delay of each signal from the SoC die to the DRAM device pin. The designer is free to length match using smaller tolerance than values shown in the table. Refer to Appendix: SOC Package Delays during the initial PCB design phase. Perform a simulation and generate a delay report to confirm skews are within the specified tolerance.

Note

It is not required nor recommended to match the lengths across all byte lanes. Length matching is only required within each byte.

Table 2-7 contains the routing specifications for the Byte0, Byte1, Byte2, and Byte3 routing groups. Each signal net class and its associated clock net class is routed and matched independently. These parameters are recommendations only, intended to get the design close to success prior to simulation. To ensure the PCB design meets all requirements, it is required the design be simulated and those results compared with the simulation results defined in Section 3.

Table 2-7. Data Group Routing Specifications

Number	Parameter	MIN	TYP	MAX	UNIT
LP4_DRS1	Propagation delay of net class DQSx (RSD1)			250 (1)	ps
LP4_DRS2	Propagation delay of net class BYTEx (RSD2)			250 (1)	ps
LP4_DRS3	Difference in propagation delays of CK0 pair and each DQS pair. (RSAC1 + RSAC2 - RSD1)(2)	0 (3) (4)		3(3) (4)	tCK
LP4_DRS4	Skew within net class DQSx Skew of DQSx to DQSx_n (RSD1)			1.5 (4) (5)	ps
LP4_DRS5	Skew across DQSx and BYTEx net classes. (Skew of RSD1 and RSD2) (6)			150 (3) (4)	ps
LP4_DRS6	Difference in propagation delays of shortest DQ/DM bit in BYTEx and respective DQSx. (RSD2 - RSD1)(7)	-49 (3) (4)			ps
LP4_DRS7	VIAs Per Trace			2 (1)	VIAs
LP4_DRS8	VIA Stub Length		40 (8)		Mils
LP4_DRS9	VIA Count Difference			0 (9)	VIAs
LP4_DRS10	RSD1 center-to-center spacing (between clock net class)	5w (10)			
LP4_DRS11	RSD1 center-to-center spacing (within clock net class) (11)	See note below			
LP4_DRS12	RSD2 center-to-center spacing (between signal net class)	5w (10)			
LP4_DRS13	RSD2 center-to-center spacing (to self or within signal net class)	3w (10)			

(1) Max value is based upon conservative signal integrity approach. FR4 material assumed with Dk ~ 3.7 - 3.9 & Df ~ 0.002. This value could be extended only if detailed signal integrity analysis of rise time and fall time confirms desired operation.
(2) Propagation delay of CK0 pair must be greater than propagation delay of each DQS pair. Consider one leg of any T-branch trace segments when delay matching.
(3) Simulation(12) must be performed and the delay report analyzed to ensure delays are within the limit. Delay reports from PCB layout tools use a simplified calculation based on a constant propagation velocity factor. TI recommends initially delay matching in PCB layout tool to a target less than 20% of the limit.
(4) Consider the delays from SOC die pad to the DRAM pin (ie. delays of SOC package + delays of PCB upto the DRAM pin. DRAM package delays are omitted). Refer to Appendix: SOC Package Delays.

(5) Recommendation for PCB layout tool design. Required to be verified by simulation(12), confirm JEDEC defined Vix_DQS_ratio (20%) and Vix_CK_ratio (25%) are satisfied, also need to have good eye margins. Refer to Section 3.5.3.1.
(6) Skew matching is only done within a byte including DQS. Skew matching across bytes is neither required nor recommended.
(7) Although the table specifies that the propagation delay of DQ/DM bits within BYTEx may be less than the propagation delay of the respective DQSx, it is recommended for the DQSx propagation delay to be less than the propagation delay of each DQ/DM bit in BYTEx.
(8) VIA stub control (micro VIA or backdrilling) may be required if operating LPDDR4 above 3200 Mbps depending on simulation(12) results.
(9) VIA count difference may increase by 1 only if accurate 3-D modeling of the signal flight times – including accurately modeled signal propagation through VIAs – has been applied to ensure skew maximums are not exceeded.
(10) Center-to-center spacing is allowed to fall to minimum 2w for up to 500 mils of routed length (only near endpoints). Spacing minimums may be relaxed if simulations(12) accurately capture crosstalk between neighboring victim and aggressor traces and show good margin. Consider also VIA spacing. Signals with adjacent VIAs near SOC should not also have adjacent VIAs near the DRAM.
(11) P to N spacing set to ensure proper differential impedance. The designer must control the impedance so that inadvertent impedance mismatches are not created. Generally speaking, center-to center spacing should be either 2w or slightly larger than 2w to achieve a differential impedance equal to twice the single-ended impedance, Zo, on that layer. Refer to impedance targets in Table 1-1.
(12) Simulation refers to a power-aware IBIS Signal Integrity (SI) simulation. Simulate across process, voltage, and temperature (PVT). Refer to Section 3.

2.15 Channel, Byte, and Bit Swapping

All address/control signals must be routed from the DDR controller to the LPDDR4 memory as described in the diagrams in Section 2.3. Address/control signals cannot be swapped with other signals. Data bit (DQx) swapping within a byte (for example, swapping D2 with D3) is allowed, but data bit DQx swapping across bytes (for example, swapping D4 and D13) is not allowed. When swapping bytes, all of the associated signals of the byte (DQx, DQSx, and DM) must be swapped together. In addition, byte lanes within a channel (for example, swapping byte 0 and 1) is allowed, but swapping byte lanes across channels (for example, swapping bytes 0 and 3) is not allowed. Byte lanes 0 and 1 must be routed to channel A of the LPDDR4 memory, and byte lanes 2 and 3 must be routed to channel B of the LPDDR4 memory. Use the DDR Subsystem Register Configuration Tool in SysConfig (*https://dev.ti.com/sysconfig*) to describe how the bits are swapped.

2.16 Data Bus Inversion

Data Bus Inversion (DBI) is recommended to reduce supply/ground noise and to improve the data eye. Therefore, the DDR Subsystem Register Configuration Tool enables Write DBI by default for LPDDR4 configurations.

3 LPDDR4 Board Design Simulations

This section is intended to provide an overview of the basic system-level board extraction, simulation, and analysis methodologies for high-speed LPDDR4 interfaces. This is an essential step to ensure the PCB design meets all the requirements to operate the targeted speeds.

3.1 Board Model Extraction

Note

This section contains various information from J7 devices and board designs. The specific details only apply to J7 board designs, but are provided here as an examples for AM62Ax/AM62Px board designs.

The board level extraction guidelines listed below are intended to work in any EDA extraction tool and are not tool-specific. It is important to follow the steps outlined in Section 3.2 through Section 3.4 immediately after completing touchstone model extractions. The design should be checked with these steps prior to running IBIS simulations.

1. For DDR extractions, extract power (VDDS_DDR/VDDQ) and signal nets together in a 3D-EM solver.
2. Use wide-band models. It is recommended to extract from DC to at least until 6x the Nyquist frequency (for example, for LPDDR4-3733 extract the model at least until 11.2 GHz).
3. Check the board stack-up for accurate layer thickness and material properties.
   a. It is recommended to use Djordjevic-Sarkar models for the dielectric material definition.
4. Use accurate etch profiles and surface roughness for the signal traces across all layers in the stack-up.
5. If the board layout is cut prior to extraction (to reduce simulation time), define a cut boundary that is at least 0.25 inch away from the signal and power nets.
6. Check the via padstack definitions.
   a. Ensure that the non-functional internal layer pads on signal vias are modeled the same way they would be fabricated.
   b. These non-functional internal layer pads on signal vias are not recommended by TI.
7. Use Spice/S-parameter models (typically available from the vendor) for modeling all passives in the system.
8. Obtain SoC package model for AM62Ax/AM62Px from your TI representative.

3.2 Board-Model Validation

The extracted board models need to be checked for the following properties:

- Passivity: This ensures that the board model is a passive network and does not generate energy
- Causality: This ensures that the board model obeys the causal relationship (output follows input).

These checks can be performed in any standard EDA simulator or extraction engine.

3.3 S-Parameter Inspection

Once the extracted S-parameters have been verified as causal and passive, the S-parameter plots should be inspected. It is recommended to check for the following:

- Insertion Loss: The single-ended insertion loss is recommended to stay within 0 to 10 dB up to 3 times the Nyquist frequency of operation. For example, if the target frequency is 8 Gbps (4GHz Nyquist), the single-ended insertion loss should stay under 10 dB up to 12 GHz.
- Return Loss: The single-ended return loss is recommended to be less than 15 dB up to 3 times the Nyquist frequency.
- Near and Far end crosstalk (FEXT/NEXT): The FEXT and NEXT are recommended to be under 25 dB for frequencies up to 3 times the Nyquist frequency.

The S-Parameter inspection plots are not pass/fail tests, but rather its more of a guide to check if the design has a reasonable chance of performing a the required level.

3.4 Time Domain Reflectometry (TDR) Analysis

As a lot of the design fixes are targeted towards maintaining uniform trace impedance, an important analysis method used in assessing the quality of the design is the Time Domain Reflectometry (TDR) analysis. This plots the impedance of a trace as a function of its length, as shown in Figure 3-1.

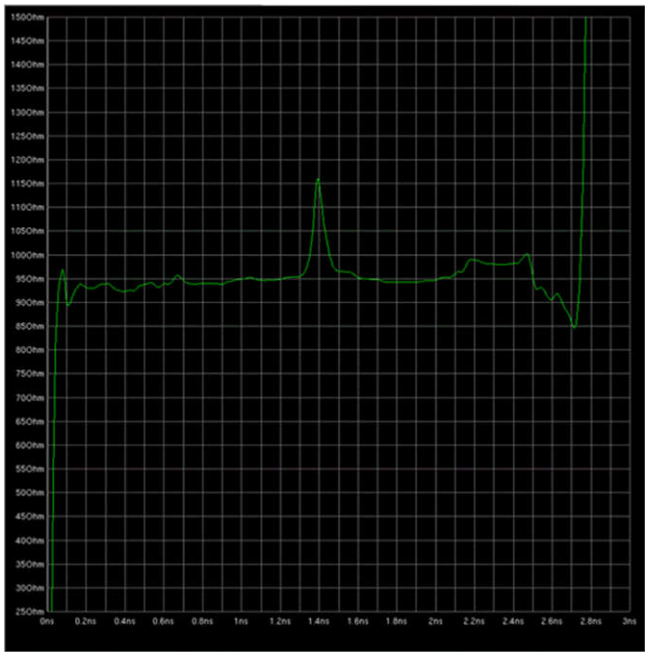

Figure 3-1. TDR Plot Example With Impedance Mismatch

As shown in Figure 3-1, the TDR plot highlights impedance discontinuities in the trace from one end to the other. This method depends on a reflected waveform from the far-end of the trace. The delay in the plot corresponding to a particular point in the trace actually corresponds to 2 times the distance of that point from the source, owing to the round trip time. This needs to be factored in for assessing the source of impedance discontinuities.

The TDR plot can be generated by reading in the S-parameter models generated by the extraction tool and assessing them in “Time-Domain” mode. A standard EDA simulator such as HyperLynx can perform this function. It is recommended to optimize the design to within a ± 5% deviation from the nominal trace impedance.

The TDR plots are not pass/fail tests, but rather is more of a guide to check if the design has a reasonable chance of performing a the required level.

3.5 System Level Simulation

The methodology for validating the DDR interface is outlined in this section. LPDDR4 interfaces, as defined in the JEDEC specification, uses eye masks defined at a target BER (Bit Error Rate) to determine pass or fail

for signal integrity. It is essential to perform channel simulations using IBIS models to generate the signal eye diagrams at the targeted BER. These are introduced for memory interfaces starting from LPDDR4

3.5.1 Simulation Setup

Set up the system-level schematic in the simulator by connecting the SOC IBIS model, board model, power supplies, DRAM package model, and DRAM IBIS model. A typical system-level DDR schematic is shown in Figure 3-2.

Note

Be aware of the DRAM configuration (number of dies in the package, number of ranks, and number of channels) while setting up the system schematic. Be aware the DRAM configuration may also include On-Die Decoupling Circuit.

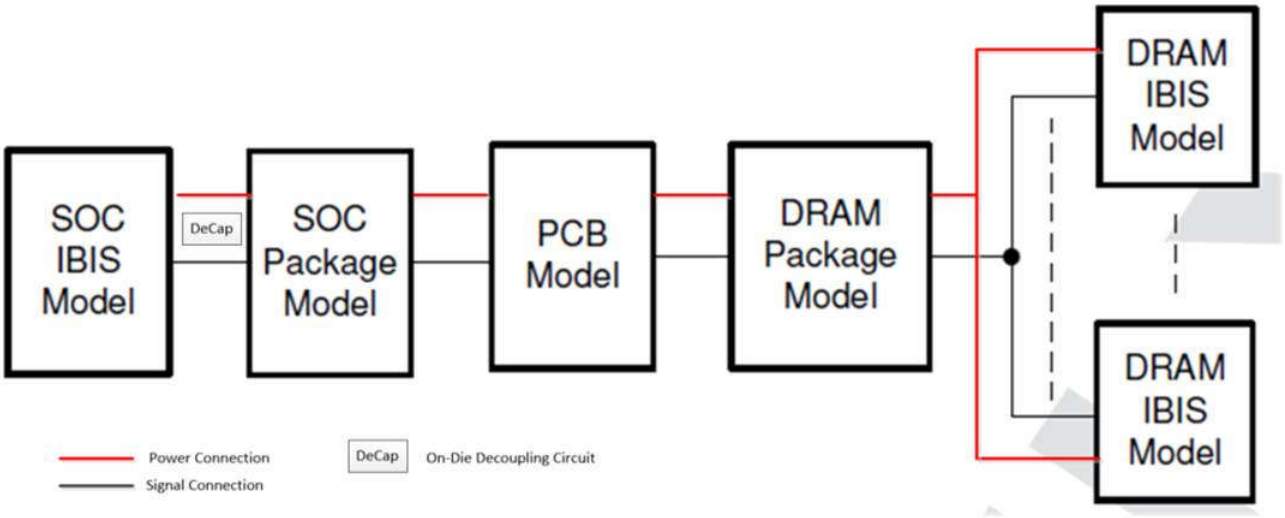

Figure 3-2. Typical System-Level DDR Schematic

- LPDDR4 simulations require power-aware IBIS models for the controller and the memory along with a simulator that supports channel simulations for DDR interfaces.
- SPICE-based transistor-level simulations cannot be used for generating BER signal eyes. Use a simulator that can handle power-aware IBIS simulations and can run channel simulations for the DDR interface.
- IBIS models reduce simulation time with minimal loss in accuracy compared with SPICE-based transistor-level simulations. IBIS models starting from version 5.0 are power-aware models which enables Simultaneous Switching Output (SSO) noise simulations. The TI IBIS model is a power-aware IBIS model.
- Use SPICE models to accurately model the on-die decoupling capacitance on the DDR supply net for both – controller and DRAM. This ensures accurate power noise and Power Supply Induced Jitter (PSIJ) estimation in DDR simulations. The on-die decoupling capacitance information for the DRAM can be obtained from the DRAM vendor.
- Use SPICE or S-parameter files to model the DRAM package. This can be requested from the DRAM vendor. EBD models are not recommended.
- Note that inside the SoC IBIS model, there is a section for the package that contains an RLC matrix for all signal and power nets including DDR. Use either this package model inside the ibis model, or the SOC package s-parameter model as shown in Figure 3-2. Do not use both in your simulations.

- AM62Ax/AM62Px model for the on-die decoupling capacitance on the DDR supply net:

```
****************************************
* On-die Decoupling circuit for AM62Ax/AM62Px (DIE_VDDS_DDR to VSS)
****************************************
* Notes:
* Includes on-die decoupling for all DDR signals
*
* This subcircuit should be added across the AM62Ax/AM62Px IBIS model's
* DIE_VDDS_DDR and VSS pins
*
****************************************
* x_decouple DIE_VDDS_DDR vss_die AM62A_P_ondie_decoupling_alldq
****************************************
.SUBCKTAM62A_P_ondie_decoupling_alldq DIE_VDDS_DDR vss_die
Cvddq_c  DIE_VDDS_DDR DIE_VDDS_DDR_c 2.6e-9
Rvddq_c  vss_die DIE_VDDS_DDR_c 42.04e-3
.ENDS
```

3.5.2 Simulation Parameters

It is important to configure the simulation to exercise the system to real, but worst case parameters.

- Use the worst-case bit pattern to excite the system. The simulator should be able to generate the worst-case bit pattern based on channel characterization.
- Select the controller and DRAM models (sets the drive strength, ODT, VOH levels, and so forth) from the IBIS files which work best for the system.
  - This is typically an iterative process.
  - Every system is unique and the optimal settings for these parameters can vary from system to system.

Table 3-1. Example Data Write ODI/ODT Optimization

Pkg Byte	Board	ODI Ω	ODT Ω	Total EW Margin (ps)	Total EH Margin (mV)B
B3	J7 370HR 10L Ref B3, No BD	40	40	50.28	15.66
B3	J7 370HR 10L Ref B3, No BD	40	48	27.62	11.76
B3	J7 370HR 10L Ref B3, No BD	40	40	33.52	2.92
B3	J7 370HR 10L Ref B3, No BD	48	48	1.54	0.86

- Data bus and address bus ODT and drive strength values can be set independently. As an example, the J7 EVM board (which supports LPDDR4 at similar speeds) used 40-Ω ODT for data read/writes and 80-Ω for CA bus. Drive strength of 40-ohms for data read/write and CA.
  - Data READ Controller model - lpddr4_odt_40, lpddr4_odt_40_diff
  - Data WRITE Controller model - lpddr4_ocd_40p_40n, lpddr4_ocd_40p_40n_diff
  - CA/CLK Controller model - lpddr4_ocd_40p_40n, lpddr4_ocd_40p_40n_diff
- Set up the channel simulation parameters. These typically consists of the data rate, ignore time/bits, minimum number of bits, bit sampling rate, BER floor, number of bits for display, types of BER eyes (voltage and/or timing), and target BER.
  - To determine the minimum number of bits one can run a series of channel simulations with different number of bits. The BER signal eye (and margins) tend to converge after a certain minimum number of bits. This should help determining the minimum number of bits to be used for the system.
  - Run channel simulations to generate the eye diagrams at LBER of -16.
- Run channel simulations with non-ideal power settings at different PVT corners. It is recommended to run the simulations at least at the SSHT and FFLT corners.

3.5.3 Simulation Targets

Once the simulation successfully completes, generate the DDR analysis reports from the simulation tool. There are several different parameters to be verified, detailed in this section. Each parameter is pass/fail, meaning each must meet the specified target to ensure the design has sufficient margin to operate at the target data rates.

Use the appropriate JEDEC Vref parameters (Vref_min, Vref_max, Vref_step, and Vref_set_tol) and mask parameters (shape, height, width).

3.5.3.1 Eye Quality

The Vix_DQS ratio and Vix_CK ratio for data write and CA bus simulations are to be verified, at the DRAM pin/BGA. Figure 3-3 from the JEDEC specification explains how to measure the Vix ratio, as well as define the ration requirement(s).

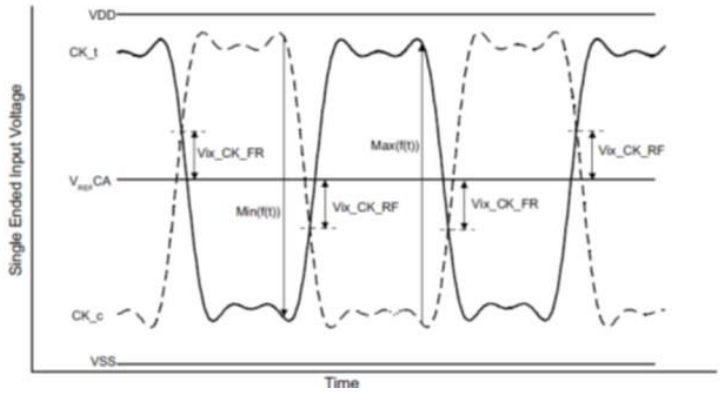

Figure 3-3. Vix_CK and Vix_DQS Ratio for Eye Quality

Table 3-2. Vix_CK and Vix_DQS Ratio for Eye Quality

Symbol	Data Rate						Unit	Note
	1600/1867		2133/2400/3200		3733/4266			
Vix_CK_ratio	-	25	-	25	-	25	%	(1), (2)
Vix_DQS	-	20	-	20	-	20	%	(1), (2)

(1) Vix_CK_Ratio is defined by the equation: Vix_CK_Ratio = Vix_CK_FR|Min(f(t))|
(2) Vix_CK_Ratio is defined by the equation: Vix_CK_Ratio = Vix_CK_RF|Min(f(t))|

3.5.3.2 Delay Report

The required interconnect delays for DQ, DQS, CA, and CLK are listed in Table 2-6 and Table 2-7. The values listed as 'Typical' are only recommendations. Any minimum/maximum value is a requirement. One key requirement is to ensure the CK delay is greater than any DQS delay. DQSx delays should also be less than the DQ/DM delays in their respective BYTEx. Consider the complete system from SOC die pad, through the PCB, to the pins of the memory package.

3.5.3.3 Mask Report

The minimum jitter and noise margins are to be captured with respect to the eye mask(s). This masks are data rate dependent, and includes:

- Data read eye mask at the SOC die pad for functionality testing
- Data write eye mask (JEDEC spec) at the DRAM pin/BGA for compliance testing
- CA bus eye mask (JEDEC spec) at the DRAM pin/BGA for compliance testing

There should be at least 2 sets of eye diagrams generated by the simulator:

- Vref set to the optimal Vref of the byte offset by the Vref_set_tol in the positive direction (Vref_set_tol is defined in JEDEC spec)
- Vref set to the optimal Vref of the byte offset by the Vref_set_tol in the negative direction

The system-level margins are the worst case noise and jitter margins from all eye diagram measurements listed above (across SSHT and FFLT corners). For all waveforms captured at the DRAM device, margins should be calculated at both the BGA pin and the DRAM pad.

Table 3-3. LPDDR4 Eye Mask Definitions/Requirements

Parameter	Mask Shape	LPDDR4-3200	LPDDR4-3733
CA eye mask TclVW	Rectangular (1)	0.3 UI (1)	(2)
CA eye mask VclVW	Rectangular (1)	155 mV (1)	(2)
Write eye mask TdlVW	Rectangular (1)	0.25 UI (1)	(2)
Write eye mask VdlVW	Rectangular (1)	140 mV (1)	(2)
Read eye mask TdlVW	Diamond	0.61 UI	0.66 UI
Read eye mask VdlVW	Diamond	140 mV	140 mV

(1) Copied from JEDEC specification: Low Power Double Date Rate 4 (LPDDR4).
(2) For details, contact the DRAM vendor.

Figure 3-4 through Figure 3-6 show the eye mask definitions translated to eye diagrams within captured waveforms.

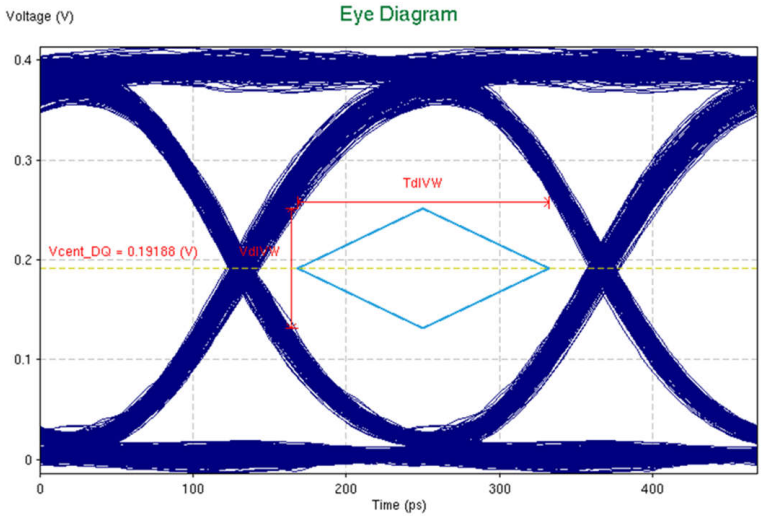

Figure 3-4. Example Simulated LPDDR4-4266 Read Eye With Diamond-Shaped Eye Mask

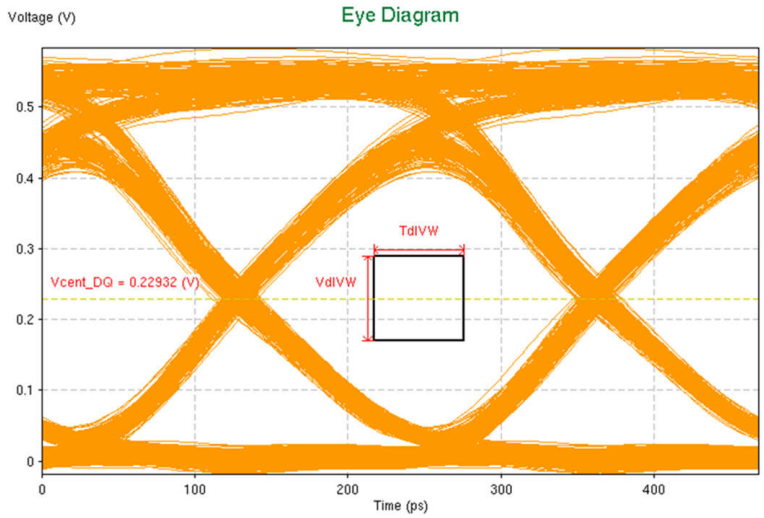

Figure 3-5. Example Simulated LPDDR4-4266 Write Eye With Rectangular JEDEC Eye Mask

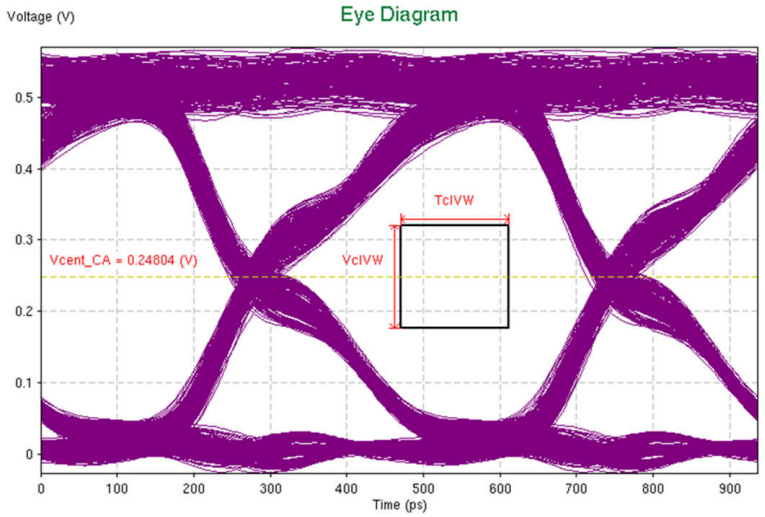

Figure 3-6. Example Simulated LPDDR4-4266 CA Eye With Rectangular JEDEC Eye Mask

3.6 Design Example

3.6.1 Stack-Up

These guidelines recommend a 10- or 12-layer PCB stack-up for full device entitlement. Below are 10- and 12-layer example stack-ups:

- Designs using FR4 products like 370HR are supported, but also recommend higher speed materials like ISOLA I-Speed (or equivalent) for increased margin. IT180A is also another material to help with cost vs. performance tradeoffs
- This example routes data groups on layers 2 and 4. While this minimizes the via travel and therefore reduces via-to-via coupling, but it leaves a longer via stub, which might require back-drill.
- In the 10-layer example, dynamic CA signals are routed on layer 7, and more static control signals routed on layer 9.

Table 3-4. Example 10-layer PCB Stackup for LPDDR4 (J7 EVM)

Layer No	Stackup	Routing Plan Highest Priorities and Layer
	Solder mask	
1	TOP - PWR/SIG	BGA breakouts/VDD_CPU, VDD_CORE and VDD_DDR_1V1
2	PWR/SIG	VDD_CPU and CORE/LPDDR (DBG #3/#1, CAT-Branches)
3	GND	REF
4	PWR/SIG	VDDA_PHYCORE_0V8, VDD_xxx, 0V85/LPDDR (DBG #2/#0)
5	PWR/GND	VDDA_0V8_xxx and GND flood for LPDDR4
6	PWR/GND	VDD_xxx, VDDA_xxx supplies and GND flooded for LPDDR4
7	SIG/PWR	VDD_xxx, VDDA_xxx/LPDDR (Dynamic CA, Trunks)/SERDES
8	GND	REF
9	SIG/PWR	VDD_xxx, VDDA_xxx/LPDDR (static CA)
10	BOTTOM - SIG/PWR	BGA breakouts/Pwr and GND plan segments
	Solder mask	

Table 3-5. Example 12-layer PCB Stackup for LPDDR4 (AM62Ax LP SK EVM)

Layer No	Stackup	Routing Plan Highest Priorities and Layer
	Solder mask	
1	TOP - PWR/SIG	BGA breakouts, VDD_LPDDR4, GND
2	GND	REF
3	PWR/SIG	VDDA_1V8, GND, LPDDR (DBG #3/#1, CA T-Branches), LVCMOS escape
4	GND	REF
5	SIG/GND	GND, LPDDR (DBG #2/#0), LVCMOS escape
6	PWR/GND	GND (under LPDDR), VDD_CORE, VDDR_CORE, VDDA_1V8, VDDSHVx
7	PWR	DVDD_3V3, DVDD_1V8, VDD1_LPDDR4_1V8
8	PWR	VDD_CORE, VDD_LPDDR4, VDDA_x
9	GND	REF
10	SIG/GND	GND, LPDDR (CA point-to-point, CA Trunks), LVCMOS escape
11	GND	REF
12	BOTTOM - SIG/PWR	GND, decaps, LVCMOS escape
	Solder mask	

Table 3-6. Example 12-layer PCB Stackup for LPDDR4 (AM62Px SK EVM)

Layer No	Stackup	Routing Plan Highest Priorities and Layer
	Solder mask	
1	TOP - PWR/SIG	BGA breakouts, VDD_LPDDR4, GND
2	GND	REF
3	PWR/SIG	VDDA_1V8, GND, LPDDR (DBG #3/#1, CA T-Branches), LVCMOS escape
4	GND	REF
5	SIG/GND	GND, LPDDR (DBG #2/#0), LVCMOS escape
6	GND	REF
7	PWR	VDD_CORE, VDD_LPDDR4, DVDD_3V3
8	PWR/GND	VDD1_LPDDR4_1V8, GND, VDDA_x
9	PWR/GND	GND, VDDR_CORE, VDDA_1V8, DVDD_3V3, DVDD_1V8
10	SIG/GND	GND, LPDDR (CA point-to-point, CA Trunks), LVCMOS escape
11	GND	REF
12	BOTTOM - SIG/PWR	GND, decaps, LVCMOS escape
	Solder mask	

Table 3-7 provides simulation results performed on sample designs, showing the impact of the PCB stackup (material, drill plan, and so forth) on LPDDR4 performance. The results showed that maximum bandwidth could be achieved on a FR4 solution, but required back-drilling. The higher frequency material could achieve same performance without back drill. Note the 8 layer design only achieved 3733, but this was due to other design compromises due to limited layers (solid reference planes, and so forth).

Table 3-7. Example LPDDR4 Performance Impact From J7 EVM Stackup

Design	Material	Layer Count	Via Back Drilling	Maximum LPDDR4 Speed (Mbps) (1)
J7 EVM	I-Speed	16	Yes	4266
Ref Board	I-Speed	10	No	4266
Ref Board	370HR	10	Yes	4266
Ref Board	370HR	8	No	3733

(1) These results are for J7 designs. For maximum supported data rates, see the device-specific data sheet.

3.6.2 Routing

The below examples from a J7 design show the LPDDR4 Clock and CA routing on an example 10-layer PCB design. The clock is routed differentially with target impedance of 70 Ω. For the T-branch to match the impedance of the trace, the impedance needs to be doubled. This can create challenges, as the higher impedances can be difficult to achieve in some PCB stackups. The CA signals are routed targeting 35 Ω, with the T-branch at two times the source impedance.

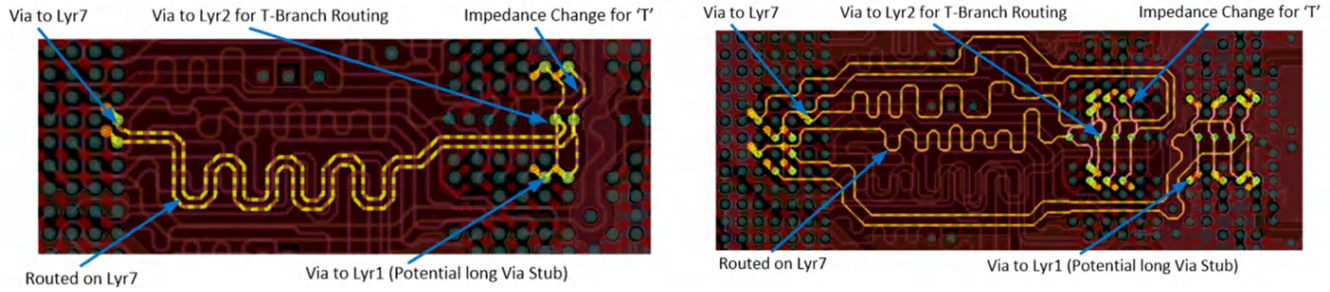

Figure 3-7. Example LPDDR4 Clock and CA Routing

On the same 10 layer reference design, the data groups are routed on layers 2 and 4. The upper layers are used due to the minimum via travel, which minimized the via inductance and via-to-via coupling. Because the data signals are point-to-point, T-branch routing is not required.

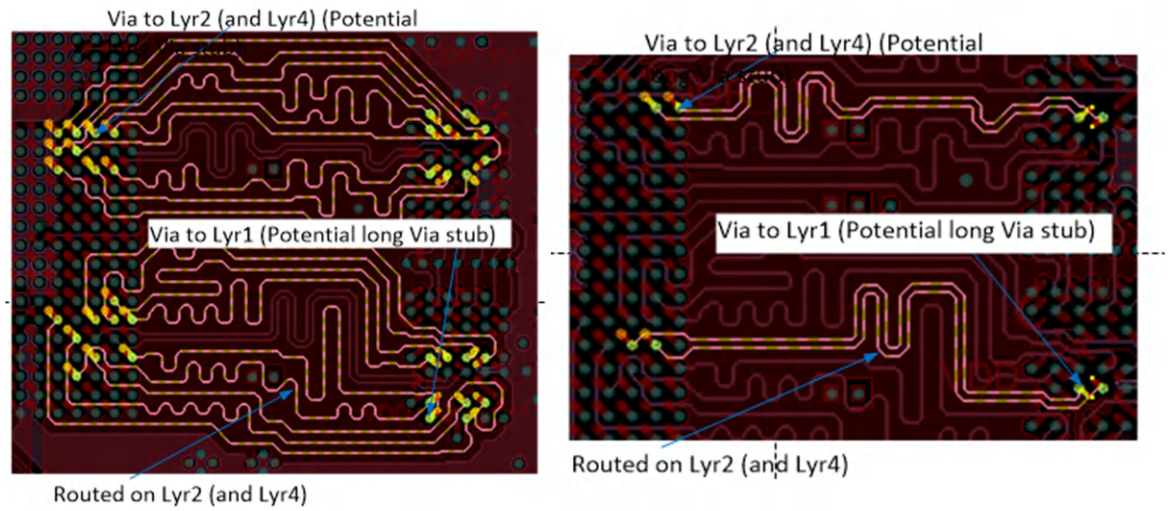

Figure 3-8. Example LPDDR4 Data Byte(s) and DQS(s) Routing

Table 3-8. LPDDR4 Performance Impact on Routing Layer (Read at pad)

Routing Layer	Via Type	Back Drilling	EW Margin (ps)	EH Margin (mV)
L1, L12	PTH	No	-7.10	56.72
L1, L12	PTH	Yes	-4.86	55.71
L1, L3	PTH	No	5.70	40.29
L1, L3	PTH	Yes	8.37	34.54

Table 3-9. LPDDR4 Performance Impact on Routing Layer (Write at pad)

Routing Layer	Via Type	Back Drilling	EW Margin (ps)	EH Margin (mV)
L1, L12	PTH	No	17.42	39.22
L1, L12	PTH	Yes	20.04	41.93
L1, L3	PTH	No	27.66	41.37
L1, L3	PTH	Yes	27.76	48.63

3.6.3 Model Verification

Before simulating, it is recommended to verify the models. One verification method described is the impedance plot (or impedance scan). The Impedance scans for a 10 layer design are provided.

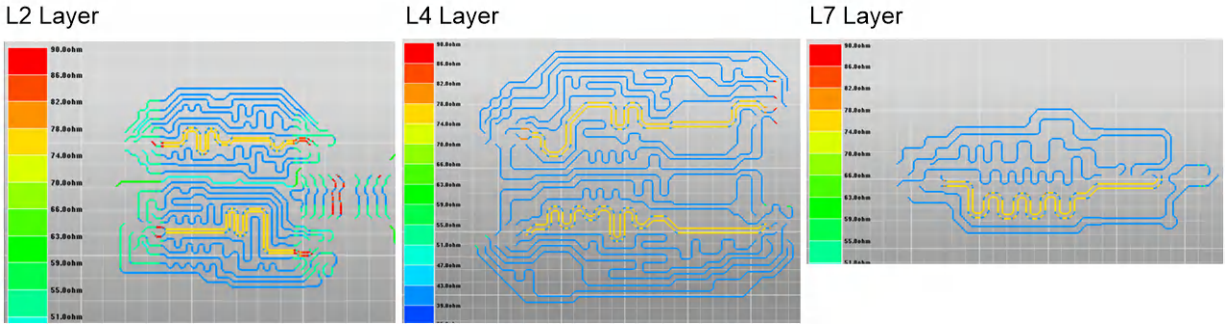

Figure 3-9. Example LPDDR4 Trace Impedance Scan

Table 3-10. Example LPDDR4 Trace Impedance Summary for Data

Layer	DDR Bus	DQ SE Impedance (Ω)	DQS/CLK Difference Impedance (Ω)
L2	B1 and B3	40.9	77.7
L2	CA	51.7	101.4
L4	B0 and B2	41.1	77.7
L7	CA	41.1	77.7

For CK and CA signals, the goal is to have the branch segment equal to two times the impedance of the feed trace. Note its common for the PCB to limit the achievable impedances. Simulations will show you if the compromises are acceptable.

Table 3-11. Example LPDDR4 Trace Impedance Summary for CA

Board	CA Feed Impedance (Ω)	CA Branch Impedance (Ω)	CA Branch Target (Ω)	Impedance Mismatch (Ω)
Initial Design	49.1	59.6	98 (49x2)	19.3
Final Design	41.1	51.7	82 (41x2)	15.3

The simulation results show the improvement made by closer matching the impedances to their targets.

Table 3-12. Example LPDDR4 Simulation Results From Improved Trace Impedance

Board	Total Eye Width Margin (ps)	Total Eye Height Margin (ps)
Initial Design	58.00	14.00
Final Design	124.68	48.08

3.6.4 Simulation Results

The simulation results are provided for the LPDDR4 interface from a 10 layer design. These simulation targets must be met to ensure the design will operate at the desired level of performance.

CA simulations need to be verified at the DRAM pin/BGA. This includes:

- Vix_CK ratio (JEDEC)
- Jitter/noise margins with respect to the eye mask (JEDEC)
- Peak-peak power noise

At DRAM Pin: Jitter/Noise Eye Margins Vix_CA Ratio

Package	Board	Total EW Margin (ps)	Total EH Margin (mV)	Min Rback Margin H (mV)	Min Rback Margin L (mV)	Vix_CK_Ratio (%)
J7 SCK 1207	J7 370HR 10L Ref 121819 ACC, No BD, SIwave	182.04	68.50	89.43	25.50	16.81

Ring-back High/Low Margins

Figure 3-10. LPDDR4 Simulation Results for CA

Data write simulations need to be verified at both the DRAM BGA pin and the DRAM pad. This includes:

- Vix_CK ration (JEDEC)
- Jitter/noise margins with respect to the eye mask (JEDEC)
- Peak-peak power noise

At DRAM Pin: Jitter/Noise Eye Margins Vix_DQS Ratio

Pkg Byte	Board	Total EW Margin (ps)	Total EH Margin (mV)	Min Rback margin H (mV)	Min Rback Margin L (mV)	Vix_DQS_Ratio (%)
B0	J7 370HR 10L Ref 121819 B0, With BD	62.32	55.20	68.63	111.83	9.80
B1	J7 370HR 10L Ref 121819 B1, With BD	54.52	94.28	86.46	114.69	7.64
B2	J7 370HR 10L Ref 121819 B2, With BD	53.40	73.96	81.19	106.32	5.55
B3	J7 370HR 10L Ref 121819 B3, With BD	54.86	52.74	34.97	48.55	9.81

Ring-back High/Low Margins

Figure 3-11. LPDDR4 Simulation Results for Write

Data read simulations need to be verified at SOC. This includes:

- Jitter/noise margins with respect to the eye mask
- Peak-peak power noise

Jitter/Noise Eye Margins Power Noise

Pkg Byte	Board	Total EW Margin (ps)	Total EH Margin (mV)	Min Rback Margin H (mV)	Min Rback Margin L (mV)	P-P VDDQ Noise (mV)
B0	J7 370HR 10L Ref 121819 B0, No BD	17.06	24.00	25.86	26.30	21.33
B1	J7 370HR 10L Ref 121819 B1, No BD	6.72	8.00	28.49	24.44	33.33
B2	J7 370HR 10L Ref 121819 B2, No BD	0.98	FAIL	19.40	17.18	28.97
B3	J7 370HR 10L Ref 121819 B3, No BD	FAIL	FAIL	11.05	20.26	15.87
B0	J7 370HR 10L Ref 121819 B0, With BD	19.02	26.00	27.84	30.10	26.12
B1	J7 370HR 10L Ref 121819 B1, With BD	6.24	8.00	30.79	27.25	39.98
B2	J7 370HR 10L Ref 121819 B2, With BD	5.24	6.00	27.95	28.83	40.24
B3	J7 370HR 10L Ref 121819 B3, With BD	4.60	6.00	35.41	34.52	25.21

Ring-back High/Low Margins

Figure 3-12. LPDDR4 Simulation Results for Read

The simulations results for read includes two sets for data, black and green. The black shows the design failed, as several bytes failed to meet the eye margins. The green is the simulation results of the same design, but with back-drilling the via stubs applied.

4 Appendix: SOC Package Delays

The SOC package delays provided in this appendix are measured from SOC die pad to SOC package pin. The skew limits specified in Table 2-6and Table 2-7 are measured from SOC die pad to DRAM package pin (including these delays inside the SOC package). The designer shall sum these package delays with the PCB delays for each net when checking for initial complance with the skew limits. Simulations of the propagation delays are then required to confirm the delays satisfy the requirements.

PROCESSOR PIN NAME	AM62Ax AMB PACKAGE DELAY (ps)	AM62Px AMH PACKAGE DELAY (ps)	NET CLASS	DESCRIPTION
DDR0_A0	22.88	21.5	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_A1	28.25	22.0	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_A2	22.05	20.7	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_A3	18.51	21.5	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_A4	32.23	21.3	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_A5	20.59	26.5	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_A6	24.25	20.9	ADDR_CTRL	Used with DDR4
DDR0_A7	33.50	28.4	ADDR_CTRL	Used with DDR4
DDR0_A8	16.81	25.8	ADDR_CTRL	Used with DDR4
DDR0_A9	25.80	26.7	ADDR_CTRL	Used with DDR4
DDR0_A10	27.13	26.4	ADDR_CTRL	Used with DDR4
DDR0_A11	17.62	16.9	ADDR_CTRL	Used with DDR4
DDR0_A12	23.81	21.2	ADDR_CTRL	Used with DDR4
DDR0_A13	27.85	24.0	ADDR_CTRL	Used with DDR4
DDR0_ACT_N	13.90	11.4	ADDR_CTRL	Used with DDR4
DDR0_ALERT_N	12.55	20.4	N/A	Used with DDR4
DDR0_BA0	14.08	9.2	ADDR_CTRL	Used with DDR4
DDR0_BA1	29.69	21.4	ADDR_CTRL	Used with DDR4
DDR0_BG0	20.88	24.9	ADDR_CTRL	Used with DDR4
DDR0_BG1	17.32	12.1	ADDR_CTRL	Used with DDR4
DDR0_CAS_N	16.50	17.6	ADDR_CTRL	Used with LPDDR4 and DDR4 (LPDDR4: copy of CS1 for LPDDR4_CS1_B)
DDR0_CK0	33.36	26.6	CK0	Used with LPDDR4 and DDR4
DDR0_CK0_N	31.54	25.1	CK0	Used with LPDDR4 and DDR4
DDR0_CKE0	23.42	24.0	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_CKE1	19.39	19.7	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_CS0_N	18.68	16.6	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_CS1_N	19.25	22.1	ADDR_CTRL	Used with LPDDR4 and DDR4
DDR0_DM0	42.32	33.9	BYTE0	Used with LPDDR4 and DDR4
DDR0_DM1	32.47	23.8	BYTE1	Used with LPDDR4 and DDR4
DDR0_DM2	37.15	25.6	BYTE2	Used with LPDDR4 and DDR4
DDR0_DM3	34.93	39.9	BYTE3	Used with LPDDR4 and DDR4
DDR0_DQ0	40.49	40.1	BYTE0	Used with LPDDR4 and DDR4
DDR0_DQ1	40.10	37.4	BYTE0	Used with LPDDR4 and DDR4
DDR0_DQ2	37.54	37.2	BYTE0	Used with LPDDR4 and DDR4
DDR0_DQ3	38.09	37.5	BYTE0	Used with LPDDR4 and DDR4
DDR0_DQ4	37.74	43.1	BYTE0	Used with LPDDR4 and DDR4
DDR0_DQ5	39.28	37.1	BYTE0	Used with LPDDR4 and DDR4
DDR0_DQ6	45.09	35.3	BYTE0	Used with LPDDR4 and DDR4
DDR0_DQ7	46.22	32.9	BYTE0	Used with LPDDR4 and DDR4

PROCESSOR PIN NAME	AM62Ax AMB PACKAGE DELAY (ps)	AM62Px AMH PACKAGE DELAY (ps)	NET CLASS	DESCRIPTION
DDR0_DQ8	36.45	29.1	BYTE1	Used with LPDDR4 and DDR4
DDR0_DQ9	27.44	31.6	BYTE1	Used with LPDDR4 and DDR4
DDR0_DQ10	37.16	22.2	BYTE1	Used with LPDDR4 and DDR4
DDR0_DQ11	35.57	29.9	BYTE1	Used with LPDDR4 and DDR4
DDR0_DQ12	34.30	25.2	BYTE1	Used with LPDDR4 and DDR4
DDR0_DQ13	29.40	22.4	BYTE1	Used with LPDDR4 and DDR4
DDR0_DQ14	40.85	24.8	BYTE1	Used with LPDDR4 and DDR4
DDR0_DQ15	42.33	32.6	BYTE1	Used with LPDDR4 and DDR4
DDR0_DQ16	44.73	25.8	BYTE2	Used with LPDDR4 and DDR4
DDR0_DQ17	37.56	22	BYTE2	Used with LPDDR4 and DDR4
DDR0_DQ18	36.87	22.1	BYTE2	Used with LPDDR4 and DDR4
DDR0_DQ19	28.07	22.2	BYTE2	Used with LPDDR4 and DDR4
DDR0_DQ20	35.14	32.8	BYTE2	Used with LPDDR4 and DDR4
DDR0_DQ21	26.37	30.2	BYTE2	Used with LPDDR4 and DDR4
DDR0_DQ22	29.40	25.3	BYTE2	Used with LPDDR4 and DDR4
DDR0_DQ23	29.78	28.4	BYTE2	Used with LPDDR4 and DDR4
DDR0_DQ24	42.45	37.2	BYTE3	Used with LPDDR4 and DDR4
DDR0_DQ25	37.11	30.6	BYTE3	Used with LPDDR4 and DDR4
DDR0_DQ26	34.38	33.3	BYTE3	Used with LPDDR4 and DDR4
DDR0_DQ27	34.47	38.7	BYTE3	Used with LPDDR4 and DDR4
DDR0_DQ28	35.37	34.7	BYTE3	Used with LPDDR4 and DDR4
DDR0_DQ29	41.43	31.5	BYTE3	Used with LPDDR4 and DDR4
DDR0_DQ30	37.85	36.2	BYTE3	Used with LPDDR4 and DDR4
DDR0_DQ31	41.82	37.1	BYTE3	Used with LPDDR4 and DDR4
DDR0_DQS0	45.57	40.1	DQS0	Used with LPDDR4 and DDR4
DDR0_DQS0_N	47.21	41.8	DQS0	Used with LPDDR4 and DDR4
DDR0_DQS1	35.22	28.1	DQS1	Used with LPDDR4 and DDR4
DDR0_DQS1_N	37.13	29.5	DQS1	Used with LPDDR4 and DDR4
DDR0_DQS2	32.77	30.2	DQS2	Used with LPDDR4 and DDR4
DDR0_DQS2_N	34.04	31.8	DQS2	Used with LPDDR4 and DDR4
DDR0_DQS3	45.45	37.1	DQS3	Used with LPDDR4 and DDR4
DDR0_DQS3_N	43.87	35.6	DQS3	Used with LPDDR4 and DDR4
DDR0_ODT0	19.87	13	ADDR_CTRL	Used with DDR4
DDR0_ODT1	24.27	21.1	ADDR_CTRL	Used with DDR4
DDR0_PAR	29.55	28.1	ADDR_CTRL	Used with DDR4
DDR0_RAS_N	14.99	10.3	ADDR_CTRL	Used with LPDDR4 and DDR4 (LPDDR4: copy of CS0 for LPDDR4_CS0_B)
DDR0_RESET0_N	14.20	31.9	ADDR_CTRL	Used with LPDDR4 and DDR4, No length matching requirement
DDR0_WE_N	11.68	20.5	ADDR_CTRL	Used with DDR4

5 References

- *AM62A Low-Power SK EVM User's Guide* (SPRUJ66)
- *AM62P SK EVM User's Guide* (SPRUJA2)

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2023 to December 13, 2023 (from Revision (February 2023) to Revision A (December 2023)) Page

- Added AM62Px device throughout the document 1
- Updated the numbering format for tables, figures and cross-references throughout the document 3
- Updates were made in Section 1.4.1, ... 5
- Reordered rows and added 2 Channel, 2 Die, 2 Rank row in Table 2-1 7
- Added 10k pull-down to RESET_n in each figure, RESET_n has no length matching requirement, removed ODT_CA_B and fixed missing connection to DQ[7:0] in Figure 2-3 7
- Update was made in Section 2.12 15
- Relaxed skew limits, skew considers SOC package delays (see appendix) and PCB delays, simulation must be performed to check delays and skew, clarified and reordered notes in Table 2-6 16
- Relaxed skew limits, skew considers SOC package delays (see appendix) and PCB delays, simulation must be performed to check delays and skew, clarified and reordered notes in Table 2-7 18
- Updates were made in Section 3.3 21
- Updates were made in Section 3.5 21
- Removed Waveform Quality section (ring-back margins) 24
- Update was made in Section 3.5.3.1 24
- LPDDR4-3733 Read eye mask VdIVW corrected to 140mV in Table 3-3 25
- Added AM62Px SK EVM stackup into Table 3-6 27
- Corrected Impedance Mismatch calculation in Table 3-11 30
- Removed Minimum ring-back margins at high/low levels (JEDEC) 30
- Added Section 4 32

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