Application Note

Hardware Design Guide for AM6442, AM6422, AM6412 and AM2434 Processors

ABSTRACT

This hardware design guide gives an overview of the design considerations to be followed by the board designers using AM6442, AM6441, AM6422, AM6421, AM6412, AM6411, AM2434, AM2432 and AM2431 processors. This application note is intended to be used at different stages of board design as a guide by the designers. The hardware design guide additionally references to collaterals (device-specific and common) that could help the designers to optimize the efforts during the board design.

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1 Introduction

The Hardware Design Guide for AM6442, AM6441, AM6422, AM6421, AM6412, AM6411, AM2434, AM2432 and AM2431 processors provides a starting point for the engineers designing with any of these processors. This hardware design guide provides an overview of the design flow, design efforts and highlights important design aspects that must be addressed. Note that this document does not contain all of the information needed to complete the board design. In many cases, it refers to the device-specific collaterals and various other user's guides as sources for specific information.

The hardware design guide (document) is organized in a sequential manner. It starts from decisions that must be made during the initial planning stages of the design, through the selection of key devices, electrical, and thermal requirements. For ensuring a successful design, issues discussed in each of the section should be resolved before moving to the next section.

Note

This hardware design guide may not cover every aspect of the board design.

Note

These processors have capabilities to help board designers address safety requirements.

This hardware design guide is focused on non-safety applications.

1.1 Before Getting Started With the Board Design

These family of processors includes wide variety of peripherals and processing capabilities, not all of which will be used in every design. Consequently, the requirements for different designs using the same device can vary widely depending on the target application. Designers must understand the requirements before determining the details of the design. In addition, the design may require additional circuitry to operate correctly in the target environment. Refer latest collaterals on TI.com like the device-specific Data Sheet, Errata, TRM and EVM User's guide for selecting the device and to determine the following:

- What are the expected environmental conditions for the device operation, target boot mode, storage type and interfaces used
- Processing (Performance) requirements for each of the cores in the selected device
- What is the DDR memory type, speed, size and interface that will be used
- Processor peripherals used for the attached devices

1.2 Processor (Device) Selection

Selection of processor is the most important step during the board design process. For understanding and selecting the device variant, features, and speed grade that is applicable, see the *Functional Block Diagram* and *Device Comparison* sections in the device-specific data sheet.

1.2.1 Availability of Tightly Coupled Memory (TCM)

Refer device-specific data sheet for the R5F Tightly Coupled Memory (TCM) size information. Irrespective of the number of cores available, the TCM remains in the subsystem that can be used by the processor.

For AM642x, one core from each subsystem (cluster) is available resulting in 256K.

Note that lockstep is not supported on AM64x processors. Refer device-specific TRM.

1.3 Technical Documentation

A number of documents relevant to the selected device are provided on the product folder page on TI.com. Read through relevant documents before the start of design.

The below link summarizes the collaterals that can be referred when starting a custom design.

[FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design – Collaterals to Get started.

1.4 Design Documentation

Throughout this document, TI recommends generating a design document periodically. Generating and storing this information provides you with the foundation for the documentation package, and this design document is needed when seeking external review support.

2 Block Diagram

A detailed block diagram, covering all the functional blocks and required interfaces is key to a successful design.

2.1 Creating the Block Diagram

The first step during the board design is to create a detailed block diagram. The block diagram should include all major functional blocks, associated devices for processor (Ex: PMIC) and attached devices, interfaces and illustrate the IOs used for interconnecting the processor and attached devices.

The following is a collection of resources to support the block diagram creation process:

- The SK-AM64B (AM64B starter kit for AM64x Sitara processors), TMDS64EVM (AM64x evaluation module for Sitara processors), TMDS243EVM (AM243x evaluation module for Arm Cortex-R5F-based MCUs) and any other available EVMs are a good source to start with the design.
- The TI.com links referred to below provide device-specific Functional Block Diagrams, Data Sheet, User's Guide, Errata, Application Notes, design considerations, and other related information for various applications. The design and development section includes EVM information, design tools, simulation models and software. As part of support and training, links to commonly applicable E2E threads and FAQs are available.
  - AM6442 Product Folder
  - AM6441 Product Folder
  - AM6422 Product Folder
  - AM6421 Product Folder
  - AM6412 Product Folder
  - AM6411 Product Folder
  - AM2434 Product Folder
  - AM2432 Product Folder
  - AM2431 Product Folder

2.2 Selecting the Boot Mode

The block diagram should indicate the configuration used for processor booting. This includes the primary boot and the backup boot.

These processors contain multiple peripheral interfaces that support boot mode. Examples include: eMMC, MMC/SD, QSPI, OSPI, GPMC (NOR/NAND), Ethernet, USB (Device & Host), PCIe, xSPI and I2C. These processors supports a primary boot mode option and an optional backup boot mode option. If the primary boot source fails to boot, the ROM moves on to the backup mode.

The boot mode pins and the associated resistor configurations provide inputs on the boot mode to be used by the ROM code during boot. These pins are sampled at power-on-reset (PORz_OUT), and must be properly set up before releasing (deassertion) the reset.

Boot mode configurations can be categorized as below:

PLL Config: BOOTMODE [02:00] – Denote system clock frequency (MCU_OSC0_XI/XO) to ROM code for PLL configuration

Primary Boot Mode: BOOTMODE [06:03] – Select the configured boot (primary) mode after POR, that is, the peripheral/memory to boot from

Primary Boot Mode Config: BOOTMODE [09:07] – These pins provide optional configurations for primary boot and are used in conjunction with the boot mode selected

Backup Boot Mode: BOOTMODE [12:10] – Select the backup boot mode, that is, the peripheral/memory to boot from, if primary boot fails

Backup Boot Mode Config: BOOTMODE [13] – This pin provides optional configurations for the backup boot devices

Reserved: BOOTMODE [15:14] – Reserved pins

Key considerations for boot mode configuration:

- TI recommends including provision to configure boot modes used during development, such as UART boot or No-boot mode for JTAG debug.
- Boot pins have other functions after reset. Ensure the board design takes this into account when choosing pullup or pulldown resistors for the boot pins. If these pins are driven by another device, they must return to the proper boot configuration levels whenever the device is reset (indicated by the PORz_OUT pin) to enable it to boot properly.
- The functionality of some boot mode pins are reserved. These pins should not be left floating and must be terminated (pullup or pulldown). For details regarding termination of reserved boot mode pins, see the *Boot Mode Pins* section of the *Initialization* chapter of the device-specific TRM.

For details regarding boot modes, see the *Initialization* chapter of the device-specific TRM.

Note

It is the designer's responsibility to set the boot mode configuration (via pullups or pulldowns, and optionally jumpers/switches) depending on the desired boot scenario.

Note

Refer *AM64x / AM243x Processor Silicon Errata* for updates related to Boot.

2.3 Confirming Pinmux (Multiplexing Compatibility)

The processor includes a number of peripheral interfaces. To optimize size, pin count, package cost while maintaining maximum functionality, many of the processor pads (pins) can multiplex up to eight signal functions. Thus, not all peripheral interface instances can be used simultaneously.

TI has developed SysConfig-PinMux Tool that helps board designer select the appropriate function using pin-multiplexing configuration too for their AM64x / AM243x based board design.

Note

It is recommended to save the pinmux configuration generated using SysConfig-PinMux Tool along with other design documentation.

3 Power Supply

After completing the processor selection and block diagram, next step in the design process is to determine the power supply architecture for the selected processor.

3.1 Power Supply Architecture

The power supply architecture that can be considered are listed below:

3.1.1 Integrated Power Architecture

The power architecture could be based on Multi-channel ICs (PMIC), refer *Powering the AM64xx with the LP8733xx PMIC*, *Using LP8733xx and TPS65218xx PMICs to Power AM64x and AM243x Sitara Processors*, *Powering the AM64x with the TPS65220 or TPS65219 PMIC* and *Powering the AM243x With the TPS65219 PMIC* application notes.

3.1.2 Discrete Power Architecture

The power architecture could be based on DC-DC converters and LDOs, refer *TMDS64EVM (AM64x evaluation module for Sitara processors)* EVM schematic.

3.2 Power (Supply) Rails

For the complete list of processor power supply rails and recommended operating range, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet. The following sections provide additional details about select power rails.

3.2.1 Core Supply

In AM64x family of processors, core supply VDD_CORE can be operated at 0.75 V or 0.85 V. When VDD_CORE is operating at 0.75 V, VDD_CORE shall be ramped up prior to all 0.85 V supplies. VDD_CORE and VDDR_CORE are expected to be powered by the same source so these ramp together when VDD_CORE is operating at 0.85 V.

In AM243x family of processors, core supply VDD_CORE can be operated only at 0.85 V. VDD_CORE and VDDR_CORE are expected to be powered by the same source such that these ramp together.

Core supplies VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C, VDDA_0P85_USB0 and VDDR_CORE are specified to operate only at 0.85 V.

Core supplies VDD_MMC0 and VDD_DLL_MMC0 are specified to operate at 0.85 V. VDD_MMC0 and VDD_DLL_MMC0 shall be connected to the same power source as VDD_CORE when MMC0 is not used.

For more information, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

Note

AM64x supports 2 core voltages 0.75 V or 0.85 V. The Operating Performance Point (OPP) is not tied to the core voltage. There is no change in performance with 0.75 V or 0.85 V core voltage. The 0.75 V supply provides an option to optimize power and the 0.85 V supply optimizes the number of power rails without change in performance.

3.2.2 Peripheral Power Supply

The processor includes dedicated peripheral supply pins for USB0, MMC0, PLLs, ADC0 and SERDES0. The recommended operating voltage is 1.8 V nominal. An additional 3.3 V analog supply is required for USB.

Depending on the selected memory DDR PHY IO (VDDS_DDR) and DDR clock IO (VDDS_DDR_C) supply can be 1.1 V or 1.2 V.

For more information, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

3.2.3 Internal LDO for IO Groups (Processor IO Groups)

The processor includes eight internal LDOs, with the output of each connected to a pin (CAP_VDDSx [x = 0..5], CAP_VDDSHV_MMC1 and CAP_VDDS_MCU). A capacitor must be connected close to each of these LDO output pins. For guidance on the capacitor value and connection, see the *Power Supply* section in the *Signal Descriptions* chapter of the device-specific data sheet.

3.2.4 Dual-Voltage IOs (LVCMOS IOs / Processor IOs)

The processor includes seven dual-voltage IO domains (VDDSHVx [x = 0..5] and VDDSHV_MCU), where each domain provides power to a fixed set of IOs. Each IO domain can be configured for 3.3 V or 1.8 V, which determines a common operating voltage for the entire set of IOs powered by the respective IO domain. All signals connected to these domains must operate from the same power source that is being used to power the respective VDDSHVx supply rail. Most of the IO buffers are not fail-safe (refer device-specific data sheet for fail-safe IOs). The supply voltage for the VDDSHVx rails must be present before any voltage is applied to the associated IOs.

IO grouping information is summarized below:

VDDSHV0 – Voltage for the General IO group

VDDSHV1 – Voltage for the PRG0 IO group

VDDSHV2 – Voltage for the PRG1 IO group

VDDSHV3 – Voltage for the GPMC IO group

VDDSHV4 – Voltage for the Flash IO group

VDDSHV5 – Voltage for the MMC1 IO group

VDDSHV_MCU – Voltage for the MCU General IO group

3.2.5 Dual-Voltage Dynamic Switching IOs for SDIO

The processor includes one integrated SDIO LDO to support SD card IO voltage switching. An output capacitor must be connected close to the LDO output pin.

Only one MMCSD port (selectable through V1P8_SIGNAL_ENA bit) can be connected to the SDIO LDO in a given system.

VDDSHV5 was designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails.

For more details, refer the *Integrated Low-dropout Regulator (LDO)* section in the *Power* chapter of the device-specific TRM.

3.2.6 VPP (eFuse ROM Programming Supply)

This supply (1.8 V) is only sourced while programming the eFuse. VPP pin can be left floating (HiZ) or terminated to ground during power-up/power-down sequences and during normal processor operation. The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be ramped up after completion of proper processor power-up sequence.
- The VPP supply has high current transients and local bulk capacitors are likely needed near the VPP pin to assist the LDO transient response.
- Select the power supply with quick discharge capability or use a discharge resistor. A Maximum current of 400 mA is required for programming. It is recommended to use a fixed LDO with input supply (3.3 V) and enable input.
- If an external power supply is used, the supply is applied after the processor power supplies are stable.
- The VPP power supply must be disabled (left floating (HiZ) or grounded) when not programming the OTP registers.

For more information, see [FAQ] AM625 / AM623 Custom board hardware design – Queries regarding VPP eFuse programming power supply selection and application.

For more information, see the *VPP Specifications for One-Time Programmable (OTP) eFuses* section in the *Specifications* chapter of the device-specific data sheet.

3.3 Determining Board Power Requirements

The maximum and minimum current requirements for each of these supply voltage rails are not available in the device-specific data sheet. These requirements are highly application-dependent and must be estimated using TI provided tools for a specific use case.

3.4 Power Supply Filters

The processor contains multiple analog supply pins that provide power to sensitive analog circuitry such as VDDA_MCU, VDDA_PLLx [x=0-2], VDDA_1P8_SERDES0, VDDA_1P8_USB0 and VDDA_ADC0. These must be attached to filtered supply sources.

3.5 Power Supply Decoupling and Bulk Capacitors

To properly decouple the processor and attached device supplies from board noise, bulk and decoupling capacitors are recommended. Refer the *TMDS64EVM (AM64x evaluation module for Sitara processors)*, *TMDS243EVM (AM243x evaluation module for Arm Cortex-R5F-based MCUs)* and other EVM schematics for the required bulk and decoupling capacitors.

For guidance on optimizing and placement of the decoupling and bulk capacitors, refer the *Sitara Processor Power Distribution Networks: Implementation and Analysis*.

3.5.1 Note on PDN Target Impedance

Note that target impedance values are not provided for all supply rails since the target impedance calculation includes reference to the maximum current on the rail and is dependent on use case.

For updates on the target impedance, see the [FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design – Collaterals to Get started or E2E.

3.6 Power Supply Sequencing

A detailed diagram for the power supply sequencing (Power-Up/Power-Down) are available in the device-specific data sheet. All power supplies associated with the processor should allow for controlled slew rate and supply sequencing using a PMIC-based power supply or using on-board logic when discrete power solution is used.

3.7 Supply Diagnostics

The processor includes below voltage monitor pins:

- VMON_VSYS (Early indication): Connect the system voltage (main supply voltage - 3.3 V, 5 V or any other voltage) through a resistor voltage divider. Consider implementing a capacitor for noise filtering as described in the device-specific data sheet.
- VMON_1P8_SOC, VMON_1P8_MCU and VMON_3P3_SOC, VMON_3P3_MCU (Monitoring): These pins can be connected directly to their respective 1.8 V and 3.3 V supplies. An internal resistor divider with software control is implemented inside the processor for each of these pins.

For more information see the *System Power Supply Monitor Design Guidelines* section in the *Applications, Implementation, and Layout* chapter of the device-specific data sheet

3.8 Power Supply Monitoring

For improved board performance, consider provisioning for external monitoring of supply rails and load currents.

For more information, see the *TMDS64EVM (AM64x evaluation module for Sitara processors)* and *TMDS243EVM (AM243x evaluation module for Arm Cortex-R5F-based MCUs)* schematics.

Now that the power supply architecture and the devices required for generating the supply rails have been finalized, create a block diagram that includes the power supply rails and interconnection. It is also recommended to create a power supply sequence (Power-Up/Power-Down) diagram.

4 Clocking

The next step of the design is proper processor clocking, and providing appropriate clocks to all attached devices. The processor clock can be generated internally by pairing external crystal with an internal oscillator or externally by a clock generator or oscillator (LVCMOS compatible). This section describes the clocks available in the processor and the requirements for these clocks.

4.1 System Clock Input

The recommended processor input clocks and oscillator connections are summarized in the *Clock Specifications* section in the *Specifications* chapter of the device-specific data sheet.

MCU_OSC0 clock is required for proper operation of the processor.

4.2 Unused Clock Input

Not Applicable.

4.3 Clock Output

IO pin CLKOUT0 can be configured as clock output. The clock output can be used as clock source for the attached devices (Ex: Ethernet PHY).

For more details, refer the device-specific data sheet and TRM.

4.4 Single-ended Clock Source

The MCU_OSC0_XI can be sourced from a 1.8 V LVCMOS square-wave digital clock source. For more details, see the *Input Clocks / Oscillators* section in the *Specifications* chapter of the device-specific data sheet.

Note

Be sure to terminate the XO pin as per the device-specific data sheet recommendation when using an external clock input.

4.5 Crystal Selection

When selecting a crystal, the board designer must consider the temperature and aging characteristics based on the worst case environment and expected life expectancy of the system.

Verify the crystal selection with the crystal manufacturer as required.

For more information, see the [FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design – Queries regarding Crystal selection.

For more information, see the *MCU_OSC0 Crystal Circuit Requirements* table of the device-specific data sheet.

5 JTAG (Joint Test Action Group)

TI supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. Although JTAG is not required for operation, TI strongly recommends that a JTAG connection be included in the designs.

5.1 JTAG / Emulation

Relevant documentation for the JTAG/Emulation:

- *Emulation and Trace Headers Technical Reference Manual*
- *XDS Target Connection Guide*
- *Boundary Scan Test Specification (IEEE-1149.1)*
- *AC Coupled Net Test Specification (IEEE-1149.6)*

5.1.1 Configuration of JTAG / Emulation

The IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) interface can be used for boundary scan and emulation. The boundary scan implementation is compliant with both IEEE-1149.1 and 1149.6. Boundary scan can be used regardless of the device configuration.

As an emulation interface, the JTAG port can be used in various modes:

- Standard emulation: requires only five standard JTAG signals
- HS-RTDX emulation: requires five standard JTAG signals plus EMU0 and/or EMU1. EMU0 and/or EMU1 are bidirectional in this mode.
- Trace port: The trace port allows real-time dumping of certain internal data. The trace port uses the EMU pins to output the trace data.

Emulation can be used regardless of the device configuration.

For supported JTAG clocking rates, see the device-specific TRM.

The required BSDL model for boundary scan testing can be downloaded.

5.1.1.1 AM64x

- AM64x / AM243x BSDL Model

5.1.1.2 AM243x

- AM243x BSDL Model

5.1.2 Implementation of JTAG / Emulation

The JTAG and Emulation pins are in same power domains. The TDI, TDO, TCK, TMS, TRSTn, EMU0 and EMU1 IOs are powered by the VDDSHV_MCU domain. VDDSHV_MCU can be configured either 1.8 V or 3.3 V.

For other system-level implementation details, see the *Emulation and Trace Headers Technical Reference Manual*.

5.1.3 JTAG Termination

For terminating the JTAG interface signal, see the *Pin Connectivity Requirements* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

Note

It is recommended to provision for connecting the JTAG using test points for development testing and the required pulls as per the pin connectivity table in the device-specific data sheet when a JTAG connector is not used.

6 Configuration (Processor) and Initialization (Processor and Device)

When the voltage rails and the required clocks are present and stable, the processor reset (MCU_PORz) may be deasserted (released) after the recommended hold time (refer device-specific data sheet) to start the processor boot process.

6.1 Processor Reset

The processor can be reset in several ways. The methods are described in detail in the device-specific data sheet and TRM.

The processor includes three external reset input pins (MCU_PORz (MCU Domain cold reset), MCU_RESETz (MCU Domain warm reset) and RESET_REQz (Main Domain external warm reset request input)).

Be sure to provide the terminations to the reset inputs as recommended in the *Pin Connectivity Requirements* section of the device-specific data sheet.

The processor also includes three reset status output pins (MCU_RESETSTATz (MCU Domain warm reset status output), PORz_OUT (Main Domain POR status output) and RESETSTATz (Main Domain warm reset status output)).

Reset status outputs when not used does not need external pull (OK to connect a test point for board testing).

For MCU_PORz (fail-safe), 3.3 V input can be applied, but the input thresholds are still a function of the 1.8 V IO supply voltage (VDDS_OSC).

MCU_PORz reset input signal has input slew rate requirement specified in the device-specific data sheet.

Additional reset modes are available through internal registers and emulation.

6.2 Latching of the Boot Mode Configuration

For more details about the processor boot mode options, see above Section 2.2.

Boot modes and certain device configuration are latched at the rising edge of PORz_OUT. The device configuration and boot mode inputs are multiplexed with pins having GPIO or other functions. After the status (level) on these pins are latched into the configuration registers, these pins are available to be used for their primary function. The PORz_OUT pin indicates latching of boot mode configuration.

6.3 Attach Device Reset

TI recommends implementing the reset using ANDing logic for on-board Media and Data Storage devices, and other peripherals as applicable. One of the AND gate input is controlled by processor general-purpose input/output (GPIO) pin with provision for pullup resistor and 0-ohm to isolate. The other AND gate input is the main domain reset status output (PORz_OUT/RESETSTATz) signal. Ensure the reset inputs are terminated as per the device recommendations.

In case ANDing logic is not used and the processor reset status output is used directly to reset the attach devices, ensure the IO levels of the attach device match the processor IO level or use a level translator to match the levels.

A power switch controlled by a reset logic is recommended to reset the SD Card since power cycling the SD Card is the only way to reset the card to its default state. The power supply (3.3 V) to the SD Card needs to be connected through the controlled external power switch.

For more information on implementing reset ANDing logic and SD Card power switch reset logic, refer the *TMDS64EVM (AM64x evaluation module for Sitara processors)*, *TMDS243EVM (AM243x evaluation module for Arm Cortex-R5F-based MCUs)* and other EVM schematics.

6.4 Watchdog Timer

Consider using an internal or external watchdog timer based on the application requirement.

7 Peripherals

This section covers the processor peripherals and modules, and is intended to be used in addition to the information provided in the device-specific Data Sheet, TRM, and relevant Application Notes. The three types of documents could be used as follows:

- Data Sheet: Pin Description, Device operational modes, AC Timings, Guidance on pin functions, Pin mapping
- TRM: Functional Description, Programming Guide, Information regarding registers and configuration
- Application Notes: System-level understanding and resolving commonly observed issues

7.1 Selecting Peripherals Across Domains

The processor is partitioned into two domains, each containing specific processing cores and peripherals:

- MAIN Domain
- Microcontroller (MCU) Domain

For most use cases, peripherals from any of the domain can be used by any of the core. All peripherals, regardless of their domain, are memory mapped, and the Arm® Cortex®-A53 cores can see and access most of the peripherals in the MCU domain. Similarly MCU can access most of the peripherals in the main domain.

7.2 Memory

DDR Subsystem supports DDR4 and LPDDR4. Refer device-specific data sheet and TRM for data bus width (16-bit), inline ECC support, speed (up-to 1600 MT/s) and Max addressable range (2GBytes (DDR4 or LPDDR4)).

The allowed configurations are 1 X 16-bit or 2 X 8-bit. 1 X 8-bit configuration is not a valid configuration.

For more details, refer the *DDR Subsystem (DDRSS)* section in the *Memory Controllers* chapter of the device-specific TRM.

7.2.1 Processor DDR Subsystem and Device Register Configuration

The DDR controller and DDR PHY have a large number of parameters to configure. To facilitate the configuration, an online tool (SysConfig tool) is provided that generates an output file consumed by the driver. Choose DDR Subsystem Register Configuration from the Software Product pulldown menu and choose the required processor. This tool takes system information, timing parameters from DDR device data sheet, and IO parameters as inputs and then outputs a header file that the driver uses to program the DDR controller and DDR PHY. The driver then kicks off the full training sequence.

The SDK will have an integrated configuration file for the device mounted on the EVM. If you need a configuration file for a different device, you need to generate the new configuration file with the DDR Register Configuration tool.

For more information, see [FAQ] AM62A7 or AM62A3 Custom board hardware design – Processor DDR Subsystem and Device Register configuration.

7.3 Media and Data Storage Interfaces

Media and Data Storage interface supports 2 x Multi-Media Card/Secure Digital (MMC/SD/SDIO) ((8b+4b) (8-bit eMMC, 4-bit SD/SDIO)) interface, 1 x General-Purpose Memory Controller (GPMC) and 1 x OSPI/QSPI.

For information related to OSPI/QSPI, see the [FAQ] OSPI FAQ for Sitara/Jacinto devices.

For more details, refer the *Memory Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.4 Ethernet Interface

AM64x / AM243x processor supports up to five concurrent external Ethernet ports. Pinmuxing overlaps one of the CPSW3G and PRU1_ICSSG.

Before configuring the MDIO interface refer advisory *i2329 MDIO: MDIO interface corruption (CPSW and PRU-ICSS) (AM64x / AM243x Processor Silicon Revision 1.0, 2.0)*.

7.4.1 Common Platform Ethernet Switch 3-port Gigabit Ethernet (CPSW3G)

The CPSW3G interface can either be configured as a 3-port switch (interfaces to two external Ethernet ports (port 1 and 2)) or a dual independent MAC interface having their own MAC address.

CPSW3G supports RGMII (10/100/1000) or RMII (RGMII) (10/100).

For RMII interface implementation, see the *CPSW0 RMII Interface* section of the device-specific TRM.

CPSW3G allows using mixed RGMII/RMII interface topology.

RGMII_ID is not timed, tested, or characterized. RGMII_ID is enabled by default and the register bit is reserved.

For more details on the Ethernet interface, see the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.4.2 Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit (PRU_ICSSG)

AM64x / AM243x processor supports two instances of PRU_ICSSG subsystems and each PRU_ICSSG contains 2 x Ethernet ports (MII (10/100) or RGMII (10/100/1000)). Refer the TRM for information on support for SGMII mode. PRU_ICSSG supports industrial protocols and the supported protocols depends on device selection.

For selecting the processor with PRU_ICSSG functionality, refer the [FAQ] AM6442: What PRU_ICSSG functionality is on each AM64x device?

For more details, refer the *Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit (PRU_ICSSG)* section in the *Processors and Accelerators* chapter of the device-specific TRM.

7.5 Universal Serial Bus (USB) Subsystem

AM64x / AM243x processor supports 1 x USB 3.1 Dual-Role Device (DRD) Subsystem. These Ports are configurable as USB host (SuperSpeed Gen 1 (5 Gbps), High-speed (480 Mbps), Full-speed (12 Mbps), and Low-speed (1.5 Mbps)), USB device (High-speed (480 Mbps), and Full-speed (12 Mbps)), or USB Dual-Role device.

Follow *USB VBUS Design Guidelines* section of the device-specific data sheet for scaling the VBUS voltage.

VBUS voltage is required to be connected when the device is configured in device mode. VBUS connection is optional in host mode.

A power switch with OC (over current) indication connected to an processor GPIO is recommended when the USB interface is configured as host. The DRVVBUS drives the power switch.

For USB connections and On-The-Go feature support, see the device-specific TRM.

For more details, refer the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.6 Peripheral Component Interconnect Express (PCIe) Subsystem

AM64x / AM243x processor supports one PCI-Express Gen2 controller (PCIe) and supports Gen2 and Single Lane operation.

For more details, refer the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

Note

No PCIe completion is generated as long as POWER_STATE_CHANGE_ACK is '0'. Configure POWER_STATE_CHANGE_ACK to '1' for generating PCIe completion.

Note

- The Serdes PHY (interface) of AM64x / AM243x is common for USB SuperSpeed and PCIe interface. Therefore, USB shall be limited to non-SuperSpeed modes when using the SerDes PHY for PCIe.
- The use of USB3 and PCIe is mutually exclusive on this processor so these (USB3 and PCIe) cannot be used at the same time.

7.7 General Connectivity Peripherals

AM64x / AM243x processor supports multiple instances of Inter-Integrated Circuit (I2C), Universal Asynchronous Receive/Transmit (UART), 12-Bit Analog-to-Digital Converters (ADC), Multichannel Serial Peripheral Interfaces (MCSPI), Fast Serial Interface Receiver (FSI_RX) cores, Fast Serial Interface Transmitter (FSI_TX) cores, Enhanced Pulse-Width Modulator (EPWM), Enhanced Capture (ECAP), Enhanced Quadrature Encoder Pulse (EQEP), Modular Controller Area Network (MCAN) modules with or without full CAN-FD support and General-Purpose Input Output (GPIO) modules.

For I2C interface with open drain output type buffers (I2C0 and MCU_I2C0), an external pullup is recommended irrespective of peripheral usage and configuration. Refer *Pin Connectivity Requirements* section in device-specific data sheet. These interfaces have slew rate limit when pulled to 3.3 V.

An external pullup is recommended for the I2C interfaces with LVCMOS type buffers based on the configuration. For the available I2C instances, see the device-specific data sheet.

For more information, see the [FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design – I2C interface.

Additionally, PRU_ICSSG supports UART0, eCAP0, PWM, IEP0 and IEP1 peripheral modules.

The number of instances available depends on the device selection and can be configured using the SysConfig-PinMux Tool based on the application.

For more details, see the *Peripherals* chapter of the device-specific TRM.

7.8 Analog-to-Digital Converter (ADC)

AM64x / AM243x processor supports single 12-bit ADC which can be multiplexed to any 1 of the 8 analog inputs (channels) with programmable data rate up to 4 MSPS.

Refer *AM64x / AM243x Processor Silicon Errata* for guidance on using SR2.0 processors on existing boards and recommendations for new board designs.

For more details, refer the *General Connectivity Peripherals* section in the *Peripherals* chapter of the device-specific TRM.

7.8.1 Change Summary of AM64x / AM243x SR2.0 ADC Errata

One of the two pins assigned to the MMC0 PHY IO supply (VDDS_MMC0) in the SR1.0 processor is assigned as the ADC0_REFP pin in SR2.0. No compatibility issue is observed when installing a SR2.0 processor on a PCB that was designed for the SR1.0 pin assignment since the ADC0_REFP operates at the same voltage as VDDS_MMC0. However, the ADC can have performance issues if trying to use the device when a SR2.0 processor is installed on a PCB designed for SR1.0 processors since noise from the MMC0 PHY IO supply can couple directly into the ADC0_REFP pin.

SR1.0 processor cannot be installed on a PCB designed for SR2.0 processors since this PCB has a dedicated ADC0_REFP source which gets shorted to VDDS_MMC0 when a SR1.0 processor is installed.

One of the VSS pin is re-assigned to be ADC0_REFN. Currently ADC0_REFN is connected to VSS in the package. This change eliminates any direct coupling of package ground bounce into the ADC reference. This pin change does not have any impact on the PCB design since the SR1.0 VSS pin is already connected to the PCB VSS plane and we expect the new SR2.0 ADC0_REFN pin to also be connected to the PCB VSS power plane.

7.9 Termination of Power Pins, Unused Peripherals and IOs

All power pins must be supplied with the supply voltages specified in *Recommended Operating Conditions* section of the device-specific data sheet, unless otherwise specified.

AM64x / AM243x processor has pins (package balls) that have specific connectivity requirements and package balls that can be unused.

For information on terminating the unused peripherals (MMC0, SERDES0, USB0, DDRSS0 and ADC0 (entire ADC or any of the ADC inputs are not used)) and IOs, see the *Pin Connectivity Requirements* section of the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

7.9.1 External Interrupt (EXTINTn)

EXTINTn is a dedicated, fail-safe interrupt pin and is recommended to be terminated when connected externally or a PCB trace is connected.

8 Interfacing of IO Buffers and Simulations

An important step in the hardware design, before schematic capture, is to confirm electrical compatibility (DC and AC) between the processor and attached external devices.

- The device-specific (processor and attached devices) data sheet has important information with regards to timing and electrical characteristics.
- For high-speed interfaces, it is recommended to run IBIS simulations using IBIS models provided for the processor to confirm the functionality and signal integrity.

For more information on terminations, see the *General Termination Details* section in the *Hardware Design Guide for KeyStone II Devices*.

The required IBIS model can be downloaded from the below sections.

8.1 AM64x

- AM64x / AM243x BSDL Model

8.2 AM243x

- AM243x BSDL Model

9 Power Consumption and Thermal Analysis

The processor power consumption depends on application, features implemented, temperature, design topology, and temperature/process variations.

9.1 Power Consumption

For estimating the processor power, see the *AM64x / AM243x Power Estimation Tool*.

9.2 Maximum Current for Different Supply Rails

For information on the maximum current for different supply rails, see the AM64x Maximum Current Ratings.

9.3 Power Modes

The processor supports multiple power modes. For more details, see the *Device Power States* section in the *Device Configuration* chapter of the device-specific TRM.

9.4 Guidance on Thermal Design

The *Thermal Design Guide for DSP and Arm Application Processors* application report provides guidance for successful implementation of a thermal solution for board designs containing this processor. This application report provides background information on common terms and methods. TI only supports designs that follow thermal design guidelines contained in the application report.

The required Thermal model can be downloaded from the below sections.

9.4.1 AM64x

- AM64x / AM243x Thermal Model

9.4.2 AM243x

- AM243x Thermal Model

10 Schematic Capture and Review

At this stage of the design, schematic capture can be started. To support the schematics capture, see the below:

10.1 Selection of Components and Components Value

Be sure to use the recommended values in device-specific data sheet as applicable when selecting the passive components.

10.2 Schematic Capture

During the schematic capture phase, the schematics can be drawn newly or EVM schematics can be reused, see the *SK-AM64B (AM64B starter kit for AM64x Sitara processors)*, *TMDS64EVM (AM64x evaluation module for Sitara processors)* and *TMDS243EVM (AM243x evaluation module for Arm Cortex-R5F-based MCUs)* schematics.

During schematic capture, follow *AM6442, AM6422, AM6412 and AM2434 Schematic Design and Review Checklist* and *AM64x / AM243x Processor Silicon Errata*.

The below link summarizes the considerations designers have to be familiar when reusing TI EVM design files.

[FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 Custom board hardware design - Reusing TI EVM design files.

Note

When EVM schematics are reused, ensure the functionality and change in net name due to redesign are reviewed.

When EVM schematics are reused, the DNI setting could be reset. Make sure the DNIs are reconfigured (populating DNIs could affect the functionality).

10.3 Reviewing the Schematics

After completing the schematic capture, verify the design against the *AM6442, AM6422, AM6412 and AM2434 Schematic Design and Review Checklist*.

Plan an internal schematic review to review the schematics with reference to the schematic design and review checklist. Verify circuit implementation for errors, value or connection inaccuracies, missing net connections, and so forth. Be sure to verify the schematics for pin connectivity requirements.

11 Floor Planning, Layout and Routing Guidelines

After completing the schematic capture and review, TI recommends floor planning of the board to determine the interconnect distances between the various devices, board size and outline. The next design step is the PCB layout. For information supporting the board layout, see the following sections.

11.1 Escape Routing Guidelines

The *AM64x / AM243x BGA Escape Routing* user's guide provides a sample PCB escape routing for the AM64x / AM243x processor.

11.2 DDR Layout Guidelines

TI provides *AM64x / AM243x DDR Board Design and Layout Guidelines*. The goal of the application note is to make the DDR4 and LPDDR4 interface implementation simpler. Requirements have been captured as a set of layout (placement and routing) guidelines that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using DDR4 or LPDDR4 memories that follow the guidelines in this application note.

The target impedance is 40-ohms (single-ended) and 80-ohms (differential) on the DDR traces.

For the propagation delay, the delay to be considered for DDR4 or LPDDR4 is the delay related to the traces on the board. There is no need to include package level propagation delay.

In-case package level propagation delay is required, reach-out to the local TI sales representative.

Refer DDR board design and layout guidelines for DDR4 data rate, device bit width, device count and LPDDR4 Count, Channel Width, Channels, Die, Ranks. Guidelines for bit swapping is also included.

It is highly recommended to perform signal integrity simulations during board design.

11.3 High-Speed Differential Signal Routing Guidance

The *High-Speed Interface Layout Guidelines* application note provides guidance for successful routing of the high-speed differential signals. This includes PCB stack-up and materials guidance as well as routing skew, length, and spacing limits. TI supports only designs that follow the board design guidelines contained in the application report.

Note

Consider using the *SK-AM64B (AM64B starter kit for AM64x Sitara processors)*, *TMDS64EVM (AM64x evaluation module for Sitara processors)* and *TMDS243EVM (AM243x evaluation module for Arm Cortex-R5F-based MCUs)* layouts as reference.

11.4 Additional References for Simulation

Refer *Board Design Simulations* chapter of the *AM62A3 / AM62A7 DDR Board Design and Layout Guidelines* and *AM625 / AM623 DDR Board Design and Layout Guidelines* application notes.

12 Device Handling and Assembly

Recommended reviewing the device thickness information, ball pitch, Lead finish/Ball material and the recommended MSL rating/Peak reflow to be followed.

For more information, see the *AM64x Ordering and quality*, *MSL Ratings and Reflow Profiles* and *Moisture sensitivity level search*.

13 References

13.1 AM64x

- Texas Instruments: *AM64x Sitara™ Processors Data Sheet*
- Texas Instruments: *SK-AM64B (AM64B starter kit for AM64x Sitara processors)*
- Texas Instruments: *TMDS64EVM (AM64x evaluation module for Sitara processors)*
- Texas Instruments: *TMDS64GPEVM (General-purpose evaluation module for Sitara processors)*
- Texas Instruments: *TMDS64DC01EVM (AM64x IO-link and high-speed breakout card)*
- Texas Instruments: *Powering the AM64x with the TPS65220 or TPS65219 PMIC*
- Texas Instruments: *Powering the AM64xx with the LP8733xx PMIC*

13.2 AM243x

- Texas Instruments: *AM243x Sitara™ Microcontrollers Data Sheet*
- Texas Instruments: *TMDS243EVM (AM243x evaluation module for Arm Cortex-R5F-based MCUs)*
- Texas Instruments: *LP-AM243 (AM243x general purpose LaunchPad™ development kit for Arm®-based MCU)*
- Texas Instruments: *TMDS243DC01EVM (AM243x and AM64x evaluation module breakout board for high-speed expansion)*
- Texas Instruments: *Powering the AM243x With the TPS65219 PMIC*

13.3 Common

- Texas Instruments: *AM64x / AM243x Sitara Processors Technical Reference Manual*
- Texas Instruments: *AM64x / AM243x Processor Silicon Errata*
- Texas Instruments: *AM64x / AM243x Power Estimation Tool*
- Texas Instruments: *AM64x / AM243x Schematic Design and Review Checklist*
- Texas Instruments: *AM64x and AM243x BGA Escape Routing*
- Texas Instruments: *AM64x / AM243x DDR Board Design and Layout Guidelines*
- Texas Instruments: *AM62A3 / AM62A7 DDR Board Design and Layout Guidelines*
- Texas Instruments: *Thermal Design Guide for DSP and Arm Application Processors Application Report*
- Texas Instruments: *PRU-ICSS Feature Comparison*
- Texas Instruments: *Industrial Communication Protocols Supported on Sitara™ Processors and MCUs*
- Texas Instruments: *Sitara Processor Power Distribution Networks: Implementation and Analysis*
- Texas Instruments: *Emulation and Trace Headers Technical Reference Manual*
- Texas Instruments: *High-Speed Interface Layout Guidelines*
- Texas Instruments: *Hardware Design Guide for KeyStone II Devices*

14 Terminology

ADC – Analog-to-Digital Converter

BSDL – Boundary-Scan Description Language

CPSW3G – Common Platform Ethernet Switch 3-port Gigabit

DRD – Dual-Role Device

E2E – Engineer to Engineer

ECAP – Enhanced Capture

ECC – Error-Correcting Code

eMMC – embedded Multi-Media Card

EMU – Emulation Control

EPWM – Enhanced Pulse-Width Modulator

EQEP – Enhanced Quadrature Encoder Pulse

FAQ – Frequently Asked Question

FSI_RX – Fast Serial Interface Receiver

FSI_TX – Fast Serial Interface Transmitter

GPIO – General Purpose Input/Output

GPMC – General-Purpose Memory Controller

HS-RTDX – High Speed Real Time Data eXchange

I2C – Inter-Integrated Circuit

IBIS – Input/Output Buffer Information Specification

IEP – Industrial Ethernet Peripheral

JTAG – Joint Test Action Group

LDO – Low-Dropout

LVCMOS – Low voltage complementary metal oxide semiconductor

MAC – Media Access Controller

MCAN – Modular Controller Area Network

McSPI– Multichannel Serial Peripheral Interfaces

MDIO – Management Data Input/Output

MII – Media Independent Interface

MMC – Multi-Media Card

MSL – Moisture Sensitivity Level

OPP – Operating Performance Point

OSPI – Octal Serial Peripheral Interface

OTP – One-Time Programmable

PCB – Printed Circuit Board

PCIe – Peripheral Component Interconnect Express

PMIC – Power management integrated circuit

POR – Power-on Reset

PRU_ICSSG – Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit

PWM – Pulse-Width Modulator

QSPI – Quad Serial Peripheral Interface

RGMII – Reduced Gigabit Media Independent Interface

RMII – Reduced Media Independent Interface

SD – Secure Digital

SDIO – Secure Digital Input Output

SDK – Software Development Kit

SGMII – Serial Gigabit Media Independent Interface

SPI – Serial Peripheral Interface

TCK – JTAG Test Clock Input

TCM – Tightly Coupled Memory

TDI – JTAG Test Data Input

TDO – JTAG Test Data Output

TMS – JTAG Test Mode Select Input

TRM – Technical Reference Manual

TRSTn – JTAG Reset

UART – Universal Asynchronous Receiver/Transmitter

USB – Universal Serial Bus

XDS – eXtended Development System

15 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2022) to Revision A (July 2023)	Page
• Added Abstract to this document	1
• Updated the numbering format for tables, figures and cross-references throughout the document	2
• Updated Section 1.3	3
• Updated Section 2.1	3
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• Added Section 3.5.1	7
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