Application Note Jacinto7 AM6x/TDA4x/DRA8x Schematic Checklist



ABSTRACT

This application report highlights the Jacinto7 AM6x/TDA4x/DRA8x Schematic Checklist Tool, which provides board design recommendations when using selected AM6x, TDA4x, and DRA8x devices. The tool is intended to supplement the information provided in the device-specific technical reference manual and data sheet. It is not an all-encompassing list, but rather a succinct reference for board designers that highlights certain caveats and care-abouts related to different use cases. Links for additional device product pages and reference documents will be added as they become available.

The spreadsheet discussed in this document can be downloaded here.

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1 Introduction

The Jacinto7 AM6x/TDA4x/DRA8x Schematic Checklist Tool provides a supplemental design check when creating designs with AM6x, TDA4x, and DRA8x devices. The tool enables customers to review critical aspects of their design as well as track which items have been reviewed and which might still need additional attention. This document provides a detailed description on how to use the spreadsheet/tool and address some of the common questions/issues that can arise.

This tool is a companion to the other processor documentation (Data Manual, Technical Reference Manual, and so forth) and does not replace it or any documentation. If there are any discrepancies between this spreadsheet/ tool and other documents, the documents take precedent (unless otherwise noted).

In reviewing a schematic design, often the Checklist Tool will refer you to TI's EVM design(s). In case of any discrepancy between TI EVMs and the device-specific data sheet, or other documentation, always follow the documentation (unless otherwise noted). Despite the designer's best efforts, the EVMs may contain errors that still function but are not completely aligned with the data sheet specification. The EVM designs are a great place for design information, but should not be considered as reference designs to be blindly reused.

1.1 Supporting Documentation

The Jacinto7 AM6x/TDA4x/DRA8x Schematic Checklist Tool supports the following devices:

- J7200
 - DRA821
- J721E
 - DRA829
 - TDA4VM
- J721S2
 - AM68x
 - TDA4VE
 - TDA4AL
 - TDA4VL
- J722S
 - AM67x
 - TDA4VEN
 - TDA4AEN
- J742S2
 - TDA4VPE
 - TDA4APE
- J784S4
 - AM69x
 - TDA4VH
 - TDA4AH
 - TDA4VP
 - TDA4AP

For AM6x parts not in this list (for example, AM644x, AM62x), see the individual checklist documents on the product pages. For example: https://www.ti.com/product/AM6442#tech-docs

Links to TI hardware designs referenced by the checklist tool and/or to be used for reference:

- J7200XSOMXEVM DRA821 System-on-Module EVM
- J721EXCP01EVM Common Processor for Jacinto 7 System-on-Modules
- J721EXSOMXEVM TDA4VM and DRA829 System-on-Module EVM
- J721S2XSOMXEVM TDA4VE, TDA4VL, and TDA4AL System-on-Module EVM
- J722SXH01EVM AM67x, TDA4VEN, TDA4AEN Evaluation Module
- J784S4XEVM TDA4VH, TDA4AH, TDA4VP, TDA4AP Evaluation Module
- SK-AM68 AM68 Processor Starter Kit
- SK-AM69 AM69 Processor Starter Kit
- SK-TDA4VM TDA4VM Processor Starter Kit for EdgeAI Vision Systems

TIDEP-01022 – Gateway Automotive Reference Design

Check the relevant Jacinto Processors Silicon Errata document when designing a board. This document contains important information on silicon issues that affect your board design.

Other useful application notes and links:

- Jacinto 7 AM6x/TDA4x/DRA8x High-Speed Interface Layout Guidelines
- Jacinto 7 AM6x/TDA4x/DRA8x LPDDR4 Board Design and Layout Guidelines
- System Configuration Tool

2 Schematic Checklist Tool

2.1 Features

The key features of the Schematic Checklist Tool are highlighted in this section. The tool covers are wide range of topics regarding board design. However, the list is not exhaustive, and other items might need to be verified in your design. If you have specific questions about this tool or aspects of a design not covered by this tool, submit a ticket on the TI E2E support forums.

Topics covered in this tool include:

- Power
- Reset
- Clocks
- Boot Modes
- Unused/Reserved Pins
- LPDDR4 Memory
- Serial Flash Memory
- High Speed Serial Interface
- Debug Support
- Other (I2C, MMC, ADC, and so forth)

2.2 Spreadsheet Overview

The Schematic Checklist Tool is comprised of Excel spreadsheet consisting of two worksheets: Checklist and Revision.

When loading a new/blank file, the Checklist worksheet is selected by default. This is worksheet that is used to conduct the schematic review.

TEXA INST	S RUMENTS	Jacinto7 Schematic Checklist	Tool	Revision: 2.00.0 Date: 02/01/2023
	Step 1: Enab	le Macros in Spreasheet (else tool will not function o	orrectly)	
	Step 2: Selec	t Device from Drop-Down Menu		
		Click to Select Device		
	Step 3. Com	plete Each Checklist Item / Update Status as	Appropria	te
		Addition	al information ca	n be found in the corresponding documenation: SPRUtbd
Topic •	Function	Item	Status 🔻	Comment/Notes
	Checklist wil	I populate after selecting device.		

Figure 2-1. Schematic Checklist Tool Default View

The 'Revision' worksheet provides the history of changes for each revision of the tool, including updates to design recommendations, new board design items, and support for new devices as they become available.



2.3 Checklist Worksheet

2.3.1 Step 1: Enable Macros in Spreadsheet

The checklist tool is excel-based, and uses macros to configure the board design recommendations specific to each processor/device. For the checklist to function properly, Macros **MUST** be enabled.

When loading the file AM6x_DRA8x_TDA4x_SchemCheckList_Tool.xlsm into Excel, the following may appear at top of screen if macros are not already enabled. Make sure to select 'Enable Content'.

1	SECURITY WARNING	Macros have been disabled.	Enable Content

Figure 2-2. Warning: Enable Macro Content

Macros can also be enabled using Excel's menu. From Excel's menu, select 'File', 'Options', and 'Trust Center'. Then click 'Trust Center Settings'. In the Trust Center, select 'Macro Settings'.

Trust Center			?	×
Trusted Publishers	Macro Settings			
Trusted Locations Trusted Documents Trusted Add-in Catalogs Add-ins	 Disable all macros without notification Disable all macros with notification Disable all macros except digitally signed macros Excepted all macros (ext excepted digitally dependent on pin) 			
ActiveX Settings Macro Settings	Enable all macros (not recommended; potentially dangerous code can run) Developer Macro Settings Transported to VIA excised which model			
Protected View Message Bar	\Box Trust access to the <u>V</u> BA project object model			
External Content File Block Settings Privacy Options				
		OK		Cancel

Most configurations should select the second option 'Disable all macros with notification'. This selection disables macros, but then provides the option to selectively enable with security warning (previously discussed). Optionally you can select the fourth option 'Enable all macros'. However, as noted in the dialog box, this can open users up to harmful macros, and should be avoided if possible. Once the selection is made, Excel might need to be restarted and the checklist file reloaded.

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2.3.2 Step 2: Select Device From Drop-Down Menu

Select 'Click to Select Device' and a drop-down menu appears listing all of the processors/devices supported by this tool. Select the device for which is included in your design. If your device is not shown, it is currently not supported by this tool. For those devices not included, see the device-specific processor's product page on TI.com for information on the individual schematic checklist documents.

	AS TRUMENTS	Jacinto7 Schematic Chec	klist	Tool		Revision: 2.00.0 Date: 02/01/2023
	Step 1: Enab	le Macros in Spreasheet (else tool will not f	unction co	orrectin		
	Step 2: Selec	t Device from Drop-Down Menu Click to Select Device	K			
	Step 3. Com	plete Each Checklist Item / Update Sta				ing documenation: SPRUtbd
Торіс	Function	Item	×	Status	Comment/Notes	*
	Checklist wi	Il populate after selecting device.				

Figure 2-3. Select Device Used in Design

Once the device is select, the tool creates the relevant board design recommendations/checklist and updates the spreadsheet as shown in Figure 2-4.

V TEXAS INSTRUMENTS Jacinto7 Schematic Checklist		Jacinto7 Schematic Checklis	st Tool Revis Date 0			
	Device:	TDA4VM				
			Additiona	I information ca	n be found in the corresponding documenation: SPRUtbd	
Topic	Function	Item 👻	AM66 / DRA829 / TDA4VM Device Details	Status 👻	Comment/Notes	
Power	Power Estimates	Have you used the output of the power model and estimates from the rest of your design to determine the power solution needed?	The power needed for each rail of the processor will vary based on the interfaces used and the environment in which it is operating. Power requirements must be determined using the power model. See ti com for additional information.	Not Checked		
	Power Delivery Solution	Check that the design utilizes one of the recommended and supported power delivery solution/schemes defineed for this processor.	The processor includes a many different power rails which must be powered with the correct voltage and correct sequence for poper operation. It is TSDNOILY commended all designs using one of the defined PDMs (Power Delivery Helwonks) for powering the processor. These power solutions are specifically defined to work with the processor and provide several different options for power/cost targets. When using one of the PDMs, be aware the SMPS/LDO default voltages, power up/down sequences, and GPIO pin assignments are all defined as part of the Power belivery solution. Check with the corresponding PDM User's Guide and/or the Power			
		Doer the related ocuer colution account for latest ocuer estimates	Management IC (PMIC) documentation for latest released details. Link to recommended Power Solutions applicaton note: TT's EVM was released prior to finalizing all the power estimations and testing of the processor. The power models and power	Not Checked		
		where CORE can exceed the implemented power solution on TI's	solutions have since been updated to include additional power capacity for VDD_CORE. This increase is not accounted for in			
	Voltage Assignments (MCU)		Nominal voltage for VDD_MCU is 0.85V. Power Pins: 120, M19, M21 Nominal voltage is 0.85V.	Not Checked		
		Review with PDN (identified in other checklist entry) to ensure rail sourced from correct supply	Power Pins for VDDAR_MCU: K19, T19	Not Checked		
		Have you checked that the correct voltage(s) are applied to the MCU Analog power rail to the device (VDA_MCU_1V8)?	Nominal voltage for VDDA_ADC_MCU is 1.80V. Power pins: N22, M23 Nominal voltage for VDDA WKUP is 1.80V. Power pins: H22	Not Checked		
		Review with PDN (identified in other checklist entry) to ensure rail	Nominal voltage for VDDA_WKUP is 1.80V. Power pins: H22 Nominal voltage for VDDA POR WKUP is 1.80V. Power pins: P22	Not Checked		
		sourced from correct supply	Nominal voltage for VDDA_FOR_WKOP is 1.80V. Power pins: P22 Nominal voltage for VDDA_MCU_PLIGRP0 is 1.80V. Power pins: G18	Not Checked		
			Nominal voltage for VDDA_MCU_TEMP is 1.80V. Power pins: P21	Not Checked		

Figure 2-4. Example Schematic Checklist for TDA4VM

The checklist can be reset by changing the device back to 'Click to Select Device'. This resets all status values back to default and erases all comments. Changing the device from one processor to another creates the checklist for the new device, and also resets status and/or comments that may have already been entered. Another method to reset the checklist is to just release the original file again.

If the checklist does not appear, then its possible macros are not enabled in your running version of Excel.

2.3.3 Step 3: Complete Each Checklist Item / Update Status as Appropriate

The tool has created the checklist and ready for the schematic review. The expectation is that the reviewer will read each board design recommendation/item and use the information provided in the tool (and supporting documentation) to review their design. As the reviewer proceeds through the checklist, the status dropdown box can be used for the reviewer to document the status and the comment box can log any questions/comments that require follow-up.

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The Schematic Checklist Tool worksheet is organized by different columns, including Topic, Function, Item, Device Details, Status, and Comments/Notes. Each column is described in detail below:

- **Topic:** The checklist is organized into major sections, referred to as Topics. The checklist can be sorted and filtered by Topic, helping users focus their review efforts on specific areas of their schematic design. Examples include Power, Clocks, Reset, LPDDR4, and so forth.
- Function: Each Topic is broken into several functional groups referred to as Functions. Examples
 of Function within the Power Topic include Power Estimation, Power Delivery, Power Rails, and Power
 Sequence. The checklist can be sorted/filtered Function.
- Item: Each row in the spreadsheet is a unique board design recommendation. It is recommended each item reviewed against the user's schematic/design to help ensure design correctness. Each Item can be specifically tracked (status) and logged with feedback comments.
- **Device-Details:** Device details provides additional review details/information that could change with each processor. It can also provide device specific review statements or conditions.
- Status: The status field is a user updateable field, and provides the status for a specific schematic review item. Each item provides a drop-down menu providing one of four possible status selections. Each status is assigned a different color to help visually identify each. The checklist can be sorted/filtered on Status.

Status Selection	Status Description					
Not Checked (Default). Each review item defaults to 'Not Checked' to indicate the task has not been started						
Verified	Indicates the item/task has been reviewed in the schematic/design, and verified to be correct.					
N/A	Indicates the item/task is not applicable for this design. Possible reasons could include a specific interface is not used, thus those review tasks are not relevant.					
Issue/Open	Indicates the schematic/design may not align with the review information or other supplemental documentation. It could also be used to highlight open questions that are currently being investigated by the reviewer. Any questions that may need help from TI should be submitted to e2e.ti.com for follow-up.					

Table 2-1. Status Definitions and Usage

• **Comments/Notes:** This user update-able field provides ability for reviewer to add comments or notes to a specific board design checklist item.

3 References

- Texas Instruments: Jacinto 7 High-Speed Interface Layout Guidelines
- Texas Instruments: Jacinto 7 LPDDR4 Board Design and Layout Guidelines

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	hanges from Revision A (February 2023) to Revision B (April 2024)	Page
•	Added support for J722S and J742S2 devices	1

C	hanges from Revision * (February 2023) to Revision A (May 2023)	Page
•	Updated associated zip file	2

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