Technical White Paper

Driver and Occupancy Monitoring Systems on AM62A

TEXAS INSTRUMENTS

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ABSTRACT

This technical white paper describes how the AM62A processor can be used to build automotive grade driver and occupancy monitoring systems.

Table of Contents

List of Figures

List of Tables

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1 Introduction

New Car Assessment Program (NCAP) regulations are a set of standards and testing procedures used to evaluate the safety performance of new vehicles. NCAP programs exist in all regions around the world including the United States, Europe, Australia and Japan, among others. Driver monitoring systems and occupancy monitoring systems play a critical role in NCAP regulation compliance by enhancing vehicle safety and occupant protection and directly impact the safety rating of the vehicle.

Driver monitoring systems (DMS) monitor the driver's attention, alertness and behavior to ensure they are actively engaged in the driving task. These systems typically deploy camera based and computer vision algorithms to detect signs of driver distraction, drowsiness, or impairment. DMS systems can also be integrated with other vehicle safety features such as lane departure warning and adaptive cruise control to improve their effectiveness.

Occupancy monitoring systems (OMS) are designed to detect the presence of vehicle occupants, including passengers and, in some cases, pets. These systems are generally also camera based and deep learning algorithms are used to determine whether seat belts are being used, if there are occupants in specific seats (for airbag deployment) and if the occupants meet certain requirements (such as child seats for children). OMS systems can help prevent or minimize injuries by providing seat belt reminders or adjusting airbag deployment based on the weight or size of the occupants. These systems are especially relevant for evaluating child occupant protection and can contribute to the safety rating of a vehicle.

This document provides an overview of the AM62A processor. Next, it is shown how its heterogeneous architecture enables deployment of DMS and OMS algorithms with the lowest compute and power. A typical DMS/OMS dataflow is presented and how the hardware feature sets in AM62A are used in a DMS/OMS system are discussed. This paper also highlights innovations in hardware like the ability to process RGB-IR sensors that enable the ability to create a complete DMS/OMS system with a single camera. A critical aspect in any automotive system is functional safety and we show the different functional safety considerations that need to be taken into account when building a DMS/OMS system with AM62A.

2 AM62A Processor

The AM62A microprocessor is a heterogeneous processor designed for camera analytics applications. There are different hardware accelerators optimized for different tasks thus enabling an optimized power and cost footprint. TI's image signal processor called the Vision processing accelerators (VPAC), Quad Arm® Cortex®-A53 cores along with TI proprietary C7x DSP and matrix multiplication accelerator (MMA) make the AM62A Sitara™ MPU, well suited for vision-based applications such as driver and occupancy monitoring and associated eye safety.

Functional safety compliance on AM62Ax is another differentiating factor which enables OEMs and Tier1s to target safety functions on auto or industrial systems integrated with AM62A. With this device, system integrators can target safety use cases such as monitoring the driver for sleep/alertness, child presence detection as well as comfort functions such as driver identification, HMI interaction, in-vehicle video calls, and so forth. AM62Ax device is targeting safety compliance to ISO-26262 ASIL-B and IEC-61508 SIL-2 for random fault integrity as well as ASIL-D / SIL-3 for systematic capability. Various on-chip diagnostics, freedom from interference features along with embedded MCU domain for safety monitoring reduces overall BOM cost by enabling application processing as well as safety functions on the same device.
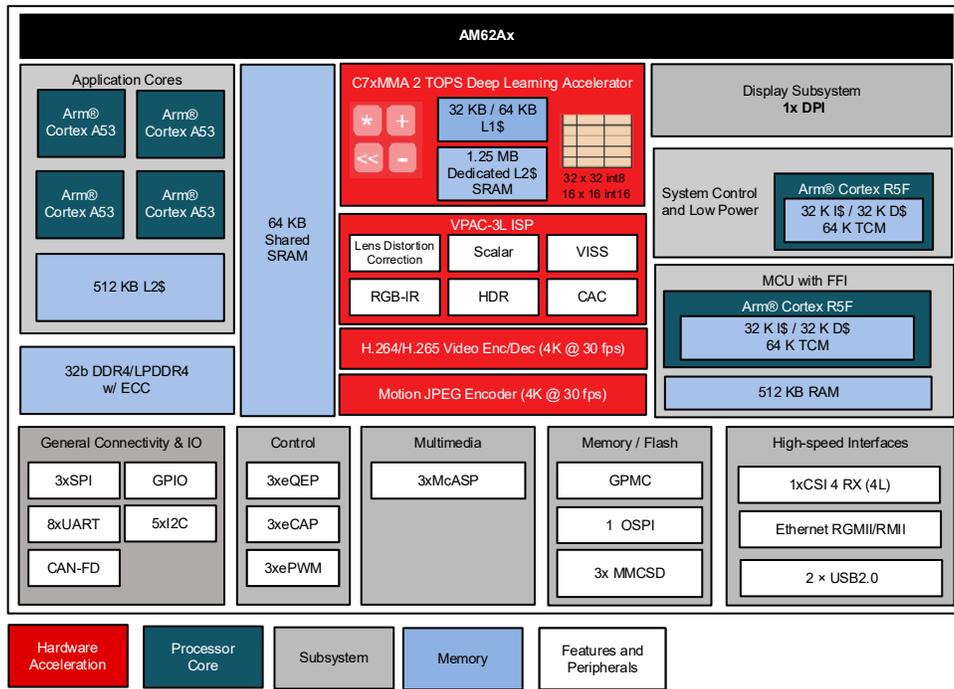
Figure 2-1. AM62A Simplified Block Diagram

The main processing and compute subsystems from a camera mirror system context in AM62A are as follows:

- Quad Arm Cortex-A53 cores: These can run up to 1.4 GHz and provide up to 16.8k Dhrystone Million Instructions Per Second (DMIPS) of performance.
- C7 Digital Signal Processor (DSP) and Matrix Multiplication Accelerator (MMA): TI's deep learning accelerator on AM62A is capable of two TOPs operations when clocked at 1GHz.
- Vision Processing Accelerator (VPAC3L): The latest generation in TI ISP technology for performing image operations some examples of which are color conversions, chromatic aberration correction, pyramid scaling and lens distortion correction. It also has dedicated hardware support for 4x4 RGB-IR color filter arrays (CFA) – a must for next generation DMS/OMS systems. VPAC3L has a total throughput of up to 300MP/s.
- VPU: The video processing unit has support for H.264/H.265 encode/decode with up to a total throughput capability of 240MP/s.

3 System Block Diagram

Figure 3-1 shows a typical DMS/OMS system block diagram based on the AM62A processor.
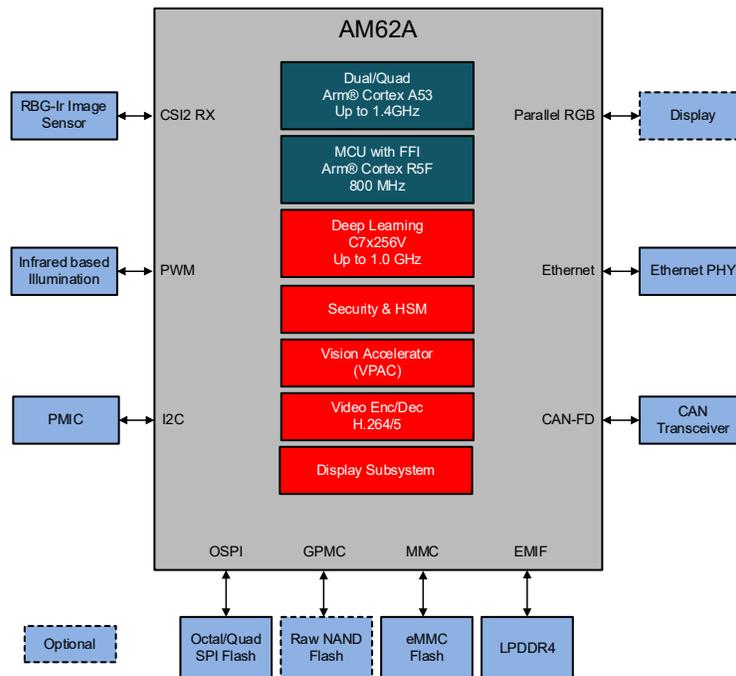

Figure 3-1. DMS/OMS System Block Diagram With AM62A

The CSI2 RX interface provides a single port 4-lane interface with a bandwidth of 1.5 Gbps per lane. This interface can handle the required bandwidth for a 5MP@60fps RGB-IR sensor or multiple sensor inputs through an external FPD-Link hub device. The AM62A processor combines processing cores and peripherals to create the DMS/OMS system while minimizing the Bill of Materials (BOM) for compact board and enclosure spaces like in a rearview mirror system. It incorporates a Cortex-R5F core and peripherals, including a CAN-FD controller, to run an isolated AutoSAR OS for system control, ensuring freedom from interference. Previously, legacy systems relied on an external MCU for this purpose, but the AM62A reduces system size and cost by integrating the MCU island with FFI. There is also support for various flash devices as boot sources, allowing system designers to select flash devices that meet the system cost or boot time requirements. Ensuring precise and safe infrared-based illumination, even in challenging lighting conditions within a car, is crucial for monitoring. The ASIL-B system requirements imply that the system has to be able to detect and control the maximum current and pulse-width within a single IR illumination pulse. Precise synchronization with the sensor is required for this purpose. Multiple PWM signals are necessary for controlling the illumination system and mechanical components in the DMS/OMS system. The AM62A supports over nine PWM output signals, thanks to ePWM, eCAP, and Timer modules, providing ample control signals for advanced DMS/OMS systems. The integrated Ethernet controller supports up to two ports and offers switch and TSN/AVB functionality for traffic scheduling and shaping. If needed, the Display Subsystem, equipped with a video pipeline and overlay features, can display the DMS/OMS system status on a screen via its DPI port. Additionally, Texas Instruments has developed a companion PMIC to support power resources and power supply sequences required by the AM62A. This PMIC includes integrated functional safety features such as a watchdog timer, facilitating the design of an ASIL-B system at the lowest possible cost.

4 Driver and Occupancy Mirror System Data Flow

Figure 4-1 illustrates the full data flow for processing of a 5MP 60 fps RGB-IR sensor for a driver and occupancy monitoring system.
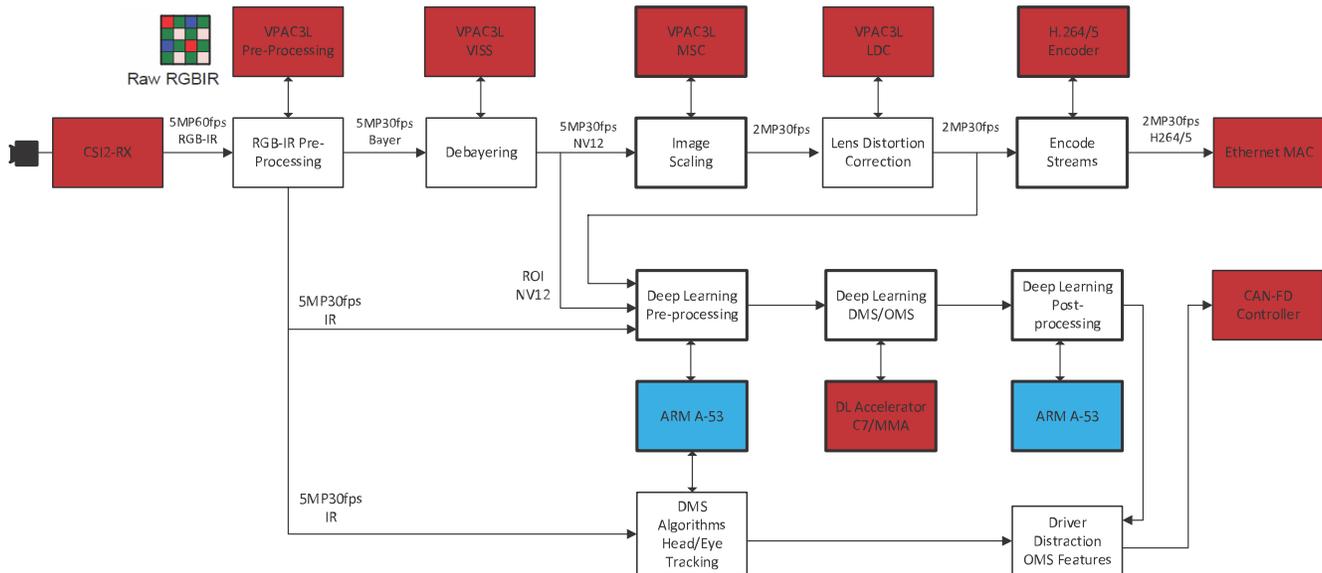

Figure 4-1. DMS/OMS Data Flow With AM62A

Upon reception via CSI2-RX, the RGB-IR data is fed into the newly developed RGB-IR pre-processing hardware integrated into the AM62A. This pre-processing hardware performs real-time separation of the RGB and IR components. The output can be either alternating RGB Bayer data and IR data at 30 frames per second for daytime mode, or IR data at 60 frames per second for night mode.

The received 5MP@30fps Bayer data is processed by the Vision Imaging Subsystem (VISS) module within the VPAC. The VISS module generates either RGB data or YUV data, depending on the desired image data format. This choice considers factors such as overall memory bandwidth requirements, image quality considerations, or input format compatibility with subsequent image processing modules. In this particular example, the NV12 format is utilized.

The output from the VISS module is then scaled down to the desired image resolution for video streaming or recording purposes using the Multi-Scalar (MSC) module. The Multi-Scalar module is capable of generating multiple pyramid scales in a single pass. To correct any lens distortion resulting from wide-angle lens used in Driver Monitoring Systems (DMS) or Occupant Monitoring Systems (OMS), the scaled-down image is processed by the Lens Distortion Correction (LDC) module.

For video streaming purposes, the H.264/265 video encode and decode hardware is employed to encode the 2MP@30fps video stream into the corresponding H.264/265 format. This processed video stream can then be transmitted over Ethernet.

The IR data acquired from the sensor is primarily utilized for eye tracking (Eye Lid and Gaze) and head tracking of the driver. At least 30fps of processing is required to detect eye lid opening and closing- a critical statistic required for drowsiness detection. Either classical computer vision techniques or deep learning analytic methods are used to detect the eyes and key points around the eyes. Classical computer vision algorithms can be implemented on the Arm Cortex-A53 cores while deep learning method based on convolution neural networks are implemented on the C7/MMA. Whereas DMS tasks typically need to be processed at a minimum of 30fps, the OMS tasks need only be performed at 1-5fps

AM62A is a heterogenous processor supporting different computing cores dedicated to running DMS/OMS algorithms. The C7x/MMA is a novel hardware deep learning engine capable of delivering up to 2 Tera Operations Per Second (TOPS) of compute capability. This deep learning engine is optimized for low power consumption, facilitating high-performance analytics within compact enclosures, such as rearview mirrors, without requiring additional cooling mechanisms.

Furthermore, the addition of the Cortex-A53 core serves as an additional hardware resource for running DMS algorithms that have already been validated and proven on AM62x devices in DMS products. This additional core provides supplementary performance when extra signal processing capabilities are required, in addition to the C7x/MMA Deep Learning accelerator.

5 Deep Learning Acceleration

Convolutional Neural Networks (CNN's) are well suited for several of the computer vision tasks required in a DMS/OMS system. As an example, for a DMS system the first step involves accurately identifying the key points around the drivers' eyes and mouth for accurate Gaze tracking and Drowsiness detection. Driver engagement may involve detecting the activity of the driver, for example, if the driver has food in his hands or is talking on the cellphone by his ear both of which are object detection tasks. For Occupancy monitoring systems the "child in the backseat" can be framed as an object detection task while the seat belt check for driver and passenger can be framed as a semantic segmentation problem. CNN's can be run on both ARM-A53 cores as well as C7/MMA deep learning accelerator

AM62A's deep learning accelerator is the C7/MMA DSP engine that is capable of up to 2TOPs of performance. It consists of a floating point C7- DSP that is coupled with a matrix multiply accelerator that is capable of multiplying two 8-bit vectors of length 32 in 1 cycle. When clocked at 1GHz, and counting a MAC as two operations it is capable of 2x32x32x1GHz=2 Tera Operations per second. The matrix multiply accelerator is a general-purpose accelerator and enables ~50x speed up when running typical Convolution Neural Networks compared to an A-53 core.

AM62A's SDK supports the three popular runtime frameworks for deploying and executing machine learning models namely a) tflite-runtime b) ONNX-runtime c) TVM. This enables the user to train your model anywhere and deploy into the hardware with only a few lines of your code using your favorite industry-standard Python or C++ application programming interface (API) from one of the frameworks. The TIDL compilation tools take care of all the memory optimizations required to map a network optimally to AM62A allowing the user to focus more on network design and selection.

TI also provides a model analyzer and model selection tool [2] that enables 3P perception stack providers to choose the deep learning model that will provide the maximum entitlement in terms of frames per second and accuracy. As an example, Table 5-1 illustrates the performance entitlement with SSDLite-MobDet-EdgeTPU-Coco model when running at 30 FPS.

Table 5-1. Example Performance of a CNN on AM62A With C7/MMA@850MHz

Model	Resolution	Target FPS	MAP Accuracy On CoCo	Latency (ms)	Deep Learning Utilization	DDR BW Utilization
SSDLite-MobDet-.EdgeTPU-coco	320x320	30	29.7	8.35	25%	504MB/s

6 Functional Safety in DMS/OMS Applications Using AM62A

## 6.1 Overview of Functional Safety Features on AM62A
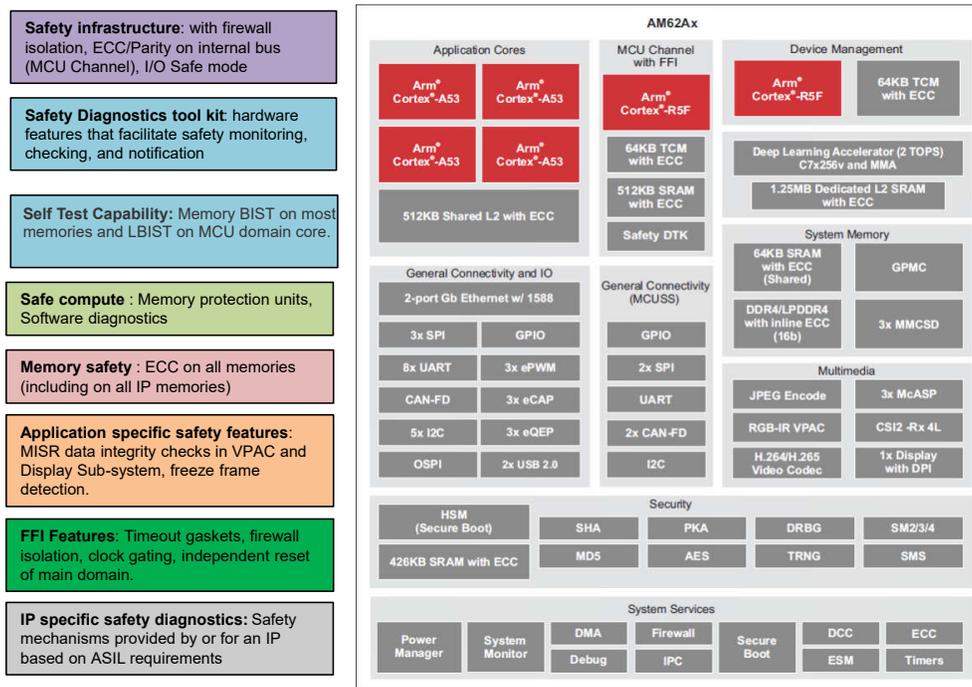
Figure 6-1. Overview of AM62A Functional Safety Features

Similar to several other Sitara MPU family of functional safety compliant devices, AM62A offers a myriad of safety features to meet targeted safety integrity levels for automotive and industrial applications. Key features are highlighted below.

- Device infrastructure enables partitioning the device into MCU domain for safety intensive functions and Main domain for application processing alone or a mix of application processing and safety functions. Safety infrastructure includes firewall isolation, ECC/parity on MCU domain interconnect and I/O safe mode.
- Safety diagnostics tool kit includes dedicated IP that facilitate safety monitoring, detection and reporting. Examples of such IP are DCC – Dual Clock Comparators, Internal Watchdogs, ECC aggregators, MCRC – Memory CRC, ESM – Error Signal Monitoring, VTM – Temperature Monitors, POK – Undervoltage and Overvoltage monitors, and so forth. Such dedicated diagnostic logic along with internal interrupt routing enable detection and reporting of faults within reasonable FTTI.
- Self-test capability includes memory BIST capability on several memories and LBIST capability on MCU domain core. Test for diagnostic features such as ECC/parity are also available on the device.
- Safe compute features such as memory protection units (MPU) and memory management units enable memory protection for cores. Software mechanisms such as program sequence monitoring, reciprocal comparison by software etc. are recommended in the safety manual for the detection of faults in CPU execution.
- Freedom from interference is provided by firewalls, timeout gaskets, clock gating features and hardware support for independent reset of main domain.
- Several hardware and software diagnostics can be enabled at a per functional IP level so as to meet application specific needs. For example, MISR data integrity checks in VPAC and DSS, hardware provided CSI protocol checks, and so forth.
- Common cause failure detection and reporting is enabled via dual clock comparators, on-chip clock loss detection logic, and so forth.

7 Functional Safety Targets and Assumptions of Use

AM62A targets ASIL-B as per ISO 26262 and SIL-2 as per IEC 61508 random fault capability on the entire device and targets ASIL-D/SIL-3 (SC 3) systematic capability on the device. AM62A is developed as Safety Element out of Context (SEooC). A list of assumptions of use are provided in the safety manual (available based on request).

8 Functional Safety in DMS/OMS Data Flow

Take the DMS/OMS data flow mentioned in Section 4 and break it down to see how IP specific functional safety diagnostics can be leveraged. Note that the safety mechanisms can be a combination of hardware as well as software diagnostic mechanisms that need to implemented by system integrator.
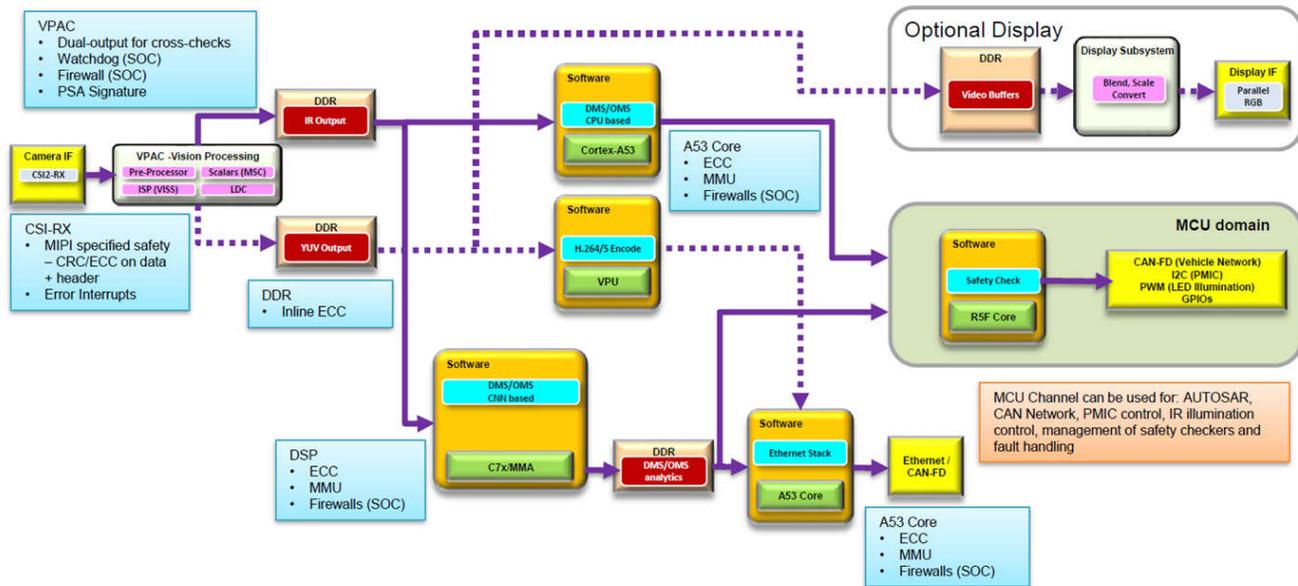
Figure 8-1. DMS/OMS Data Flow With Hardware Provided Safety Mechanisms

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Note

The analysis below assumes safety criticality in each step of the data flow/application. Other concepts which assume QM processing in main domain and safety function including safety monitoring in the MCU domain may be employed.

Note

Key IP involved in the data flow have been listed. Several other IP performing functions such as DMA, Inter-processor communication, boot haven not been listed. Failure modes and safety mechanisms shown here are a sample set. For complete recommendation of safety mechanism combinations to meet desired safety integrity levels, please refer the AM62Ax Functional Safety Manual.

Table 8-1. Data Flow Considerations in DMS/OMS Data Flow

Step in Data Flow	IP Involved and Failure Modes	Safety Mechanisms
1. Camera capture of RGB-IR data source	CSI-RX No image data transmitted or image corruption Hang during image data transmission	Hardware mechanisms – MIPI specified packet protocol checks, error interrupts, ECC protection of RAM data, watchdog Software mechanisms – Software processing of pixels within a frame and frame to frame
2. Transfer of camera captured data to DRAM for VPAC to read and process as well as to store processed image data	DDR Corruption of image data due to fault in DDR controller or interference due to lower ASIL function	Hardware mechanisms – DDR controller provided multi-phase ECC, device firewalls for isolation Software mechanisms – Information redundancy techniques applied to image data
3. Image processing of RGB+IR data and split of data into RGB and IR streams for further analysis	VPAC Corruption of image data Hang resulting in incorrect program flow	Hardware mechanisms – HWA (HTS) timers, internal watchdog timers, VPAC provided PSA signature computation, ECC/parity on critical memories Software mechanisms – Software processing of pixels within a frame and frame to frame, Golden Frame Testing
4. CNN based calculations for analytics of image data, Deep Learning Accelerator	C7x and MMA Corruption of image data Incorrect program execution causing algorithm to take incorrect decisions	Hardware mechanisms – C7x provided MMU, ECC on memories, device firewalls for isolation, dedicated watchdog Software mechanisms – Program flow monitoring or reciprocal comparison using another software implementation of DMS algorithm running on A53 core. **Note** – Software mechanisms such as program flow monitoring and reciprocal comparison by software are recommended in ISO 26262:2018-5
5. CPU based DMS algorithms running using classical vision techniques (Optionally – can be used for cross-checking the C7x core execution)	A53 core Incorrect program execution causing algorithm to take incorrect decision	Hardware mechanisms – MMU, ECC on memories, device firewalls for isolation, dedicated watchdog Software mechanisms – Program flow monitoring or reciprocal comparison by software, ARM provided STL mechanisms. **Note** – Software mechanisms such as program flow monitoring and reciprocal comparison by software are recommended in ISO 26262:2018-5.
6. AUTOSAR and CAN communication with external ECU, PMIC control, IR illumination control	MCU channel – MCU R5 core, MCU dedicated CAN Failure in communication with external ECU due to unresponsive core Message corruption Lower ASIL function from main domain causing interference with MCU domain function Incorrect program execution	Hardware mechanisms – ECC on MCU R5, CAN memories, LBIST on MCU R5 core, CAN protocol specific error detection, SOC firewalls for isolation, isolation mechanisms between Main and MCU domain. Software mechanisms – CRC in CAN message, program sequence monitoring on core, reciprocal comparison using another core on device

9 LED Driver Illumination Use Case

An extension of the DMS/OMS application is the need to provide eye safety by providing proper control of LED illumination. ASIL-B is typical safety integrity level targeted for this application. The software driver code that controls the LED via the LED driver is expected to run on the Cortex-R5 MCU. Safety mechanisms listed in Table 8-1 for MCU domain will be leveraged to provide protection of software driver code running on the Cortex-R5. LED driver shown in the diagram is an external component provided by system integrator. This LED driver can be functional safety qualified as well. Faults from the LED driver can then be further reported to the MCU R5. Software running on the Cortex-R5 MCU can take necessary action when faults are reported from external components such as the LED driver (GPIO can be used for fault communication) or internal fault reporting from error signal monitors within the AM62A device.
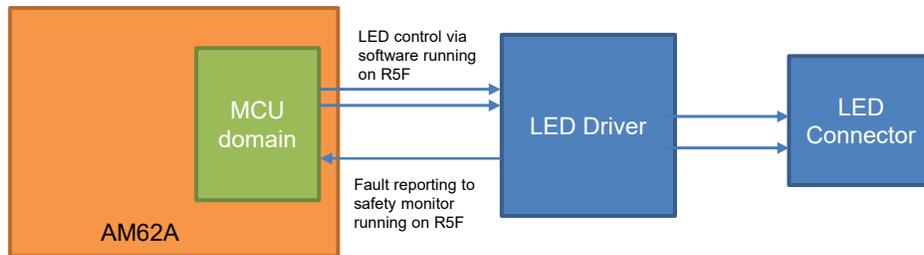
Figure 9-1. LED Driver Illumination Use Case

10 Summary

This technical white paper describes the enabling features in AM62A that make it a perfect fit for driver and occupancy monitoring systems. An overview is presented of a typical DMS/OMS data flow and how key operations map to the 62A IP blocks. Functional safety is a critical consideration in any automotive design and an in depth overview of how AM62A addresses functional safety requirements was presented.

11 References

1. AM62A3-Q1 Product Folder
2. AM62A7-Q1 Product Folder
3. Model Analyzer
4. SmartEye on AM62A

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