OMAP5910 Dual-Core Processor Camera Interface Reference Guide

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Read This First

About This Manual

The camera interface receives 8-bit parallel data with vertical and horizontal synchronization signals from an external camera module. The interface is connected to the 32-bit MPU-public-peripheral bus. Data can be retrieved either by the MPU directly or through the System DMA. Optionally, the clock and reset signals can be provided from the OMAP5910 device.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.

Related Documentation From Texas Instruments

The following documents describe the OMAP5910 device and related peripherals. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

OMAP5910MPU Subsystem Reference Guide (literature number SPRU671)

OMAP5910 DSP Subsystem Reference Guide (literature number SPRU672)

OMAP5910 Memory Interface Traffic Controller Reference Guide (literature number SPRU673)

OMAP5910 System DMA Controller Reference Guide (literature number SPRU674)

OMAP5910 LCD Controller Reference Guide (literature number SPRU675)

OMAP5910 Universal Asynchronous Receiver/Transmitter (UART) Devices Reference Guide (literature number SPRU676)

OMAP5910 Universal Serial Bus (USB) and Frame Adjustment Counter (FAC) Reference Guide (literature number SPRU677)

OMAP5910 Clock Generation and System Reset Management Reference Guide (literature number SPRU678)

OMAP5910 General-Purpose Input/Output (GPIO) Reference Guide (literature number SPRU679)

OMAP5910 MMC/SD Reference Guide (literature number SPRU680)

OMAP5910 Inter-Integrated Circuit (I2C) Controller Reference Guide (literature number SPRU681)

OMAP5910 Timer Reference Guide (literature number SPRU682)

OMAP5910 Inter-Processor Communication Reference Guide (literature number SPRU683)

OMAP5910 Camera Interface Reference Guide (literature number SPRU684)

OMAP5905 Multichannel Serial Interface (MCSI) Reference Guide (literature number SPRU685)

OMAP5910 Micro-Wire Interface Reference Guide (literature number SPRU686)

OMAP5910 Real-Time Clock (RTC) Reference Guide (literature number SPRU687)

OMAP5910 HDQ/1-Wire Interface Reference Guide (literature number SPRU688)

OMAP5910 PWL, PWT, and LED Peripheral Reference Guide (literature number SPRU689)

OMAP5910 Dual-Core Processor Multichannel Buffered Serial Port (McBSP) Reference Guide (literature number SPRU708)

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The camera interface receives 8-bit parallel data with vertical and horizontal synchronization signals from an external camera module. The interface is connected to the 32-bit MPU-public-peripheral bus. Data can be retrieved either by the MPU directly or through the System DMA. Optionally, the clock and reset signals can be provided from the OMAP5910 device.

1.1 Functional Architecture

The camera interface provides the following four functions:

- Buffer:

  A buffer is used to store the data word received from the camera module and transfer it to the MPU peripheral bridge using the DMA mode or the CPU mode. It contains a 128-word FIFO.

  Four consecutive 8-bit data groups from the camera module are combined into a single 32-bit data group for the maximum use of the 32-bit-wide TIPB.

- Clock divider:

  This function is mainly used to manage clock division and to handle the external clock generation for synchronous/asynchronous mode gating.

- Interrupt generator:

  An interrupt is generated to indicate the start and end of a frame, the start and end of a line, and a FIFO overflow condition.

- TIPB registers:

  Status, control, and data 32-bit registers connect via the TIPB.

Figure 1. Camera-Interface Block Diagram

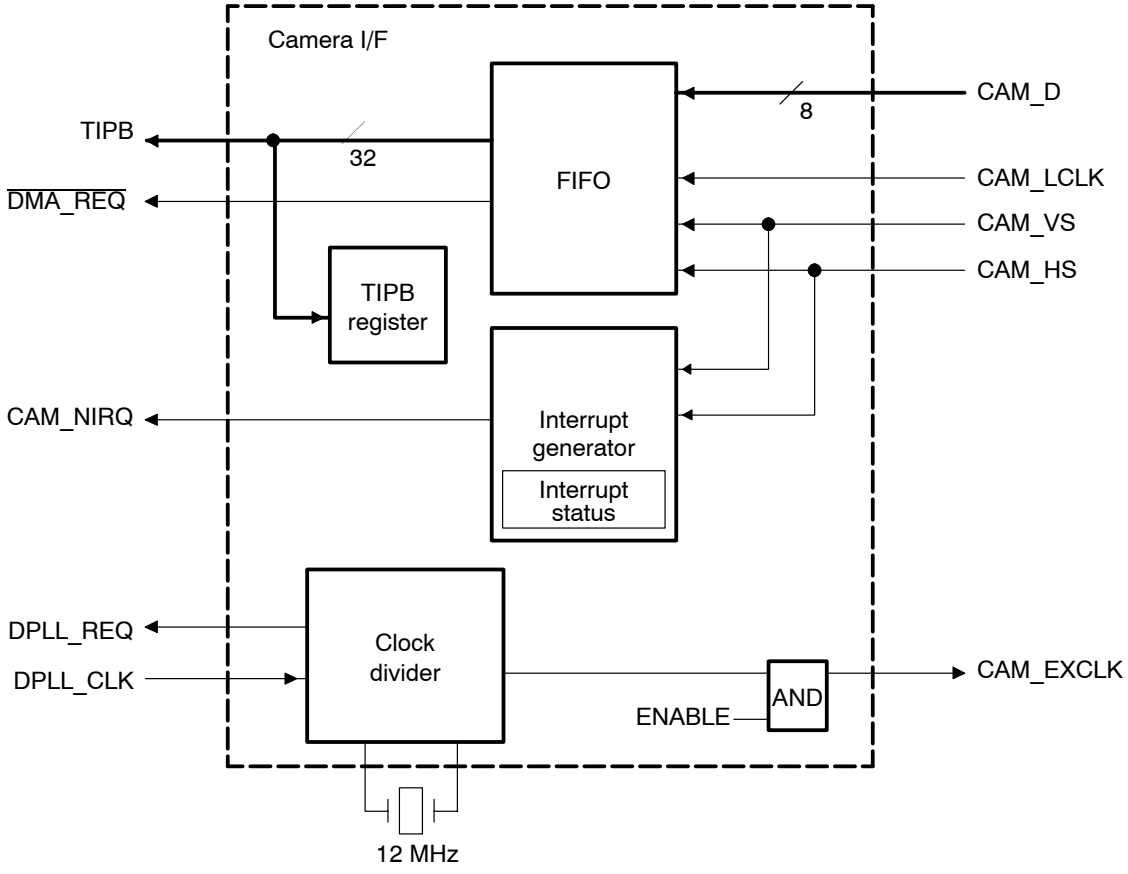
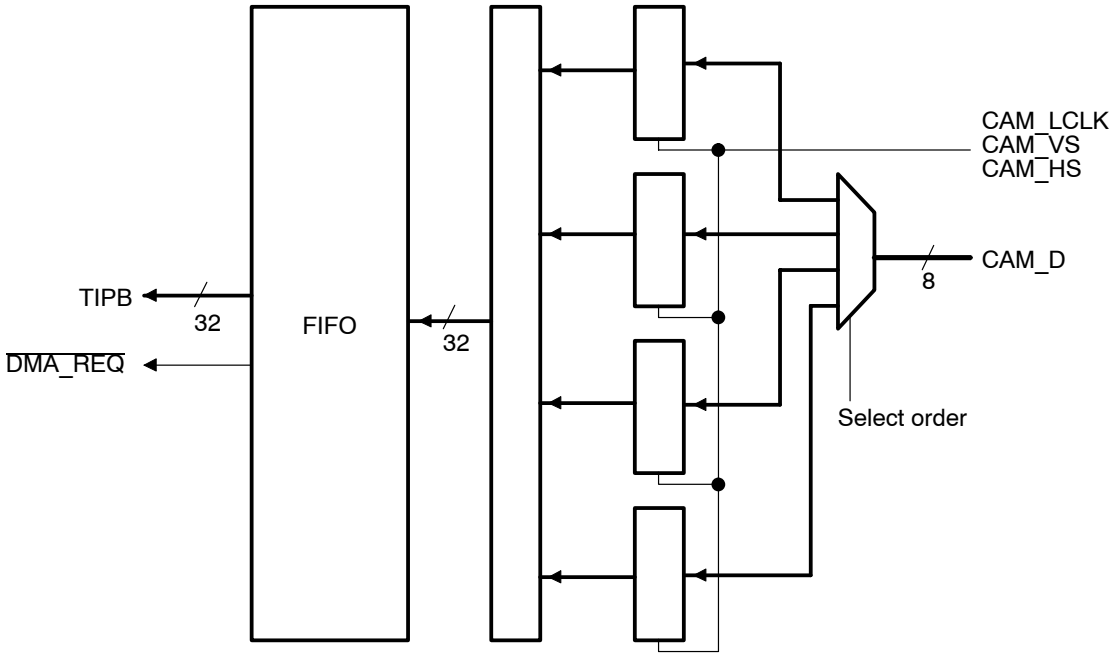


Figure 2. Image Data Transfer



1.1.1 Camera Data Validation

The incoming byte on the camera interface data bus (CAM.D) can be latched on the rising or falling edge of the camera interface line clock (CAM.LCLK) generated by the camera itself. The POLCLK bit can select the polarity of the CAM.LCLK in the clock-control register.

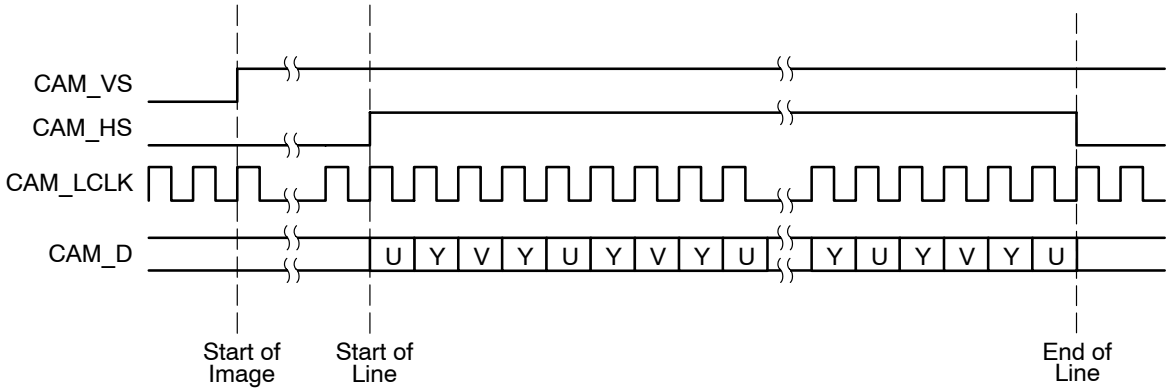
Program the camera interface so that data is always captured opposite the launch edge. For example, if the camera module outputs data on the rising edge of the CAM.LCLK, configure the interface to latch the data on the falling edge of the CAM.LCLK.

The high level of the camera interface vertical sync (CAM.VS) and camera interface horitzontal sync (CAM.HS) signals indicates that the data is valid on the CAM.D. These levels can be monitored by the MPU program through the VSTATUS and HSTATUS fields in the STATUS register, respectively.

The CAM.LCLK must be running even during the VSYNC and/or HSYNC blanking periods. The camera interface uses the CAM.LCLK to flash coalescing data buffers and prepare the next line/frame.

If either the CAM.VS or CAM.HS negates before all of the coalescing buffers are filled, the remaining data is discarded by the next CAM.LCLK edge and is not written into the FIFO.

Figure 3. Timing Chart of Image Data Transfer (POLCLK = 1)



1.1.2 Autostart

The camera module starts retrieving data when the CAM.VS activates. This mechanism ensures that the transfer starts at the beginning of the image.

Note:

If a reset FIFO occurs (see Section 1.1.3) while the interface is latching data, the capture is automatically disabled and the autostart function is enabled.

1.1.3 Reset FIFO

Setting the RAZ_FIFO bit in the Camera-Interface-Mode Register (MODE) clears any remaining data in the coalescing buffers, and resets, the FIFO with its read and write pointers, the interrupt status, and the FIFO peak counter.

Before starting a new transfer, any remaining data must be cleared by setting the RAZ_FIFO field in the following sequence.

1) Set the LCLK_EN field in the Clock-Control Register (CTRLCLOCK) to disable the CAM.LCLK signal.

2) Set the RAZ_FIFO bit to clear any remaining data and reset the FIFO.

3) Clear the LCLK_EN field to enable the CAM.LCLK signal.

4) Clear the RAZ_FIFO bit to start the camera-interface function.

1.1.4 Set of Order

As mentioned earlier, the camera-interface module inputs 8-bit data and outputs 32-bit data to the MPU-public-peripheral bus. The ORDERCAMD field in the Camera-Interface-Mode-Configuration Register (MODE) specifies the YUV word order from the camera interface module as shown in Figures 4 and 5.

Figure 4. Order of Camera Data on TIPB (Not Swapped)

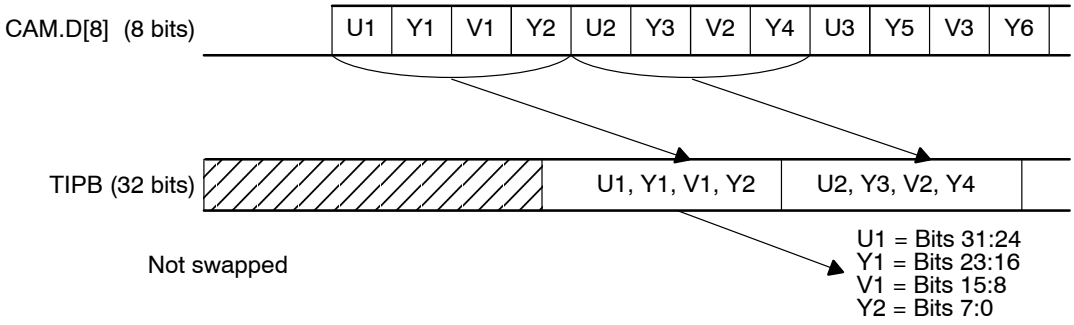
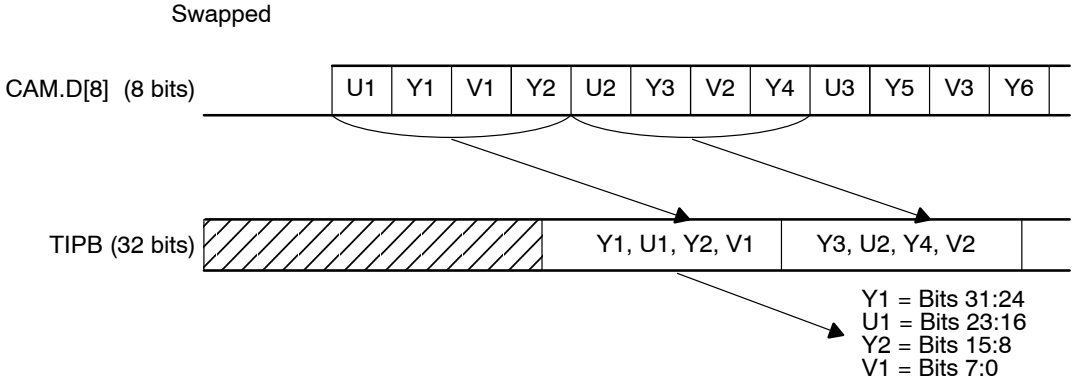


Figure 5. Order of Camera Data on TIPB (Swapped)



1.1.5 FIFO Buffer (128 x 32)

The THRESHOLD field in the Camera-Interface-Mode-Configuration Register (MODE) sets the trigger level of the FIFO between 1 and 128 in the 32-bit word. Either the MPU interrupt or the DMA request is generated when the FIFO counter reaches the trigger level.

In the DMA mode, the trigger level must be set to the same size as the DMA transfer to obtain maximum performance. Setting the transfer size to a value greater than the trigger level may result in unexpected behavior.

The FIFO continues to receive up to 128 values regardless of an MPU interrupt or a DMA transfer acknowledgement. The next DMA request is generated immediately after the current DMA transfer is completed if new new data in the FIFO reaches the trigger level again before the current DMA transfer is completed.

Setting the trigger level to 0 generates an MPU interrupt or a DMA request every time the 32-bit data is received.

Figure 6. DMA Request

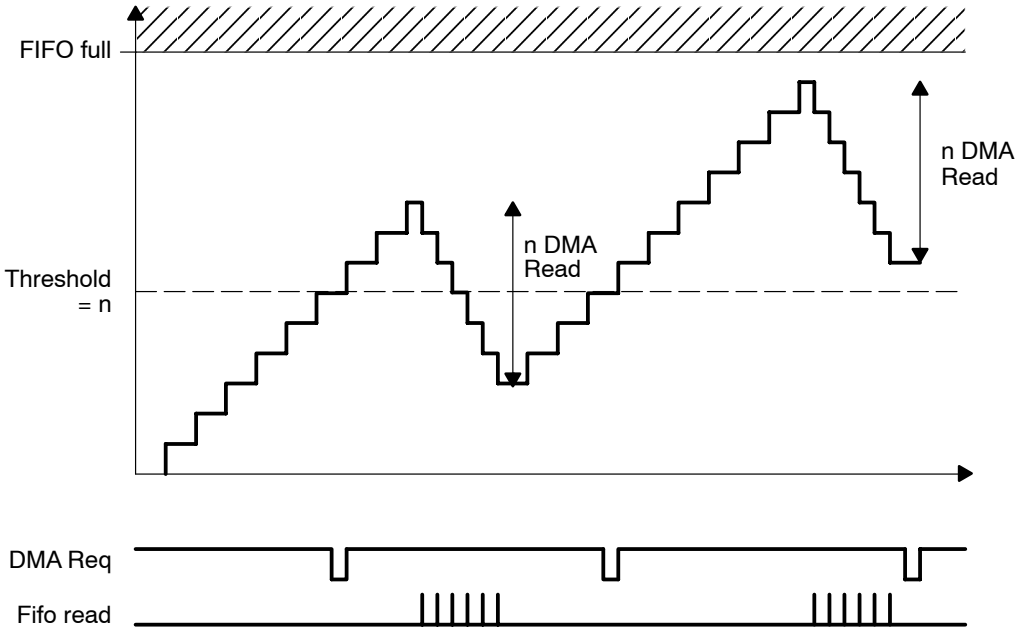
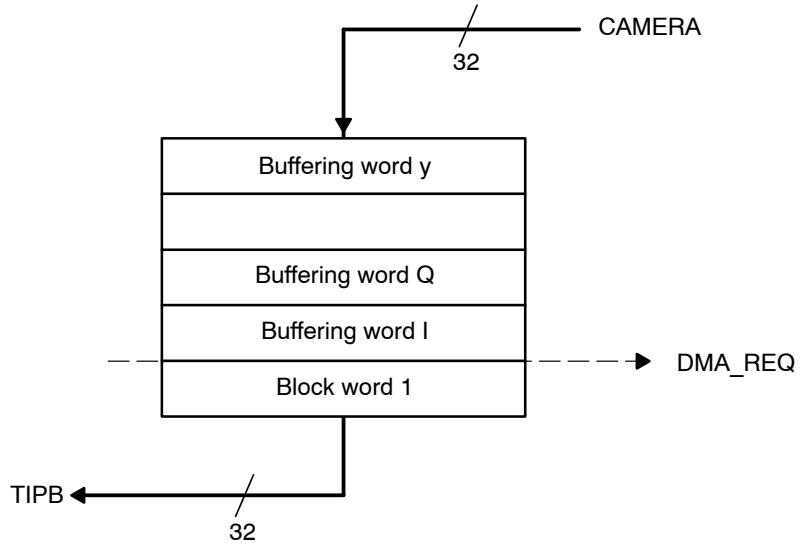


Figure 7. FIFO-Buffer Parts



When the threshold value is set to 0, the interrupt is generated immediately. This is the equivalent of the threshold always being exceeded regardless of whether or not any data is present in the FIFO.

1.1.6 Clock Divider

The clock divider inputs the internal 12-MHz clock source or the 48-MHz source from either the ULPD_DPLL or ULPD_APLL to generate the external clock CAM.EXCLK. The division factor is programmable in the clock-control register through FOSCMOD (see Table 1).

Table 1. Clock Ratios

Ratio	CAM.EXCLK	
	From 12 MHz	From 48 MHz
1	12 MHz	–
1/2	6 MHz	24 MHz
1/5	–	9.6 MHz
1/6	–	8 MHz

A request is automatically generated to wake up the DPLL when the 48 MHz signal is needed. The switch is performed when the 48-MHz signal is stable.

The CAM.EXCLK needs to be disabled before switching the clock source.

The clock divider also allows disabling the external clock by setting the CAMEXCLK_EN bit.

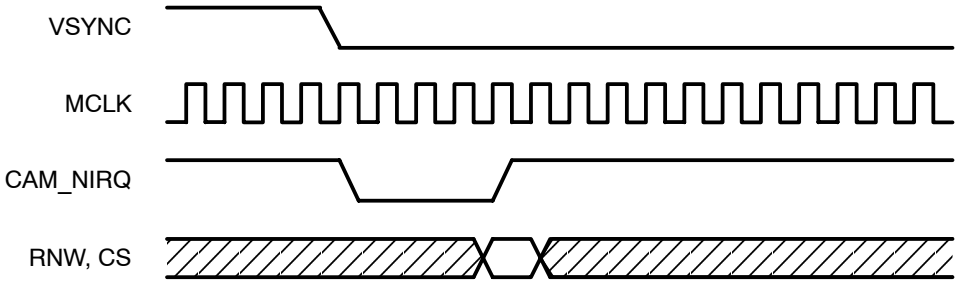
1.1.7 Interrupt Generator

The following sources can generate an MPU interrupt.

- ❏ Data transfer interrupt. (An interrupt is generated per word received.)
- ❏ HSYNC rising edge (start of line)
- ❏ HSYNC falling edge (end of line)
- ❏ VSYNC rising edge (start of frame)
- ❏ VSYNC falling edge (end of frame)
- ❏ FIFO overflow

Each of the interrupt sources can be masked individually. The interrupt source can be determined by reading the Interrupt-Source-Status Register (IT_STATUS). Reading this register automatically clears the register value and the interrupt signal.

Figure 8. IRQ Generated on VSYNC Falling Edge



1.1.8 DMA Procedure

Below is a sample procedure to input camera data with the following conditions.

Frame size = 352 x 288 (CIF size)

Bits per Pixel = 16

FIFO Trigger Level = 64

System DMA Length = 128 words (64 x 32 bit)

1) Configure the camera modules and the System DMA Channel.
2) A rising edge of the CAM.VS results in the camera-interface module starting to input the data.
3) A high level of the CAM.HS and a proper CAM.LCLK starts the first data transfer. After the first two pixels of data are received (8 bits x 4 transfers = 32 bits), the data is stored in the FIFO.
4) When the FIFO write-pointer reaches the trigger level, a DMA request is issued.
5) After 396 (352 x 288 / 4 / 64) DMA transfers, the DMA controller generates an MPU interrupt to indicate to the MPU the completion of the frame transfer.

Note:

The DMA transfer size is recommended to be the same size as the threshold. Autostart frees the MPU to watch for a rising edge on VSYNC.

1.1.9 TIPB Registers

The camera-interface module contains seven registers for communication between the TIPB and camera module. They mainly control clock generation, interrupt requests, and status register (see Section 1.1.10).

The address of each register is the starting address (FFFB:6800) plus the offset indicated in Table 3.

Table 2 shows the default configuration of several critical register fields at reset. See Table 4 through Table 10 for full descriptions of these register fields.

Table 2. Default Configuration at Reset

Item	Function
ORDERCAMD	Not swapped
MASK	Interrupts on VSYNC and HSYNC disabled
FOSCMOD	Division rate for CAM.EXCLK = 1 (12 MHz)
POLCLK	Data latched on rising edge of CAM.LCLK
CAMEXCLK_EN	CAM.EXCLK disabled
MCLK_EN	Internal clock disabled
DPLL_EN	DPLL clock source disabled
THRESHOLD	Trigger level = 1 word

1.1.10 Camera-Interface Registers (FFFB:6800)

Because the TIPB register read accesses are resynchronized to the camera interface clock, the MCLK_EN bit must first be set before any camera-interface registers access. Table 3 lists the camera-interface registers. Table 4 through Table 10 describe the individual registers.

Table 3. Camera-Interface Registers

Register	Description	R/W	Size	Offset Address
CTRLCLOCK	Clock control	R/W	32 bits	0x00
IT_STATUS	Interrupt source status	R	32 bits	0x04
MODE	Camera-interface mode configuration	R/W	32 bits	0x08
STATUS	Status	R	32 bits	0x0C
CAMDATA	Image data	R	32 bits	0x10
GPIO	Control the CAM.RSTZ pin to reset an external camera module.	R/W	32 bits	0x14
PEAK_COUNTER	FIFO peak counter	R/W	32 bits	0x18

Before changing the clock source, disable the 12MHz clock of the camera-interface module by clearing the MCLK_EN field. The clock can also be disabled to save power.

Before clearing the PEAK_COUNTER, read all of the data in the FIFO. The PEAK_COUNTER is updated when the FIFO write-pointer exceeds the PEAK_COUNTER value. Thus, the PEAK_COUNTER contains the peak number for data remaining in the FIFO.

Table 4. Clock-Control Register (CTRLCLOCK)

Bits	Field	Value	Description	R/W	Reset Value
31–8	RESERVED		This field is reserved (unknown value after reset).	R/W	0xX
7	LCLK_EN	0	Disables	R/W	0x0
		1	Enables incoming CAM.LCLK		
6	DPLL_EN	0	Disables	R/W	0x0
		1	Enables the DPLL source (48 MHz)		

Table 4. Clock-Control Register (CTRLCLOCK) (Continued)

Bits	Field	Value	Description	R/W	Reset Value
5	MCLK_EN	0	Disables	R/W	0x0
		1	Enables internal clock of interface		
4	CAMEXCLK_EN	0	Disables	R/W	0x0
		1	Enables the CAM.EXCLK		
3	POLCLK		Sets polarity of the CAM.LCLK	R/W	0x0
		0	Data latched on the rising edge		
		1	Data latched on the falling edge		
2–0	FOSCMOD		Sets the frequency of the CAM.EXCLK clock	R/W	0x00
		000	12 MHz		
		010	6 MHz		
		100	9.6 MHz (48 MHz/5)		
		101	24 MHz (48 MHz/2)		
		110	8 MHz (48 MHz/6)		

Table 5. Interrupt-Source-Status Register (IT_STATUS)

Bits	Field	Description	Type	Reset Value
31–6	RESERVED	Reserved bits	R–R	0xX
5	DATA_TRANSFER	Data transfer status. Set to 1 when the trigger is reached.	R–R	0x0
4	FIFO_FULL	Detect the rising edge on the FIFO-full flag.	R–R	0x0
3	H_DOWN	Flag for the horizontal synchronous falling edge occurred.	R–R	0x0
2	H_UP	Flag for the horizontal synchronous rising edge occurred.	R–R	0x0
1	V_DOWN	Flag for the vertical synchronous falling edge occurred.	R–R	0x0
0	V_UP	Flag for the vertical synchronous rising edge occurred.	R–R	0x0

Table 6. Camera-Interface-Mode-Configuration Register (MODE)

Bits	Field	Value	Description	R/W	Reset Value
31–19	RESERVED		Reserved bits	R/W	0xX
18	RAZ_FIFO		1 Clears data in the FIFO; reinitializes read and write pointers; clears the FIFO-full interrupt, the FIFO peak counter; and resynchronizes.	R/W	0x0
17	EN_FIFO_FULL	0	Disables	R/W	0x0
		1	Enables an interrupt on FIFO_FULL		
16	EN_NIRQ	0	Disables	R/W	0x0
		1	Enables the data transfer interrupt (bypass DMA mode)		
15–9	THRESHOLD		Programmable DMA request trigger value; the DMA request is made when the FIFO counter is equal to the threshold value. Currently, set this field to 1 in the DMA mode.	R/W	0x0000001
8	DMA	0	Disables	R/W	0x0
		1	Enables the DMA mode		
7	EN_H_DOWN	0	Disables	R/W	0x0
		1	Enables an interrupt on the HSYNC falling edge.		
6	EN_H_UP	0	Disables	R/W	0x0
		1	Enables an interrupt on the HSYNC rising edge.		
5	EN_V_DOWN	0	Disables	R/W	0x0
		1	Enables an interrupt on the VSYNC falling edge.		
4	EN_V_UP	0	Disables	R/W	0x0
		1	Enables an interrupt on the VSYNC rising edge.		

Table 6. Camera-Interface-Mode-Configuration Register (MODE) (Continued)

Bits	Field	Value	Description	R/W	Reset Value
3	ORDERCAMD		Sets order of 2 consecutive bytes received from the camera (YUV format).	R/W	0x0
		0	Not swapped		
		1	Swapped		
2–0	RESERVED		Reserved bits	R/W	0x00

Table 7. Status Register (STATUS)

Bits	Field	Description	R/W	Reset Value
31–2	RESERVED	Reserved bits	R	0xX
1	HSTATUS	CAM.HS status (edge detection)	R	0x0
0	VSTATUS	CAM.VS status (edge detection)	R	0x0

Table 8. Camera-Interface-GPIO Register (GPIO)

Bits	Field	Description	R/W	Reset Value
31–1	RESERVED	Reserved bits	R/W	0xX
0	CAM.RST	Control the CAM.RST pin status. This pin can be used as the reset signal for the external camera module.	R/W	0x0

Table 9. Image-Data Register (CAMDATA)

Bits	Field	Description	R/W	Reset Value
31–0	CAMDATA	Image data from the FIFO	R	0x0

Table 10. FIFO-Peak-Counter Register (PEAK_COUNTER)

Bits	Field	Description	R/W	Reset Value
31–7	RESERVED	Reserved	R/W	Unknown
6–0	PEAK_COUNTER	Keeps the maximum number of 32-bit words written to the FIFO during a transfer.	R/W	0x0000000

1.2 Clock-Switching Procedures

1.2.1 CAM.EXCLK Switch Protocol

Before changing the CAM.EXCLK configuration, both the 12MHz and the DPLL clock sources must be disabled as shown in the following procedure.

1) Disable the MCLK and DPLL_CLK (MCLK_EN = 0, DPLL_EN = 0, FOSCMOD = FOSCMOD).
2) Change the CAM.EXCLK value (FOSCMOD = new FOSCMOD).
3) Enable the MCLK and DPLL_CLK (MCLK_EN = 1, DPLL_EN = 1, FOSCMOD = FOSCMOD).

1.2.2 CAM.LCLK Switch Protocol

Bit 3 of the clock-control register (POLCLK) sets the polarity of the CAM.LCLK. The CAM.LCLK must be disabled before selecting the rising or the falling edge.

1) Disable the CAM.LCLK (LCLK_EN = 0).
2) Set the new polarity (POLCLK = 1 or 0).
3) Enable the CAM.LCLK (LCLK_EN = 1).

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