OMAP5912OSK
Target Module
Hardware Reference Guide

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Preface

Read This First

About This Manual

This document discusses the design of the OMAP5912 target module used in the OMAP5912 Starter Kit (OSK). It details the design of each aspect of the target module. Sufficient detail is provided to show how each component interacts and what functions they perform. Additional information is found in the individual component datasheets.

The OMAP5912 target module is the processor module for the OMAP5912OSK. It provides a means to evaluate the OMAP5912 processor by allowing you to work with the ARM, DAP, and peripherals of the OMAP5912.

How to Use This Manual

The sections that make up this design specification include:

- ❏ Target module requirements
- ❏ Detailed design
- ❏ Expansion connectors
- ❏ I/O connectors
- ❏ Mechanical specifications

Notational Conventions

This document uses the following acronyms:

Acronym	Definition
CFC	Compact Flash Controller
DDR	Dual Data Rate
Flash	Nonvolatile memory
JTAG	Joint Test Access Group
OTC	OMAP Technology Center
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
USB	Universal Serial Bus

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Related Documentation From Texas Instruments

The following books describe the OMAP devices and related support tools. To obtain a copy of any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477−8924. When ordering, please identify the book by its title and literature number.

OMAP5912 Applications Processor (literature number SPRS231) data sheet contains the electrical and timing specifications for the OMAP5912™ device, as well as signal descriptions for all of the available packages.

TPS65010: Power and Battery Management IC for Li-Ion Powered Systems (literature number SLVS149) data sheet contains the electrical and timing specifications for the TPS65010™ device.

Documentation that describes the OMAP5912 device, related peripherals, and other technical collateral, is available in the OMAP5912 Product Folder on TI's website: www.ti.com/omap5912.

Related Documentation

256M bits DDR Mobile RAM EDK2516CBBH(16M words x 16 bits) (Document No. E0300E70) data sheet, Elpida Memory, Inc., published October 2003 (K) Japan Ver 7.0

8Mx16 Mobile SDRAM 54CSP (K4M28163PD-R(B)G/S) data sheet, Samsung Electronics, published December 2002 Revision 1.3

Universal Serial Bus Specification Revision 2.0 Compaq Computer Corporation, Hewlett−Packard Development Company, Intel Corporation, Lucent Technologies, Microsoft Corporation, NEC Corporation, Philips Electronics, Revision 2.0 April 27, 2000

Open HCI—Open Host Controller Interface Specification for USB*,* Compaq Computer Corporation, Release 1.0a October 1996

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Contents

Figures

Tables

Chapter 1

OMAP5912 Target Module Major Components

The following sections provide a detailed description of the design of the major components of the OMAP5912™ target module.

Topic **Page**

1.1 OMAP5912 Target Module Summary

Table 1−1 lists the major components for the OMAP5912 target module.

Table 1−1. OMAP5912 Target Module Components

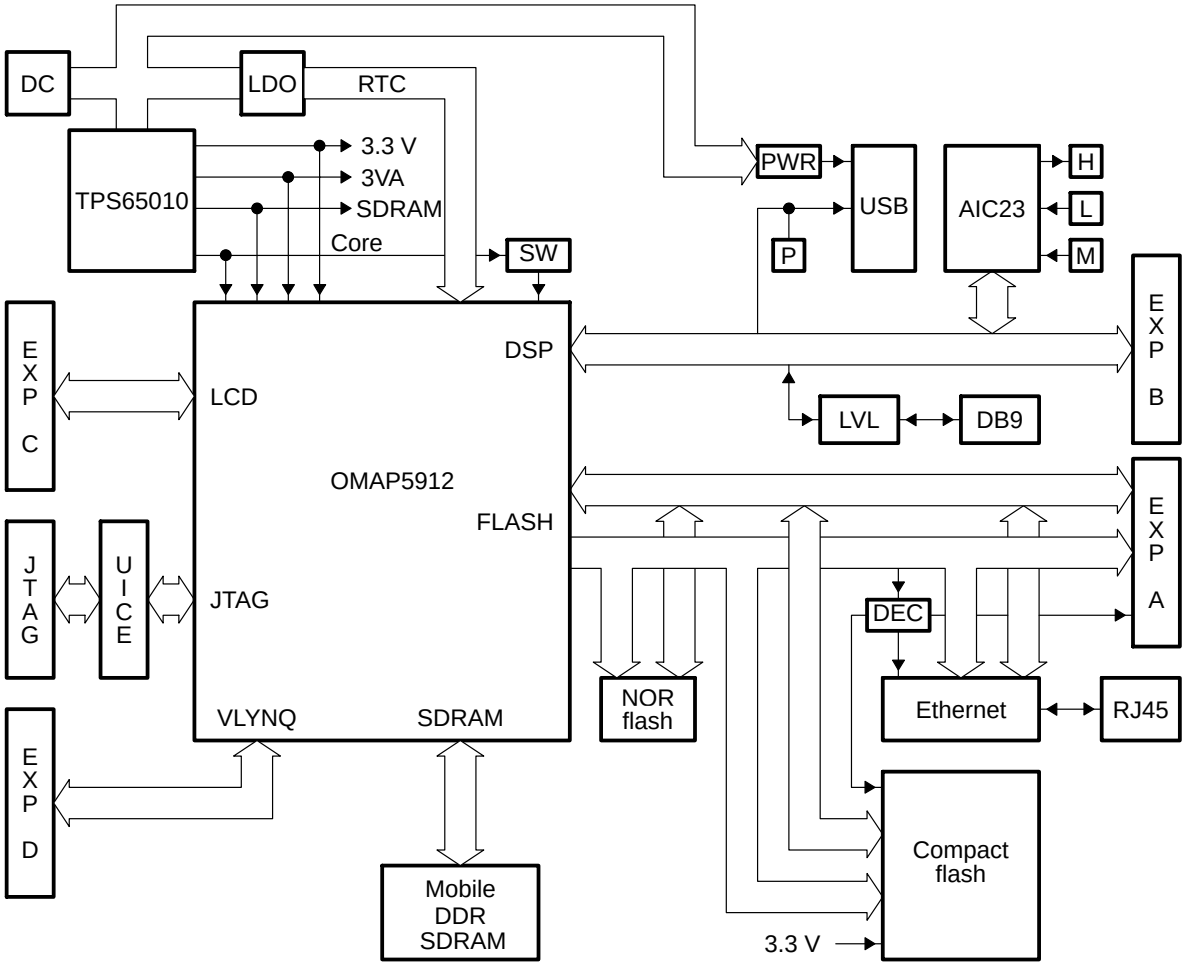
Component	Description	Comments
	Processor	
OMAP5912	GDY Package	1.0mm pitch
	SDRAM	
32MB	Mobile DDR	1.8V Only
	FLASH	
NOR Strata	32MB	Expandable to 64MB
	Power Management	
DC Input	DC Jack	Wall supply, 5V,3W, Regulated
Status LEDs	Power good	User defined
Low Power Option		
Power on reset		
MPU Reset	Via switch	
	Audio CODEC	
Audio CODEC	AIC23	
Line-In	3.5mm Jack	
Headphone Out	3.5mm Jack	
MIC In	3.5mm Jack	
	Serial Ports	
RS232	DB9 Male	Tx, Rx
USB Host	250ma power	USB Type B
Ethernet	10Mb	RJ45, status LEDs
	Expansion	
Compact Flash	Type I and Type II	Use integrated controller
Expansion Connectors	All signals except SDRAM	Support Expansion Cards

Table 1−1. OMAP5912 Target Module Components (Continued)

Component	Description	Comments
	Debugging	
JTAG	14 Pin	
Multi-ICE	20 Pin	TRST polarity jumper
	Form Factor	
Small as practical	Stackable	

Figure 1−1 is the high level block diagram of the OMAP5912 target module design.

Figure 1−1. OMAP5912 Target Module Block Diagram



1.2 Memory Map

The memory map of the OMAP5912 target module contains Flash bus and SDRAM memory.

1.2.1 Flash Memory Bus Memory Map

Table 1−2 defines the Flash bus or EMIFS (Expansion Memory Interface Slow) memory map. The Compact Flash interface has an option in the design to move the address space to the chip select (CS) CS2 region. This is the default location. Refer to section 1.8, Compact Flash, for more detail.

Table 1−2. Flash Bus Memory Map

CS	Type	Start	End	Bytes	
CS1A	Not Used	0400 2000	047F FFFF	8M	Can be used on an expansion board.
	Ethernet	0480 0000	04FF FFFF	8M	
	Not Used	0500 0000	057F FFFF	8M	Can be used on an expansion board.
	Not Used	0580 0000	05FF FFFF	8M	Can be used on an expansion board.
CS1B	Not Used	0600 0000	07FF FFFF	32M	Can be used on an expansion board.
CS2	Compact Flash Memory	0800 0000	0800 07FF	2K	When Compact Flash space is used, CS2 cannot be used for any other memory.
	Compact Flash Attrib	0800 0800	0800 0FFF	2K	When Compact Flash space is used, CS2 cannot be used for any other memory.
	CF I/O	0800 1000	0800 17FF	2K	When Compact Flash space is used, CS2 cannot be used for any other memory.
CS3	Flash Memory	0C00 0000	0FFF FFFF	64M	Can be used on an expansion board.

The flash memory in the CS3 region has four possible configurations as shown in Table 1−3.

Table 1−3. Flash Memory Map Configurations

(a) 4 MB Mode, Supports 2 4 MB Memory Parts, 8 MB Total

CS	Type	Start	End	Bytes	
CS3	FLASH Slot 1	0C00 0000	0C3F FFFF	4M	Can be used on an expansion board via FLASH.DIS pin.
	FLASH Slot 2	0C40 0000	0C7F FFFF	4M	Can be used on an expansion board via FLASH.DIS pin.
	Not Used	0C80 0000	0FFF FFFF	56M	Can be used on an expansion board.

(b) 8 MB Mode, Supports 2 8 MB Memory Parts, 16 MB Total

CS	Type	Start	End	Bytes	
CS3	FLASH Slot 1	0C00 0000	0C7F FFFF	8M	Can be used on an expansion board via FLASH.DIS pin.
	FLASH Slot 2	0C80 0000	0CF8F FFFF	8M	Can be used on an expansion board via FLASH.DIS pin.
	Not Used	0CD0 0000	0FFF FFFF	48M	Can be used on an expansion board.

(c) 16 MB Mode, Supports 2 16 MB Memory Parts, 32 MB Total Default Mode

CS	Type	Start	End	Bytes	
CS3	FLASH Slot 1	0C000 0000	0CFF FFFF	16M	Can be used on an expansion board via FLASH.DIS pin.
	FLASH Slot 2	0D00 0000	0DFF FFFF	16M	Can be used on an expansion board via FLASH.DIS pin.
	Not Used	0E00 0000	0FFF FFFF	32M	Can be used on an expansion board.

(d) 32 MB Mode, Supports 2 32 MB Memory Parts, 64 MB Total

CS	Type	Start	End	Bytes	
CS3	FLASH Slot 1	0C000 0000	0DFF FFFF	32M	Can be used on an expansion board via FLASH.DIS pin.
	FLASH Slot 2	0E00 0000	0FFF FFFF	32M	Can be used on an expansion board via FLASH.DIS pin.

The OMAP5912 target module supports multiple configurations of NOR FLASH that can be loaded with various devices to create the different configurations. For more information on the different configurations refer to section 1.5, *Flash Memory*.

1.2.2 SDRAM Memory Map

A single mobile DDR (Double Data Rate) SDRAM (Synchromous Dynamic Random Access Memory) device is provided on the OMAP5912 target module. Table 1−4 defines the memory map for the DDR SDRAM. The 32MB configuration is the default mode.

Table 1−4. SDRAM Memory MAP

Mode	Start	End	Bytes	
32MB	1000 0000	11FF FFFF	32M	Default configuration
64MB	1000 0000	13FF FFFF	64M	To change the DDR configuration, the part on the OMAP5912 target module must be replaced.
Reserved	1800 0000	18FF FFFF		

1.3 OMAP5912 Processor

This section covers the part of the design that is specific to the OMAP5912 processor. The following components are discussed in this section:

- OMAP™ processor
- Clock interface
- Reset circuitry
- Power connections
- Configuration pins

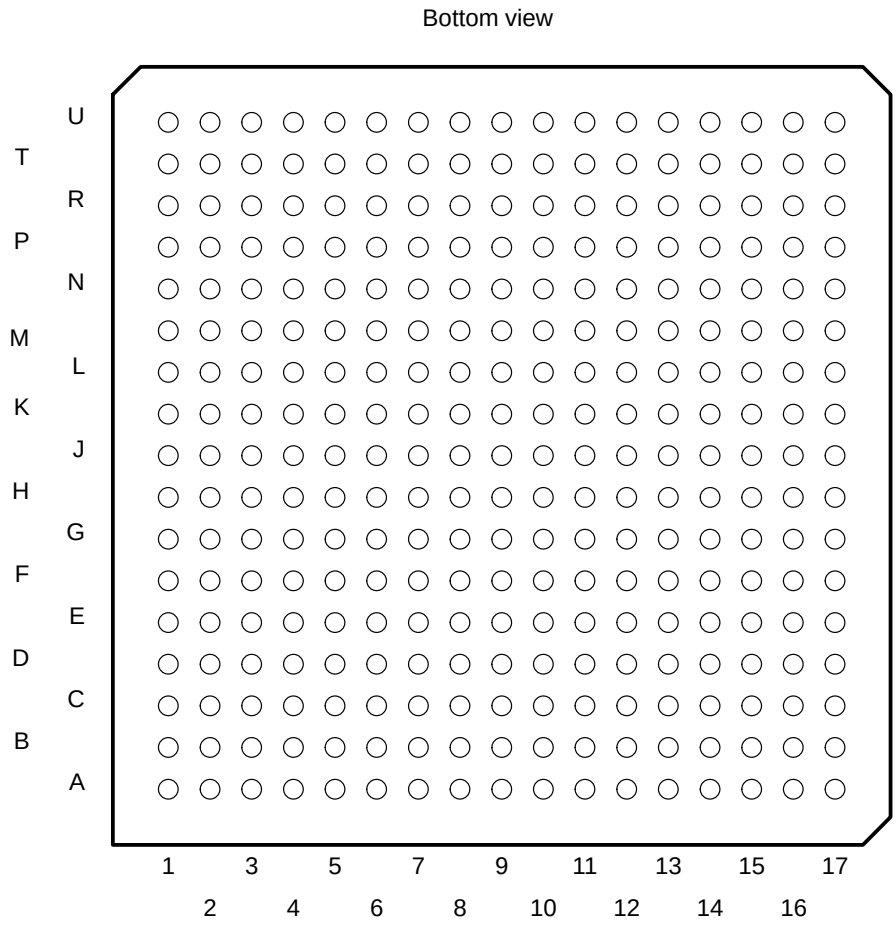
1.3.1 OMAP5912 Processor

There are two different packages available for the OMAP5912:

- ZDY Plastic BGA
- ZZG Plastic BGA

The ZDY and ZZG packages are 289-pin devices. The ZZG package is a much smaller package and has a finer pitch. The OMAP5912 target module uses the ZDY package. Figure 1−2 shows the pinout of the ZDY package.

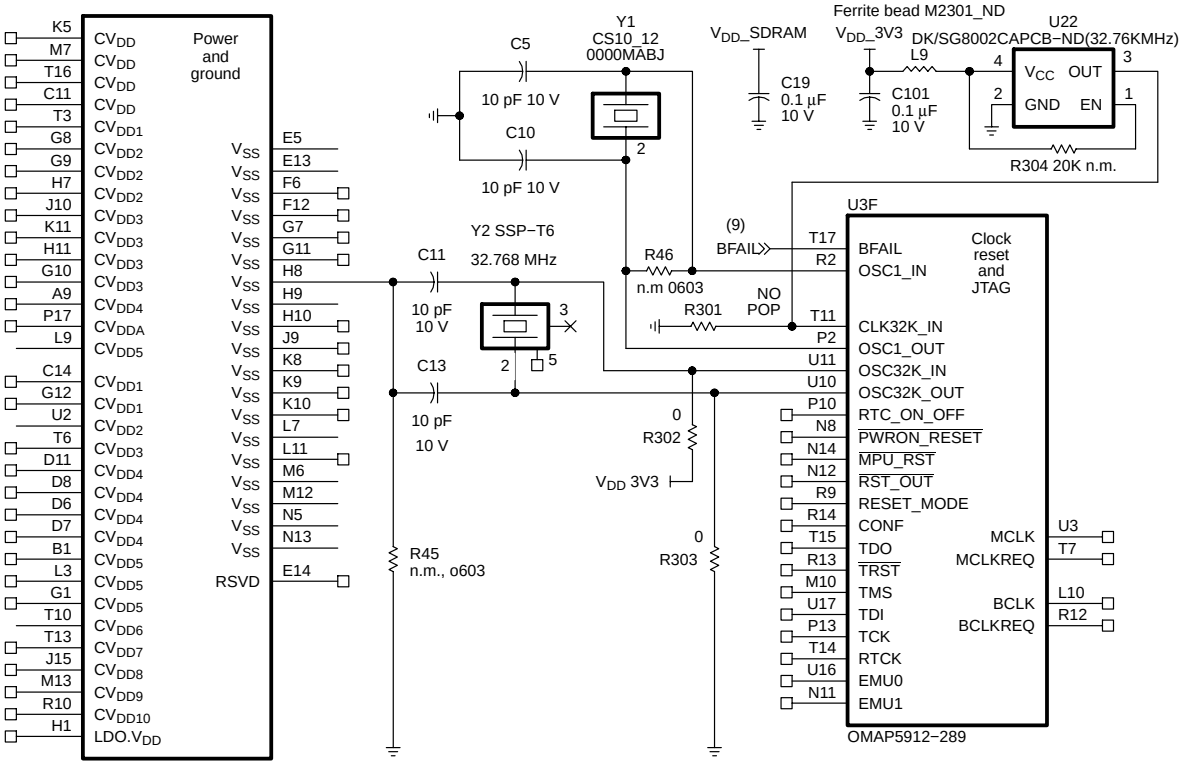
Figure 1−2. OMAP5912 Clock Inputs



1.3.2 Clock Interface

Figure 1−3 shows the design of the crystals for the OMAP5912 target module.

Figure 1−3. OMAP5912 Clock Inputs



The 32 KHZ clock has two options provided on the board, crystal or external oscillator. The build of the OMAP5912 target module uses the external oscillator.

1.3.2.1 Crystal Configuration

In the crystal configuration for the 32KHZ clock, an external crystal, Y2, is used for the clock source. The crystal is connected across pins U10 and U11. Because the crystal is used, pin T11 must be grounded. Capacitors C11 and C13 terminate the crystal to ground. These capacitors must be connected directly to pin H8 of the OMAP5912, which is internally connected to ground. The length of this connection should be kept as short as possible. As an option, R45 can provide a direct connection to ground, if needed. It is not needed under the current design.

In this configuration, the following components are *not* to be installed:

- ❏ C101
- ❏ L9
- ❏ U22
- ❏ R304
- ❏ R302
- ❏ R303

1.3.2.2 Oscillator Configuration

In the oscillator configuration, U22 provides the 32KHZ clock. L9 and C101 provide filtering into the power rail of the oscillator. R304 provides a pull up to the enable pin of the oscillator. R302 and R303 provide the termination of the crystal pins on the OMAP5912 as required when using the external oscillator.

In this configuration, the following components are *not* installed:

- ❏ C11
- ❏ C13
- ❏ Y2
- ❏ R301

1.3.2.3 12 MHZ Clock

Crystal Y1 provides the 12MHZ function for the OMAP5912. Capacitors C5 and C10 provide termination for Y1. An external oscillator can be used for the 12MHZ clock. This option is not supported in the OMAP5912 target module design.

In addition, you can use a 13MHZ crystal in place off the 12MHZ crystal. The OMAP5912 target module is not supplied with a 13MHZ crystal. However, you can replace the 12MHZ crystal if needed for your application.

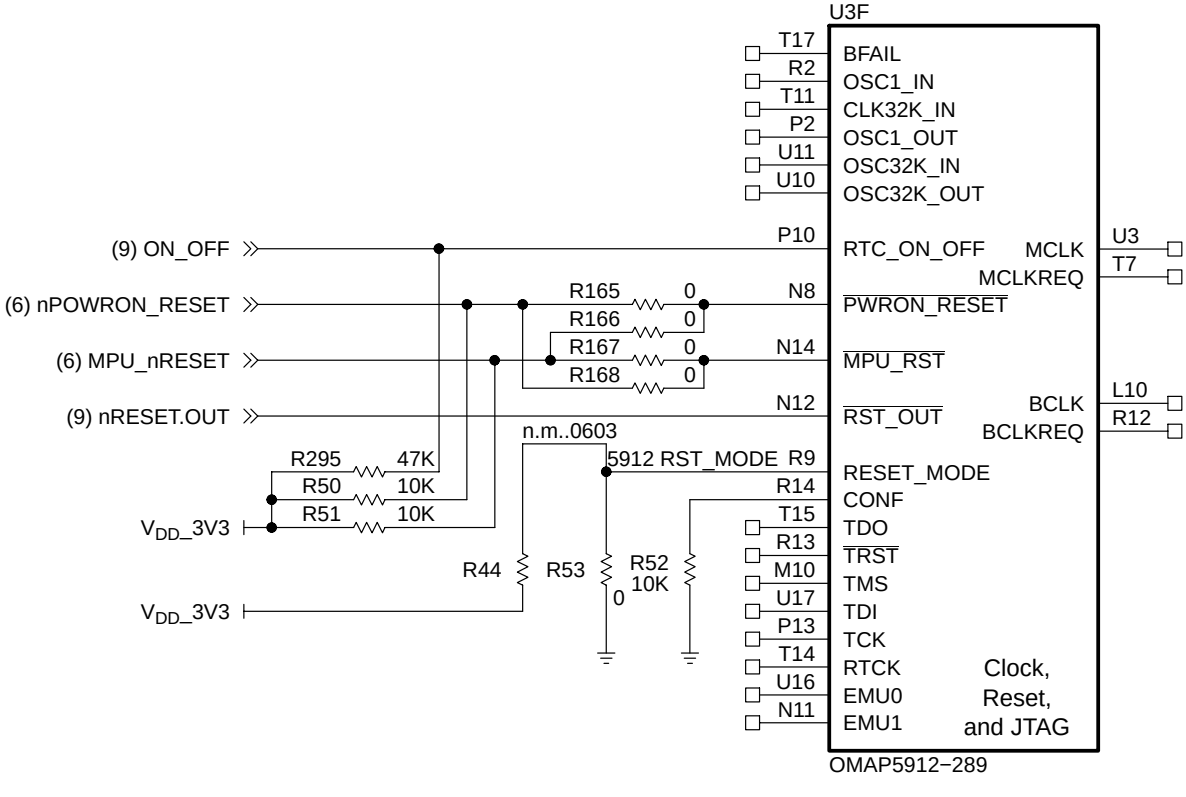
1.3.3 Reset Interface

Figure 1−4 defines the use of the three pins that make up the reset functions on the OMAP5912.

The nPWRON_RESET is an input to the OMAP5912 that, when taken low, resets the entire OMAP5912.

The MPU_RESET signal is an input to the OMAP5912 that when taken low, resets the ARM core on the OMAP5912.

Figure 1−4. OMAP5912 Reset Interface



There are four resistors on the module, which based on the way they are loaded, provide several options to configure the reset signals. The reset signals for the **nPWRON_RESET** and the **nMPU_Reset** are generated by the TPS65010™ power management device. Both of these signals are open drain outputs. For more information, refer to section 1.4.3, *TPS65010*.

Both the nPWRON_RESET and nMPU_RESET signals are needed to generate an nPWRON_RESET signal into the OMAP5912. The reset switch on the TPS65010 only generates as nMPU_RST. Because only the nPWRON_RESET signal on the OMAP5912 is used, you need to make sure that both resets from the TPS65010 generate only the nPWRON_RESET signal. This is done by loading the resistors as follows:

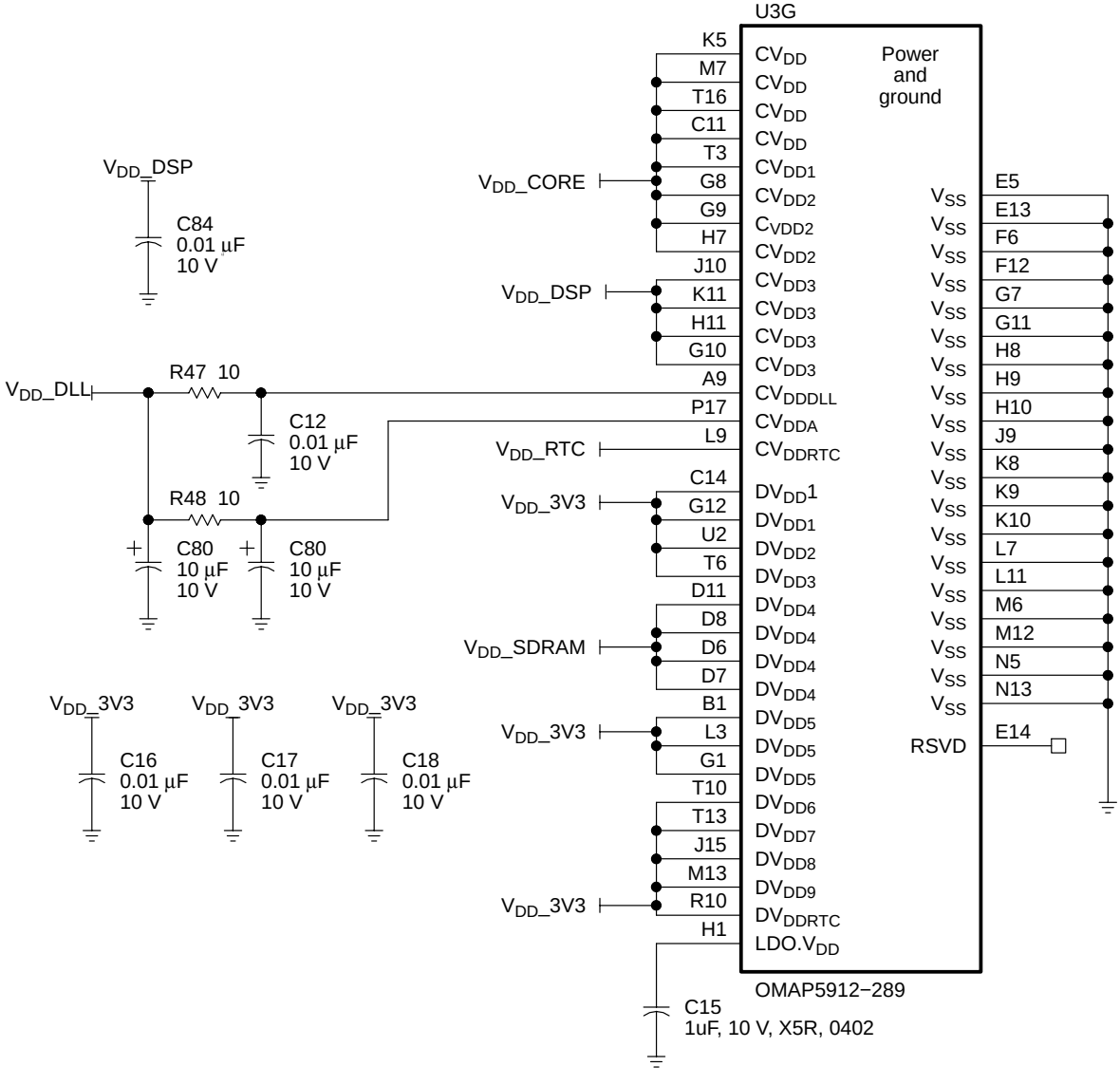
- R165, connecting nPWRON_RESET to nPWRON_RESET of the OMAP5912
- R166, connecting nMPU_RST to the nPWRON_RESET of the OMAP5912.
- R167 and R168 are not installed.

This allows both reset signals from the TPS65010 to generate only an nPWRON_RESET into the OMAP5912.

1.3.4 Power Connections

Figure 1−5 shows the power connections on the OMAP5912 processor. Each of these is discussed in the following paragraphs.

Figure 1−5. OMAP5912 Power Connections



The V_{DD_DLL} power on the OMAP5912 can be sensitive to noise. Therefore, two RC circuits are used to provide enhanced noise immunity. R47 and C12 provide a filter for the CV_{DDLL} pin, which is the core voltage supply pin for the DLL. R48 and C14 perform the same function for the CV_{DDA} pin, which provides the power to the DLL itself. Capacitor C80 provides low frequency filtering for the DLL supply. Power for the DLL is supplied by a separate LDO, U5. For information, refer to section 1.4, *Power Management*.

V_{DD_CORE} is the main supply to the internal core voltages of the OMAP5912 and is a nominal 1.6 V but can be set to 1.1 V−1.5 V under software control through the TPS65010. Refer to section 1.4, *Power Management*, for more details. Filtering of the voltage is supplied by the bypass and filter capacitors.

V_{DD_DSP} is the supply pin for the DSP in the OMAP5912. Power for the DSP is supplied through U11. U11 should be placed as close as possible to the OMAP5912 in the layout process. U11 can be disabled by taking GPIO4 of the TPS65010 low.

V_{DD_RTC} supplies power to the Real Time Clock inside the OMAP5912. Power is supplied by U9. Refer to section 1.4.9, *Real Time Clock Power*, for a more detailed description.

V_{DD_3V3} is the 3.3 V supply for the OMAP5912. This supplies power to the various I/O function pins as well as the FLASH bus.

V_{DD_SDRAM} supplies voltage to the output pins for the SDRAM interface.

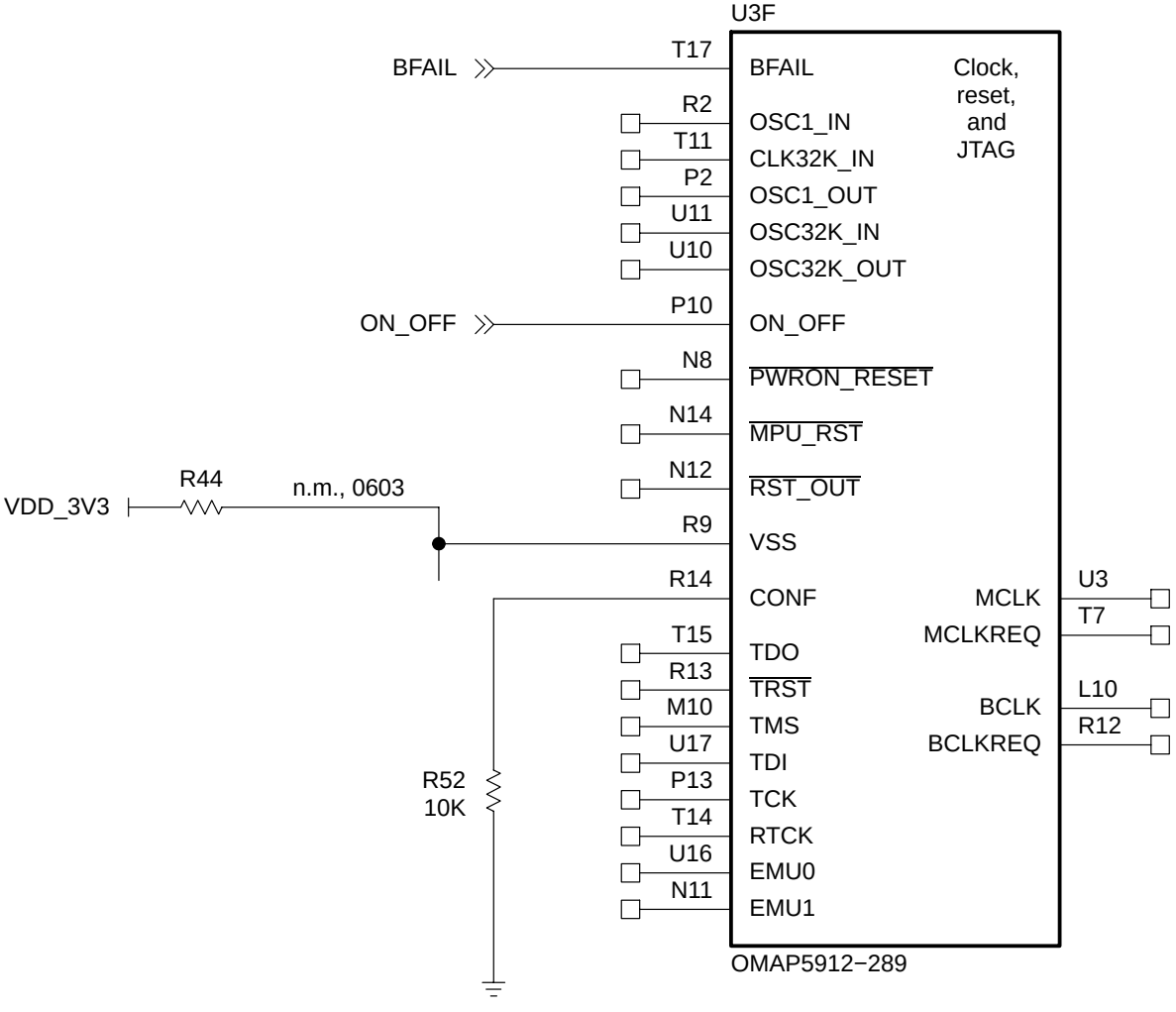
Pin H1 on the OMAP5912 processor is the output of a regulated supply that is delivered by an embedded LDO to the DPLL macros. The regulated supply is available on the OMAP5912 at pad H1. A decoupling capacitor of 1 µF must be connected externally between LDO.FILTER and ground.

All power is connected to a common ground. All leads from the ground pins on the OMAP5912 to the actual ground plane are kept as short as practical.

1.3.5 Configuration Pins

There are a group of pins that are used to configure the OMAP5912 processor based on each individual application. Figure 1−6 shows these pins.

Figure 1−6. OMAP5912 Configuration Pins



BFAIL is the battery power failure and external FIQ interrupt input. BFAIL can be used to gate certain input pins when battery power is low or failing. The pins that can be gated are configured via software. This pin can also optionally be used as an external FIQ interrupt source to the MPU. The function of this pin is configurable through software.

On the OMAP5912 target module, this pin connects to pin 54 of Expansion Connector B. It is not used by any circuitry on the OMAP5912 target module and is free to be used by an expansion card.

ON_OFF controls the internal RTC. When pulled low, the RTC is disabled. A resistor insures that the RTC is enabled by pulling the pin to V_{DD_RTC}. This pin also connects to pin 56 of Expansion Connector B for use by the expansion cards as needed either as a way to disable the internal RTC or to be used as one of its optional features. Refer to the *OMAP5912 Application Processor* data sheet (literature number SPRS231) for more detail on how the pin can be used.

CONF must be tied low through a 10K Ω resistor to put the OMP5912 in the operational mode. Pulling this pin high puts the device in the test mode. The test mode is not used on the OMAP5912 target module design.

1.4 Power Management

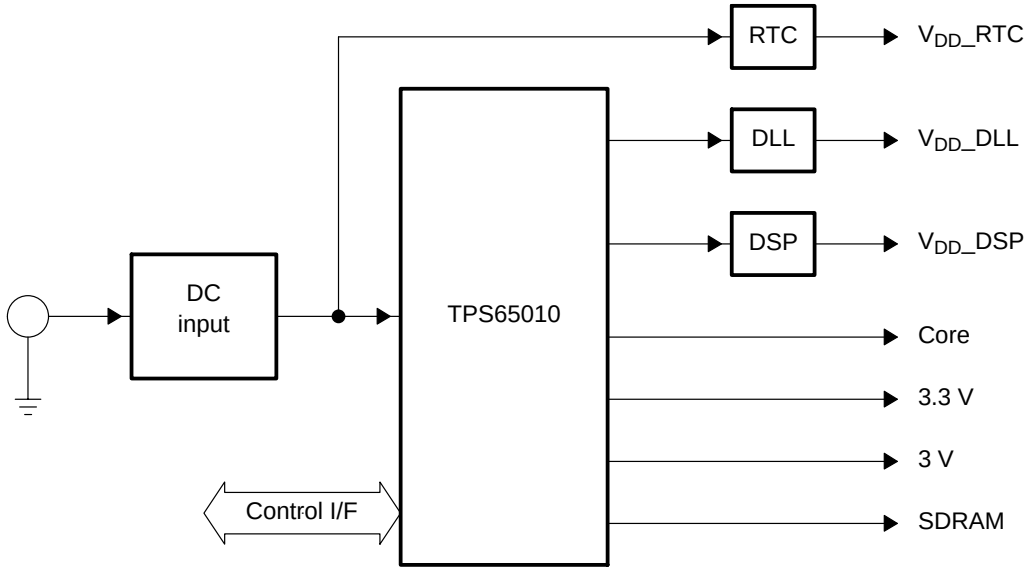
This section covers the design of the power management circuitry for the OMAP5912 target module. Covered in this section are these components:

- ❑ Block diagram
- ❑ Power budgets
- ❑ TPS65010
- ❑ DC input
- ❑ SDRAM voltage
- ❑ V_{DD_3V3} supply
- ❑ V_{DD_3V} supply

1.4.1 Block Diagram

Figure 1−7 is the high level block diagram of the Power Management Circuitry.

Figure 1−7. Power Management Block Diagram



The TPS65010 is the power management device used.

The DC Input block is the interface to the external dc power supply.

The SDRAM rail provides power to the SDRAM device on the board.

The 3.3 V rail is the main power rail to the 3.3 V bus on the board including the FLASH memory devices.

The 3 V rail supplies power to the AIC23 audio CODEC.

The control interface contains the setting of the configuration pins and the I2C interface through which the OMAP51912 communicates to the TPS65010.

The RTC block provides power to the Real Time Clock voltage input of the OMAP5912.

The DLL block provides a separate power rail to the internal DLL power of the OMAP5912.

The DSP block provides the ability to control the power to the DSP block of the OMAP5912.

The Core voltage rail supplies power to the core components in the OAMP5912 processor.

Each of these blocks is discussed in more detail in the following sections.

1.4.2 Power Budget

Table 1−5 defines the estimated power budget for each section of the OMAP5912 target module. The design of the power circuitry is based on these parameters. These are very rough worst case estimates with a lot of head room allowed. Actual power consumption depends on the clock speed and applications that are being run.

Table 1−5. OMAP5912 Target Module Power Budgets

Capacity (Ma)−−−−−−>		**2500**	**400**		**1000**		**200**	**200**	
			CORE	**3V3**	**RTC**	**DLL**	**3 V**	**SDRAM**	
Device	**Voltage**	**DC_IN**	**1.6 V**	**3.3 V**	**1.8 V**	**1.8 V**	**3.0 V**	**1.8 V**	**Comments**
TPS65010(Ma)	VINMAIN	932.3							
TPS65010(Ma)	VINCORE	206							
TPS65010(Ma)	VIN1	23							
TPS65010(Ma)	VIN2	75							
TPS65010(Ma)	AC	500							Only when battery connected
OMAP5912(Ma)			206		5	5			Estimated
OMAP5912(Ma)				85					I/O Voltage
AIC23(Ma)							23		
Flash (2) (Ma)				160					Worst case all Devices

Note: The 3.3 V expansion supply is limited to 125ma and is for running a single expansion card. If more power is needed, the dc input should be used.

Table 1−5. OMAP5912 Target Module Power Budgets (Continued)

Capacity (Ma)−−−−−−>		2500	400		1000		200	200	
			CORE	3V3	RTC	DLL	3 V	SDRAM	
Device	Voltage	DC_IN	1.6 V	3.3 V	1.8 V	1.8 V	3.0 V	1.8 V	Comments
DDR SDRAM(Ma)								75	Estimated
SN74LVC139(Ma)				2					Conservative est.
SN74CBTLV3257(Ma)				0.3					
LEDS (4) (Ma)				40					
LAN91C96(Ma)				64					
AT93C46(Ma)				2					
MAX3221(Ma)				10					Estimated
SN74AHC1G04DCKR(Ma)				10					
SN74LVC244AGQN(Ma)				24					Estimated
Compact Flash(Ma)				400					Limited to 500mA. Spec @ 400ma
Expansion Slot(Ma)		500		125(1)					
USB Host(Ma)		250							Shuts down @ 440ma. Spec @ 250ma
(Ma)	Totals	2486.3	206	922.3	5	5	23	75	
(Ma)	Remaining	13.7	194		67.7		177	125	

Note: The 3.3 V expansion supply is limited to 125ma and is for running a single expansion card. If more power is needed, the dc input should be used.

1.4.3 TPS65010

The TPS65010 is a power management device specifically designed for use with the OMAP family of processors. Its features are:

- ❏ Linear charger management for single Li-Ion Li-Polymer cells
- ❏ Dual input ports for charging from USB or from wall plug; handles 100-mA/500-mA USB requirements
- ❏ Charge current programmable through external resistor
- ❏ 1 A, 95% efficient step-down converter for I/O and peripheral components (VMAIN)

- ❏ 400 mA, 90% efficient step-down converter for processor core (VCORE)
- ❏ 2 × 200-mA LDOs for I/O and peripheral components, LDO enable via bus
- ❏ Serial interface compatible with I2C; supports 100 kHz, 400-kHz operation
- ❏ LOW_PWR pin to lower or disable processor core supply voltage in deep sleep mode
- ❏ 70-µA quiescent current
- ❏ 1% reference voltage
- ❏ Thermal shutdown protection
- ❏ HBM and CDM capabilities of 1 kV at VIB, PG, and LED2 pins

The TPS65010 is an integrated power and battery management integrated circuit (IC) for applications powered by one Li-Ion or Li-Polymer cell, which require multiple power rails. Both step-down converters enter a low power mode at light load for maximum efficiency across the widest possible range of load currents.

The LOW_PWR pin allows the core converter to lower its output voltage when the application processor goes into deep sleep. The TPS65010 also integrates two 200-mA LDO voltage regulators, which are enabled through the serial interface. Each LDO operates with an input voltage range between 1.8 V and 6.5 V, allowing them to be supplied from one of the step-down converters or directly from the battery.

The TPS65010 also has an integrated and flexible Li-Ion linear charger and system power management. It offers integrated ac-adapter supply management with autonomous power-source selection, power FET and current sensor, high accuracy current and voltage regulation, charge status, and charge termination. The USB mode is for the charger and is not used in this particular design. In the ac-adapter configuration an external resistor sets the maximum value of charge current.

The battery is charged in three phases: conditioning, constant current, and constant voltage. Charge is normally terminated based on minimum current. An internal charge timer provides a safety backup for charge termination. The TPS65010 automatically restarts the charge if the battery voltage falls below an internal threshold. The charger automatically enters sleep mode when the dc supply is removed.

Note: Battery Not Supported with OMAP Starter Kit

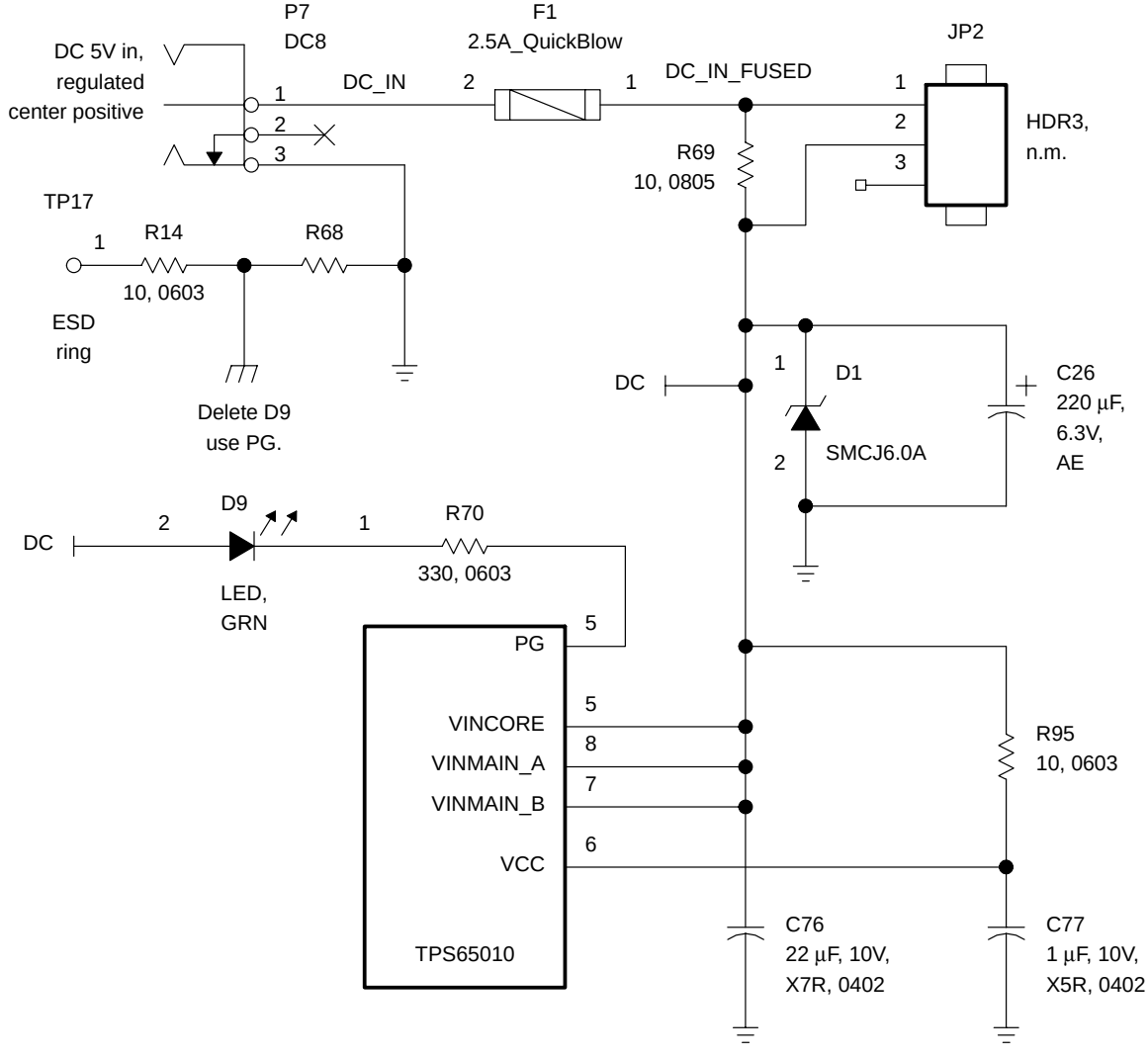
While the battery can be added to the OSK, it is not supported with the OSK. You need to add a battery as needed. For more information, see section 1.4.13, *Battery Mode*.

The serial interface can be used for dynamic voltage scaling, for collecting information on and controlling the battery charger status, for optionally controlling two LED driver outputs, masking interrupts, or for disabling and setting the LDO output voltages. The interface is compatible with the fast/standard mode I2C specification allowing transfers at up to 400 kHz.

1.4.4 Digital Current Input

Figure 1−8 shows the design of the dc input portion of the board.

Figure 1−8. Digital Current Input Design



P7 is the main power jack for the external dc supply. The external supply is specified to be a regulated 5 V. A regulated 5 V is required for the USB interface. In series with the dc input is a 2.5A quick blow fuse in a 1206 package. This fuse is a protection device in the case that the external + 5 V supply does not shut down properly. Diode D1 provides an additional protection function that insures that the input dc voltage cannot get over 6 V. C26 provides filtering of the dc input. C76 is required by the TPS65010 and should be placed as close to the device as possible.

JP2 is an option jumper that is not normally installed. Its purpose is to allow for the selection of either the dc input mode or the battery mode. In the battery mode the battery is used as the main dc input. For details, refer to section 1.4.13, *Battery Mode*. The standard configuration is the loading of the R69, a 1206 sized 0 Ω resistor. You can replace R69 with a .01 Ω or larger resistor to allow for the measurement of the total board current consumption by using an oscilloscope to measure the voltage drop across R69.

D4 is an LED that is connected to the PG (Power Good) output of the TPS65010. This is the main power LED for the OSK. The open-drain PG output indicates when a valid power supply is present for the charger on the ac adapter input. The output turns *on* when a valid voltage is detected. A valid voltage is detected whenever the voltage rises above the voltage on VBAT plus 100 mV. This output is turned off in the sleep mode. The PG output can also be programmed through the LED1_ON and LED1_PER registers in the serial interface of the TPS65010. It can then be programmed to be permanently on, off, or to blink with defined on and off period times. PG is controlled per default through the charger.

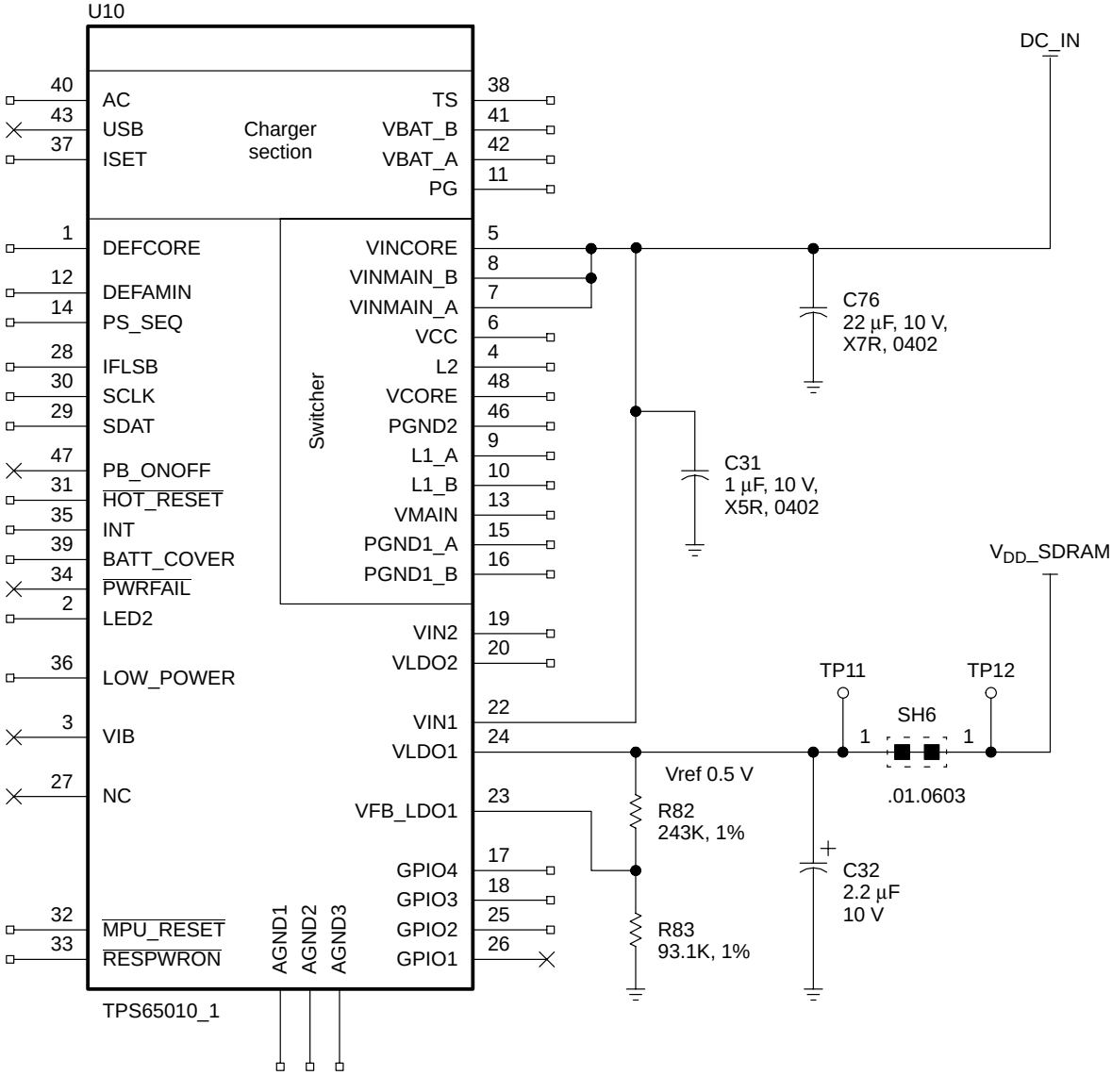
Due to the nature of the TPS65010 design, the main dc input can exhibit noise. For this reason, the V_{CC} input of the TPS65010 must be filtered. This is done through an RC circuit comprised of R95 and C77. The supply current of the V_{CC} rail for the TPS65010 is specified at 50 µA.

There is a single point ground connection. This is the point in which the Frame ground and signal ground connect through R68. This connection is not actually required but is intended to insure that the ground buses stay separated and that the PCB layout software does not try to interconnect the ground planes anywhere other than at this single point. This point should be as close to the dc input ground pin as possible. In addition, there is an ESD ring that goes around the board that also connects to this single point through R111, which is used to lower the current of the discharged voltage.

1.4.5 SDRAM Voltage

The SDRAM voltage bus has a dedicated voltage supply that minimizes noise on the bus. Figure 1−9 covers the portion of the design that comprises the SDRAM voltage supply.

Figure 1−9. SDRAM Power Design



The SDRAM and the OMAP5912 voltage pins use LDO1 of the TPS65010. Resistors R82 and R83 are supplied to allow for the voltage to be offset back into the sense input of the TPS65010. This allows for the voltage to be adjusted for voltage drops experienced by the layout. The default configuration is to set the voltage at 1.8 V, which is done by making R82 a 243K and R83 a 93.1K into the sense input.

LDO1 delivers up to 200 ma. The requirement for the SDRAM is 75 ma. The voltage on LDO1 can be adjusted through software. However, the default setting is external adjust. The optional settings under software control are not used. Refer to the *TPS65010: Power and Battery Management IC for Li-Ion Powered Systems* (literature number SLVS149) data sheet for more detail.

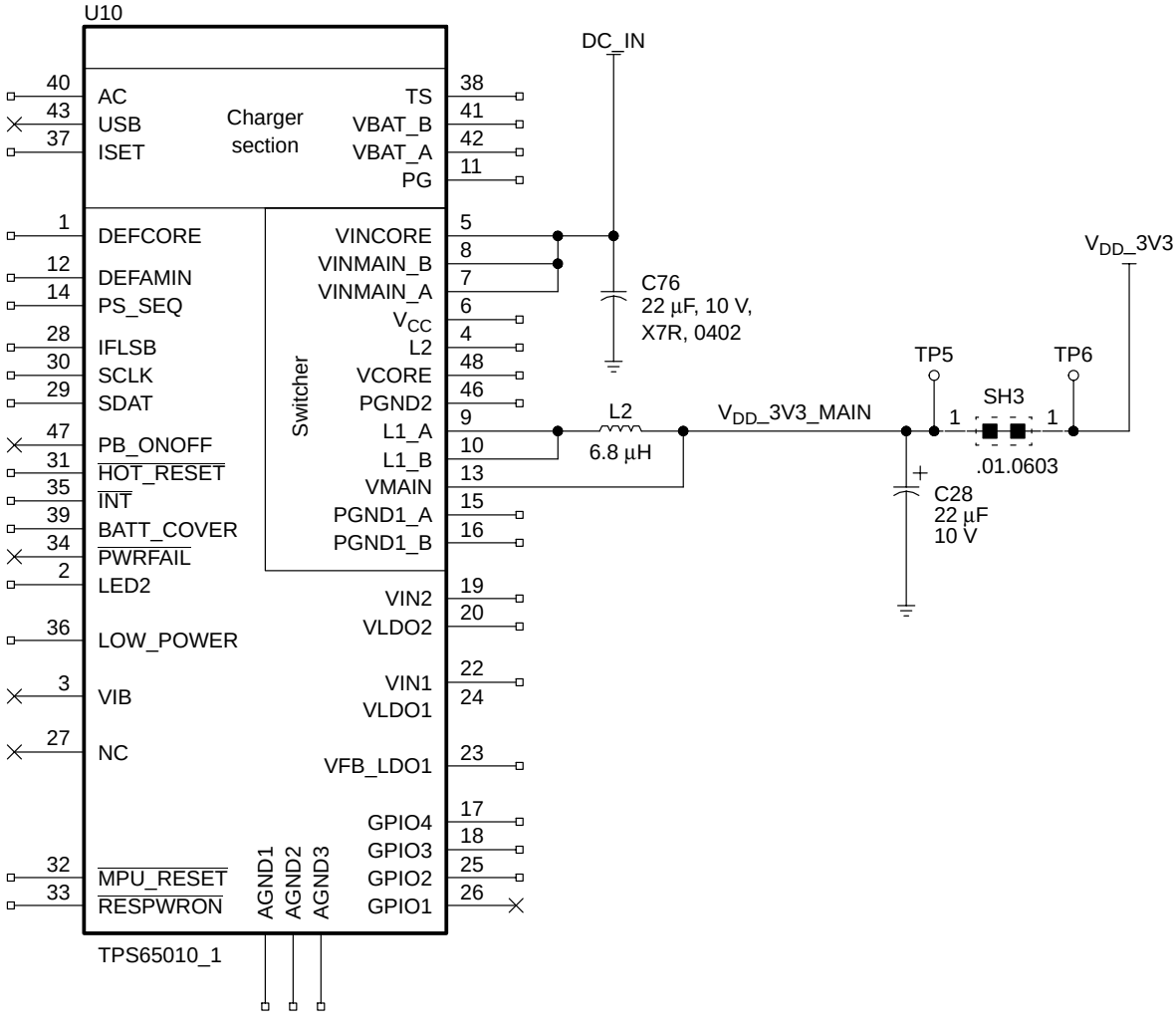
Capacitor C32 provides filtering for the voltage rail. Power for the VLDO1 is supplied by the main dc voltage input rail. Capacitor C31 is required to minimize ripple into the LDO, which can be generated by the TPS65010 back onto the main dc rail.

The current consumption of the V_{DD_SDRAM} voltage rail can be measured across SH6 using test points TP11 and TP12 by using a scope to measure the voltage drop across the .01 Ω resistor in SH6. Refer to *Appendix D* for a description of the current measuring procedure.

1.4.6 3.3 V Supply

Figure 1−10 defines the design of the 3.3 V voltage rail on the OMAP5912 target module. The 3.3 V supply is the main power supply for most of the circuitry on the board including the Flash and Ethernet devices.

Figure 1−10. 3.3 V Power Design



The 3.3 V power supply is supplied by the main switcher in the TPS65010, which incorporates synchronous step-down converters operating typically at 1.25 MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents the converters automatically enter power save mode and operate with pulse frequency modulation (PFM). The 3.3 V converter is capable of delivering 1A output current. The converter output voltages are programmed through the VDCDC1 and VDCDC2 registers in the serial interface. The 3.3 V converter defaults to 3.3 V output voltage because the DEFMAIN configuration pin is tied to V_{CC}. The 3.3 V output voltage can subsequently be reprogrammed after start-up through the serial interface.

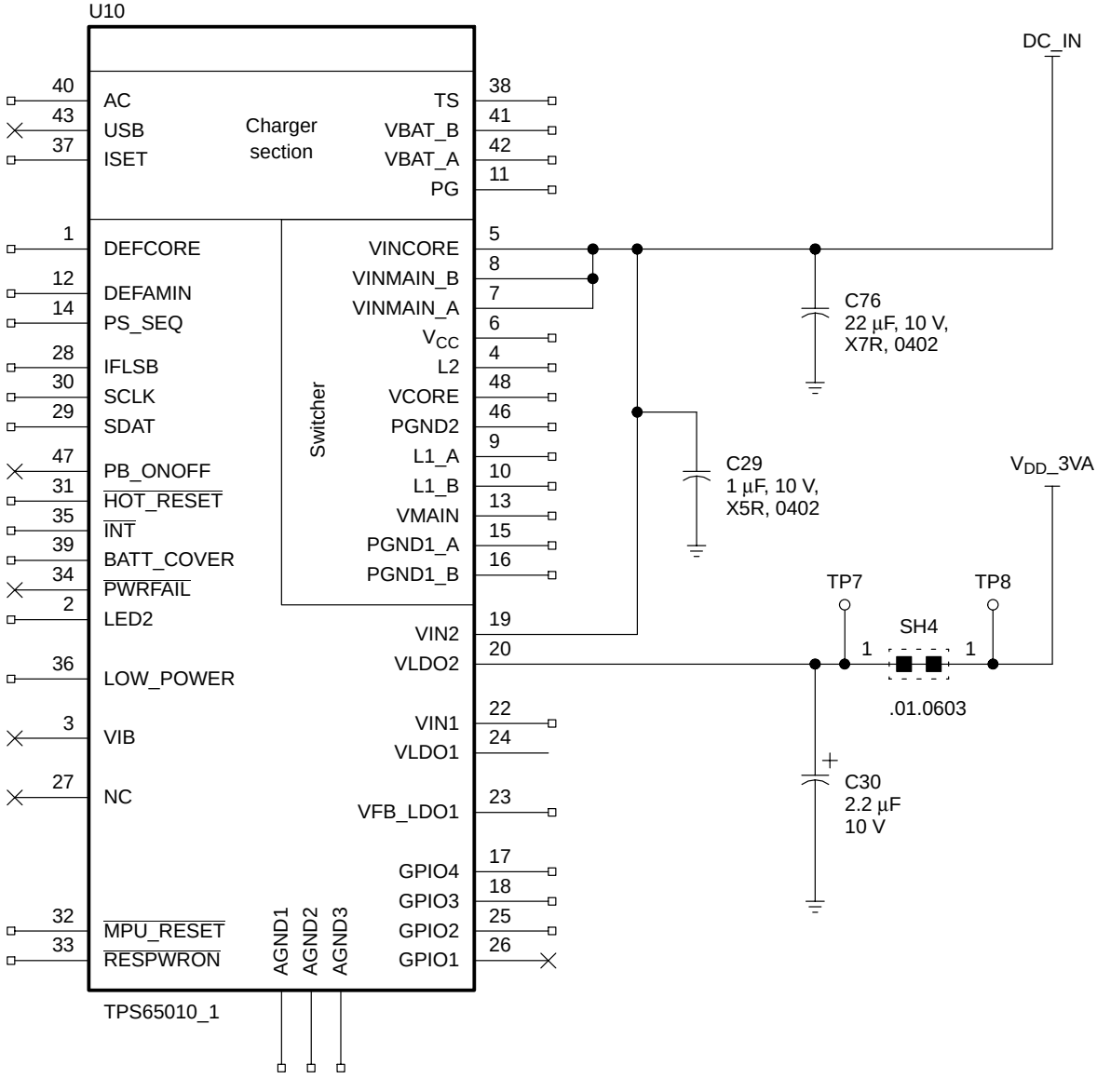
Inductor L2 is required for the switcher in the TPS65010. Capacitor C28 provides filtering for the voltage rail. The 3.3 V power is supplied by the main dc voltage input rail. Capacitor C76 is required to minimize ripple into the switcher.

The current consumption of the V_{DD_3V3} voltage rail can be measured across SH3 using test points TP5 and TP6 by using a scope to measure the voltage drop across the .01 Ω resistor in SH3. Refer to *Appendix D* for a description of the current measuring procedure.

1.4.7 3 V Supply

Figure 1−11 shows the design of the 3 V power supply, which is dedicated for use by the AIC23 CODEC on the board.

Figure 1−11. 3 V Power Design



The 3 V voltage supply uses LDO2 of the TPS65010. LDO2 delivers up to 200 ma. The requirement for the AIC23 is 25 ma. The voltage on LDO2 can be adjusted through software while there is no external adjustment mechanism on VLDO2. The maximum voltage on VLDO2 is 3.0 V. Refer to the *TPS65010: Power and Battery Management IC for Li-Ion Powered Systems* (literature number SLVS149) data sheet for more detail.

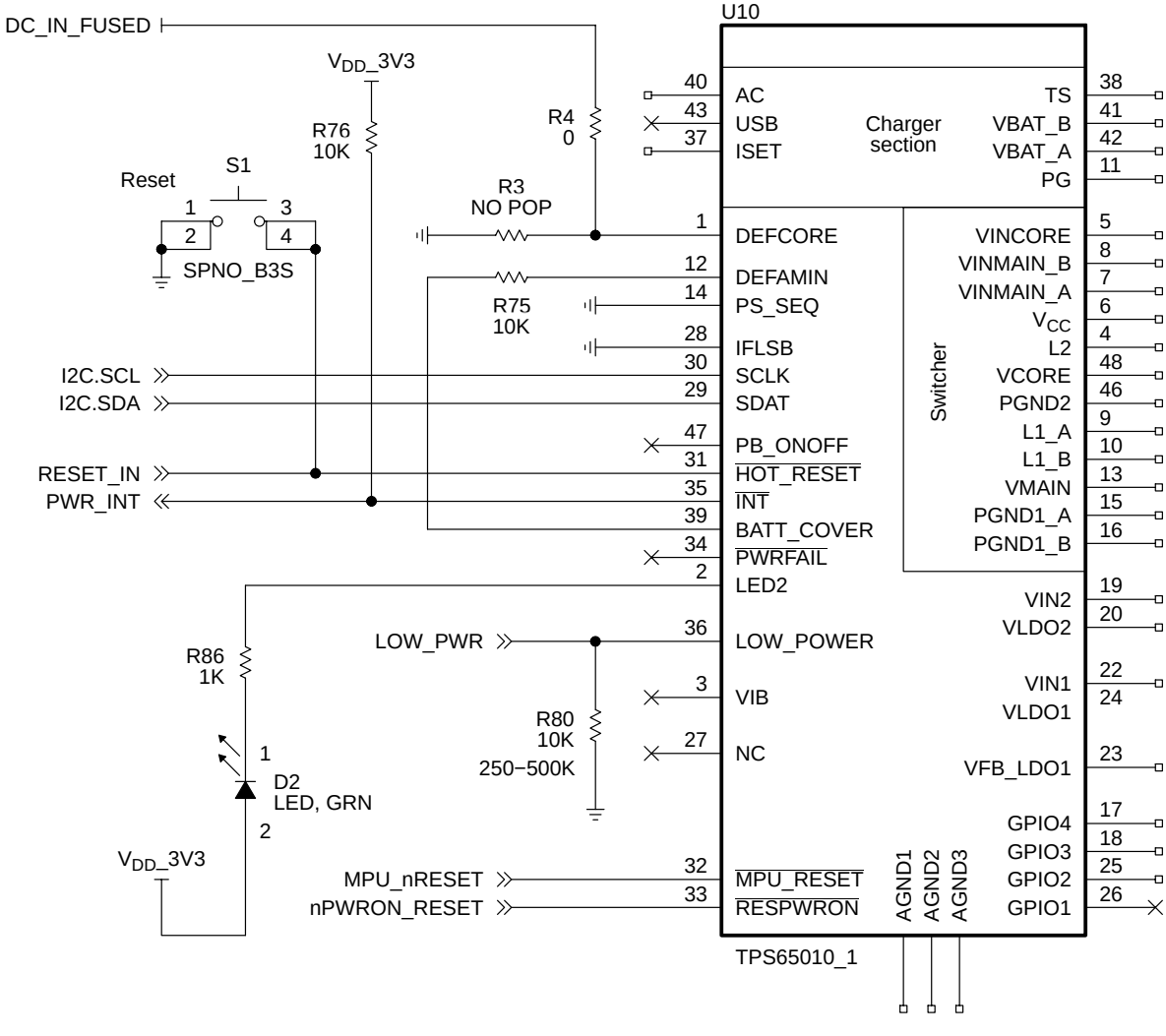
Capacitor C30 provides filtering for the voltage rail. Power for the VLDO2 is supplied by the main dc voltage input rail. Capacitor C29 is required to minimize ripple into the LDO which can be generated by the TPS65010 back onto the main DC rail.

The current consumption of the V_{DD_3VA} voltage rail can be measured across SH4 using test points TP7 and TP8 by using a scope to measure the voltage drop across the .01 Ω resistor in SH4. Refer to *Appendix D* for a description of the current measuring procedure.

1.4.8 Control Interface

Figure 1−12 is the control interface portion of the TSP65010 device.

Figure 1−12. TPS65010 Control Interfaces



1.4.8.1 Default Core Voltage

Resistors R3 and R4 set the default core voltage on power up. With R4 populated and R3 not populated, which is the default configuration, the core voltage is 1.6 V at power up. With R3 populated and not R4, the default voltage is 1.6 V or as determined by the loading of R3 and R4.

1.4.8.2 SW1

SW1 connects to the HOT_RESET input and is used to generate an MPU_RESET signal for the ARM processor. HOT_RESET is de-bounced internally by the TPS65010 and has a typical de-bounce time of 56 ms. The RESET_IN signal connects to the Expansion Connector B pin 59 to allow the expansion cards to generate an MPU_RESET if needed. It can also be used to exit Low Power Mode, in this case the TPS65010 waits until the VCORE voltage has stabilized before generating the MPU_RESET pulse. The MPU_RESET pulse is active low for 100 µsec. HOT_RESET has an internal 1M pullup to V_{CC}.

1.4.8.3 LED D2

The LED2 output is connected to D2 and can be programmed to blink or be permanently on or off. The LED2_ON and LED2_PER registers are used to control the blink rate. For LED2, the minimum blink on time is 10 ms and this can be increased in 127 10 ms-steps to 1280 ms. The minimum blink period is 100 ms and this can be increased in 127 100-ms steps to 12800 ms. Software applications are free to use this as needed.

1.4.8.4 LOW_POWER Input

The low_power state is entered by the processor setting the ENABLE_LP bit in the serial interface and then raising the LOW_PWR pin. The TPS65010 actually uses the rising edge of the internal signal formed by a logical AND of the LOW_PWR and ENABLE LP signals to enter low power mode.

The VMAIN switching converter remains active, but the VCORE converter can be disabled in low power mode through the serial interface by setting the LP_COREOFF bit in the VDCDC2 register. If left enabled, the VCORE voltage is set to the value predefined by the CORELP0/1 bits in the VDCDC2 register. The LDO1OFF/nSLP and LDO2OFF/nSLP bits in the VREGS1 register determine whether the LDOs are turned off or put in a reduced power mode (transient speed-up circuitry disabled in order to minimize quiescent current) in low power mode.

All TPS65010 features remain addressable through the serial interface. TPS65010 can exit this state through the following events:

- ❏ Due to an under-voltage condition at V_{CC}
- ❏ Due to an OVERTEMP condition
- ❏ By the processor deasserting the LOW_POWER pin
- ❏ By your activating the HOT_RESET pin or the PB_ONOFF pin

1.4.8.5 Interrupt Output

The open drain INT pin is used to combine and report all possible conditions through a single pin to the OMAP5912. INT can also be activated if any of the regulators are below the regulation threshold. The PWR_INT signal connects to MPUIO1 on the OMAP5912.

1.4.8.6 I2C

The SDA and SCL pins form the I2C interface that connects to the OMAP5912 processor to allow applications on the OMAP5912 to control the functions of the TPS65010 device.

The I2C serial interface is compatible with the standard and fast mode I2C specifications, allowing transfers at up to 400 kHz. The interface enables most functions to be programmed to new register contents that remain intact as long as V_{CC} remains above 2 V.

The TPS65010 has a 7-bit address with the LSB set by the IFLSB pin which is tied to ground. The 6 MSBs are 100100. Attempting to read data from register addresses not listed in this section results in FFh being read out.

For normal data transfer, DATA is allowed to change only when CLK is low. Changes when CLK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the TPS65010 device generates an acknowledge bit after the reception of each byte.

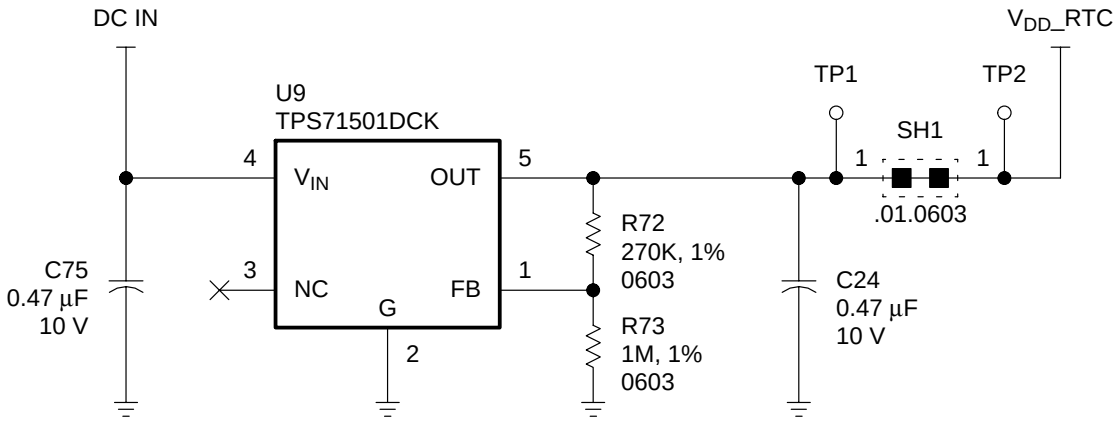
The OMAP5912 must generate an extra clock pulse that is associated with the acknowledge bit. The TPS65010 device must pull down the DATA line during the acknowledge clock pulse so that the DATA line is a stable low during the high period of the acknowledge clock pulse. The DATA line is a stable low during the high period of the acknowledge-related clock pulse. Setup and hold times must be taken into account.

During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave TPS65010 device must leave the data line high to enable the master to generate the stop condition.

1.4.9 Real Time Clock Power

The Real-Time Clock section provides power to the separate Real-Time Clock input of the OAMP5912 processor. Figure 1−13 provides the design of the circuit.

Figure 1−13. Real Time Clock Power Design



The real-time clock power regulator is separate from the TSP6510 and is fed directly by the main dc supply. This insures that power can be fed continuously from the external supply or the battery, when installed. Even though the TPS6510 can power down, the voltage to the RTC is always supplied.

U9 is a TPS71501 LDO regulator. The features of this regulator include:

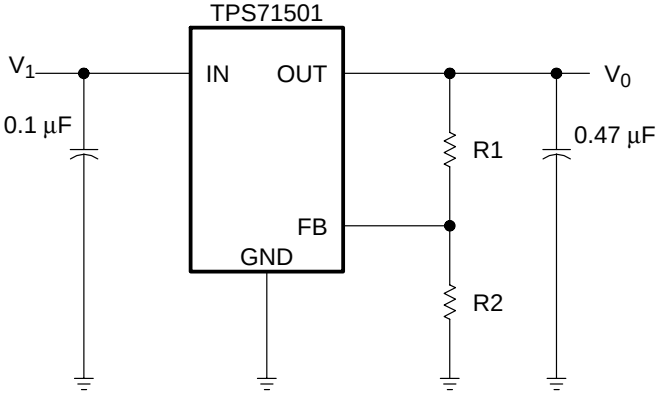
- ❏ 50-mA low-dropout regulator
- ❏ Available in 2.5 V, 3.0 V, 3.3 V, 5.0 V, and adjustable
- ❏ 24-V maximum input voltage
- ❏ Low 3.2-µA quiescent current at 50 mA
- ❏ 5-Pin SC70/SOT-323 (DCK) package
- ❏ Stable with any capacitor (>0.47 ìF)
- ❏ Over current limitation
- ❏ –40°C to 125°C operating junction temperature range

The OMAP5912 target module design uses the adjustable version of the regulator, which allows the voltage to be set by changing R72 and R73. This insures that no matter how the layout is done, exactly 1.8 V is on the OMAP5912 processor pins.

In the Figure 1−13 resistors R1 and R2 should be chosen for approximately 1.5-µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and, therefore, erroneously decreases/increases V_O. The recommended design procedure is to choose R2 = 1 MΩ to set the divider current at 1.5 µA, and then calculate R1 using the information in Figure 1−14.

Figure 1−14. Real Time Clock Voltage Adjustment

$$R1 = \left(\frac{V_0}{V_{ref}} - 1\right) \times R2$$



Output Voltage Programming Guide

Output Voltage	R1	R2
1.8 V	0.499 MΩ	1 MΩ
2.8 V	1.33 MΩ	1 MΩ
5.0 V	3.16 MΩ	1 MΩ

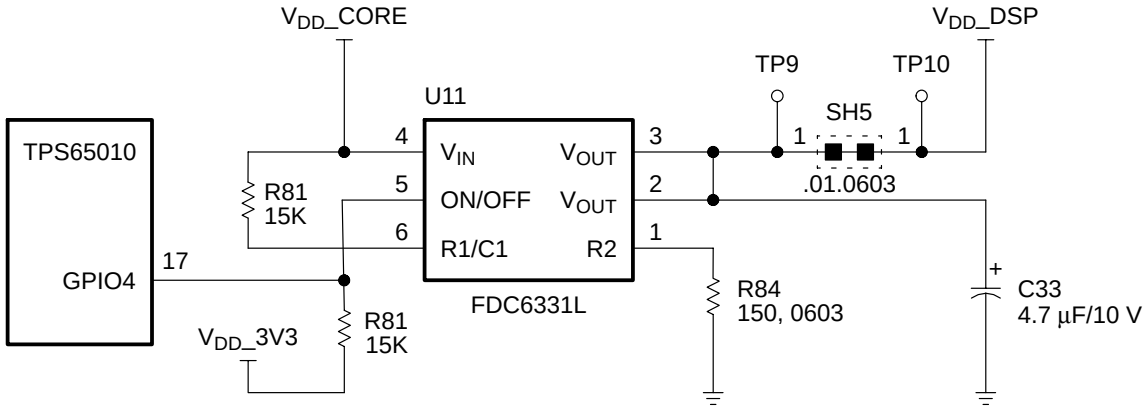
The current consumption of the V_{DD_RTC} voltage rail can be measured across SH1 using test points TP1 and TP2 by using a scope to measure the voltage drop across the .01 Ω resistor in SH1. Refer to *Appendix D* for a description of the current measuring procedure.

There is no separate external battery backup on the real-time clock. This requires that the battery be installed and the OMAP5912 processor be put into deep sleep mode.

1.4.10 DSP Voltage Control

You can remove the DSP voltage to conserve power on the OMAP5192. Figure 1−15 shows the control circuitry for this function.

Figure 1−15. DSP Voltage Control



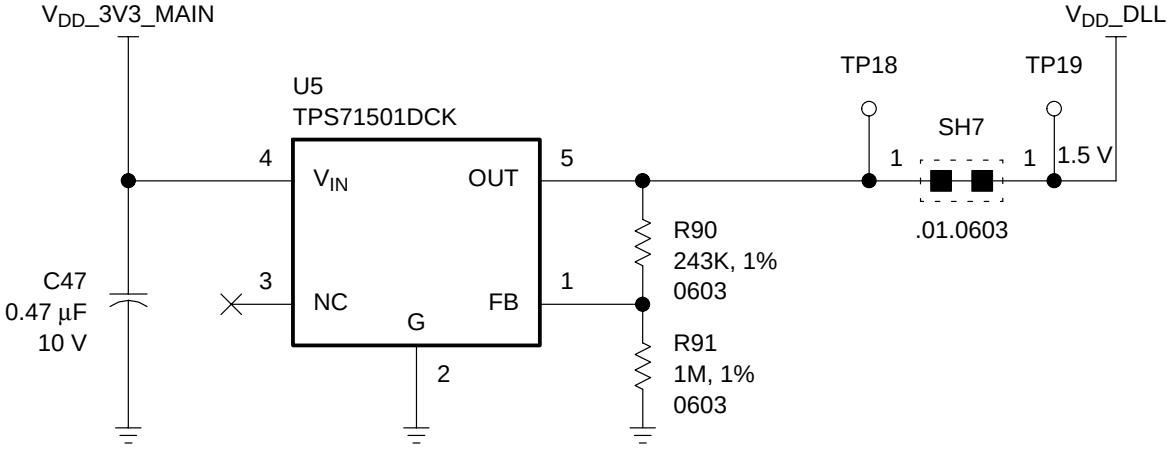
U11 is a FDC6331L™ integrated power switch from Fairchild. This device is an FET switch that allows the voltage on the DSP to be completely removed by taking pin 16 of the TPS6501 low. This load switch integrates a small N-Channel power MOSFET that drives a large P-Channel power MOSFET (Q2) in one tiny 6 package. Access to the GPIO pin is through the I2C bus between the TPS6501 and the OMAP5912.

The current consumption of the V_{DD_DSP} voltage rail can be measured across SH5 using test points TP9 and TP10 by using a scope to measure the voltage drop across the .01 Ω resistor in SH5. Refer to *Appendix D* for a description of the current measuring procedure.

1.4.11 DLL Voltage

Figure 1−16 shows the dedicated LDO regulator for DLL power supply.

Figure 1−16. DLL Voltage Circuit



The DLL power regulator is separate from the TSP6510 and is fed directly by the 3.3 V supply from the TPS65010.

U5 is a TPS71501 LDO regulator. The features of this regulator include:

- ❏ 50-mA low-dropout regulator
- ❏ Available in 2.5 V, 3.0 V, 3.3 V, 5.0 V, and adjustable
- ❏ 24-V maximum input voltage
- ❏ Low 3.2-ìA quiescent current at 50 mA
- ❏ 5-Pin SC70/SOT-323 (DCK) package
- ❏ Stable with any capacitor (>0.47 ìF)
- ❏ Over current limitation
- ❏ –40°C to 125°C operating junction temperature range

The OMAP5912 target module design uses the adjustable version which allows the voltage to be set by changing R90 and R91. This insures that no matter how the layout is done, exactly 1.5 V is on the DLL power pins. The correct value has been set on the OMAP5912 target module as required by the layout.

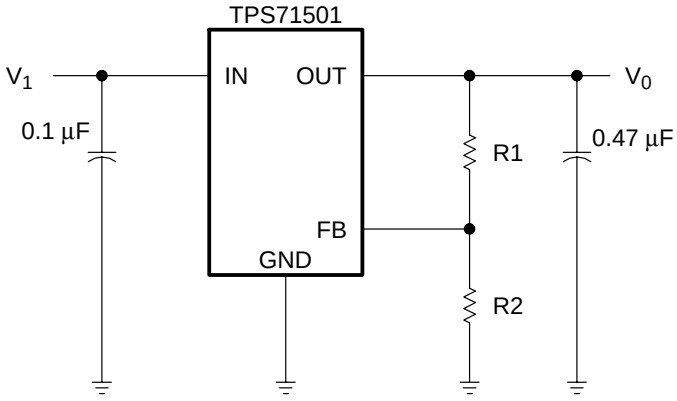
Note: Proximity to OMAP5912

During the layout process, all of the components from C74 forward need to be placed as close to the OMAP5912 as possible.

Figure 1−17 shows that resistors R1 and R2 should be chosen for approximately 1.5-ìA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases V_O. The recommended design procedure is to choose R2 = 1 M? to set the divider current at 1.5 ìA, and then calculate R1 using the equation illustrated in Figure 1−17.

Figure 1−17. DLL Voltage Adjustment

$$R1 = \left(\frac{V_0}{V_{ref}} - 1\right) \times R2$$



Output Voltage Programming Guide

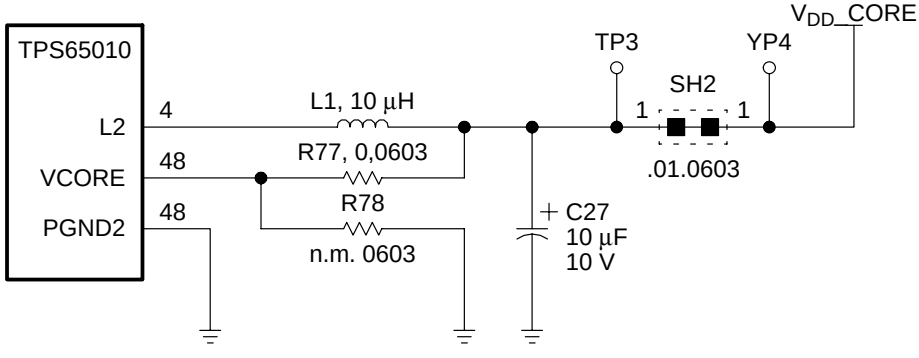
Output Voltage	R1	R2
1.8 V	0.499 MΩ	1 MΩ
2.8 V	1.33 MΩ	1 MΩ
5.0 V	3.16 MΩ	1 MΩ

The current consumption of the V_{DD_DLL} voltage rail can be measured across SH7 using test points TP18 and TP19 by using a scope to measure the voltage drop across the .01 Ω resistor in SH7. Refer to *Appendix D* for a description of the current measuring procedure.

1.4.12 Core Voltage

The Core voltage output of the TPS6510 provides power for the core circuitry inside the OMAP5912. Figure 1−18 shows the external components on the TPS6510.

Figure 1−18. Core Voltage Circuit



The VCORE converter is always enabled in a typical application. The VCORE output voltage can be disabled or reduced from 1.6 V to a lower, preset voltage under processor control. When the processor enters the sleep mode, a high signal on the LOW_PWR pin initiates the change. When the processor is in sleep or low power mode, the VCORE voltage can be programmed to lower voltages without a problem.

In order to insure that the voltage is exactly at the correct value on the OMAP5912 pins, R77 and R78 have been added to allow the VCORE to be set as needed. In the default configuration R78 is not installed and R77 is a 0 Ω resistor.

The exact core voltage for the OMAP5912 is set at 1.6 V. This may change at a later date as testing progresses. This design allows the voltage level to be changed as needed.

The current consumption of the V_{DD_CORE} voltage rail can be measured across SH2 using test points TP3 and TP4 by using a scope to measure the voltage drop across the .01 Ω resistor in SH2. Refer to *Appendix D* for a description of the current measuring procedure.

1.4.13 Battery Mode

An optional Li-ION battery can be connected by using header J4. The selection of this battery is your responsibility; the battery is not supplied with the OMAP5912 target module or the OSK. Refer to the *TPS65010: Power and Battery Management IC for Li-Ion Powered Systems* (literature number SLVS149) data sheet for information on selecting the appropriate battery. In order for the circuit to operate properly, the temperature sense lead must be connected on the battery.

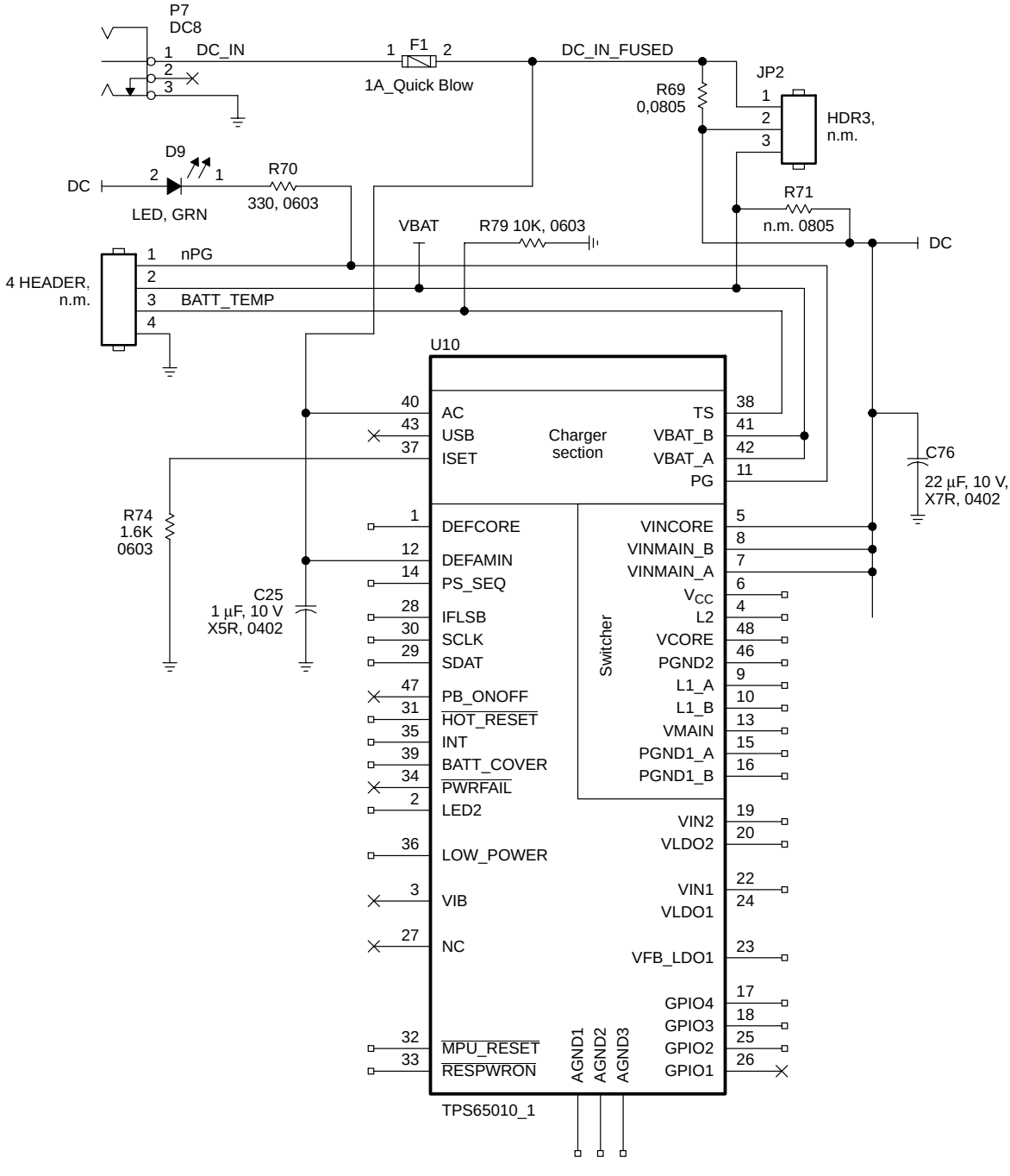
In order for the TPS65010 to operate correctly in the Non-Battery mode, resistor R79 must be installed to insure that the temperature detection circuitry in the TPS65010 is kept happy. When in the battery mode of operation, R79 MUST is removed.

JP2 can be used to attach the battery to the circuitry by placing it so that pins 2 and 3 are shorted. For this to work, R69 and R71 must be removed. Optionally, R69 can be removed and R71 installed.

This places the battery as the main voltage source and uses the dc input only as a supply to the charger circuit of the TPS65010. C25 is a filter for the input of the battery charger circuit in the TPS65010. R74 sets the default charge current for the battery.

Figure 1−19 illustrates the design of the battery mode of operation.

Figure 1−19. Optional Battery Configuration



1.5 Flash Memory

The OMAP5912 target module supports two NOR FLASH devices and can be configured in several ways to obtain a range of Flash densities. It also provides for a mechanism whereby the FLASH can be disabled by an expansion board and that expansion board is then the provider of the FLASH devices.

The following sections provide a description of the FLASH circuitry on the OMAP5912 target module.

1.5.1 Supported Configurations

Table 1−6 defines the supported FLASH memory configuration on the OMAP5912 target module. The standard configuration is the dual 16 MB devices for a total of 32 MB.

Table 1−6. FLASH Configurations

Size	Slot 1	Slot 2
4Mb	4Mb	−
8Mb	4Mb	4MB
8Mb	8Mb	−
16Mb	8Mb	8Mb
16Mb	16Mb	−
32Mb	16Mb	16Mb
32Mb	32Mb	
64Mb	32Mb	32Mb

1.5.2 Supported FLASH Devices

The Flash design supports the devices specified in Table 1−7.

Table 1−7. Supported FLASH Devices

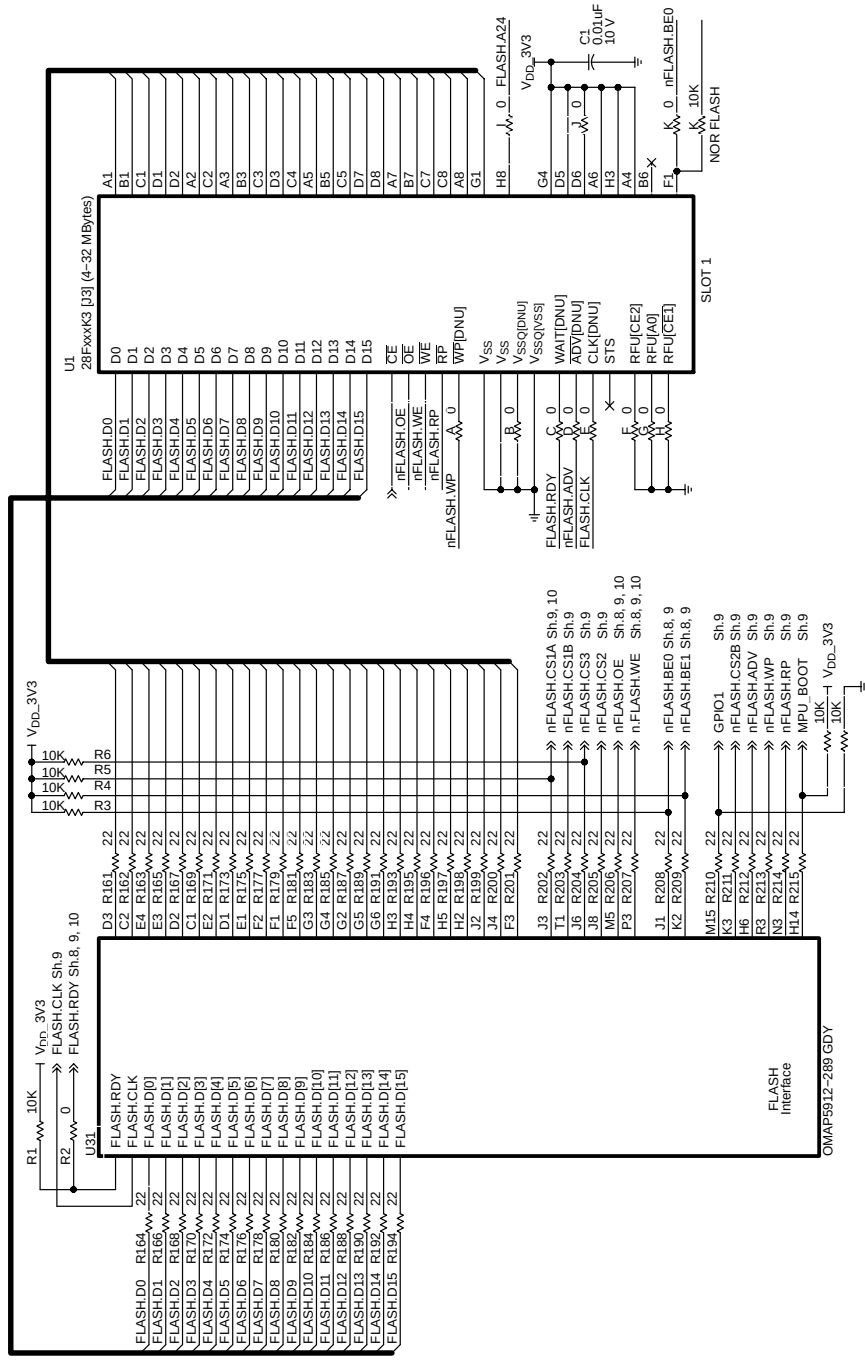
Manufacturer	Part Number	Size
Micron	MT28F320J3	32Mb
Intel	RC28F320J3A110	32Mb
MIcron	MT28F640J3	64Mb
Intel	RC28F640J3A120	64Mb
Micron	MT28F128J3FS-12	128Mb
Intel	RC28F128J3C150	128Mb

Only the NOR flash devices are supported on the OMAP5912 target module. The base configuration is two Micron MT28F128J3 devices. The Micron QFlash™ devices are software compatible with the Intel Strata Flash™ devices. They are offered in a version with a Micron ID or an Intel ID. The Micron ID version is used on the OMAP5912 target module.

1.5.3 FLASH Circuit Design

Figure 1−20 is the interconnection between the OMAP5912 and the FLASH devices. Only one FLASH device is shown. The differences in connections required for the second FLASH device is contained in the text.

Figure 1−20. FLASH Circuitry Design



1.5.4 Address Bus

The OMAP5912 has 24 address lines, A1−A25. Only address lines 1−24 are used for the largest device. Even though all of the address lines are connected to the devices, not all of the pins can be used depending on which device is installed.

1.5.5 Data Bus

The data bus from the OMAP5912 is 16 bits wide. All of the data bits are connected to each of the Flash devices.

1.5.6 Control Signals

All signals are the same for both slots except the chip select (CS) signal. Slot 0 uses the CSXA while Slot 1 uses CSXB. Depending on the type of memory used, some of the signals may not be connected. This is handled by the populating or unpopulating of certain resistors.

The signal GPIO1 is used to set the configuration of the Flash bus. To be compatible with the OMAP5912 target module design, this pin must be tied to ground. The MPU_BOOT signal should be tied high for the OMAP5912 target module application.

1.5.7 Address Decode Logic

Figure 1−21 illustrates the design of the decode logic for the FLASH devices.

Figure 1−21. FLASH Decode Logic

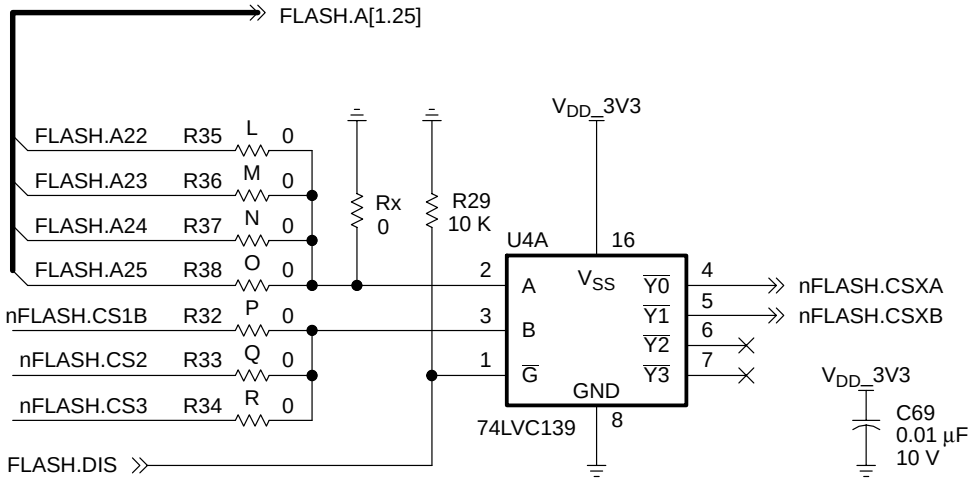


Table 1−8 defines how the resistors are to be loaded for each of the supported memory size configurations. In order to support contiguous memory between the two memory device slots, the address decoding for the second block must be moved. This is done by moving the A bit of the ‘139 decoder to the appropriate address line at the beginning of the Slot 2 address range. The default value of the OMAP5912 target module design is highlighted in Table 1−8.

Table 1−8. Flash Address Decode Resistor Options

Devices	Size	L	M	N	O	Address line used
1	4MB	x				A22
2	8MB	x				A22
1	8MB		x			A23
2	16MB		x			A23
1	16MB			x		A24
2	32MB			x		A24
1	32MB				x	A25
2	64MB				x	A25
1	64MB					None

In the event a single 64MB device is used, Rx in Figure 1−21 must be installed to insure that the full 64MB range is valid for the chip select.

The base address range can also be moved between chip selects. Table 1−9 defines how this can be done. The moving of the chip select is not impacted by whether or not there is one or two memory devices used.

Table 1−9. Flash Chip Select Resistor Options

Chip Select	Size	P	Q	R
CS1B	32MB	x		
CS2	64MB		x	
CS3	64MB			x

If CS1B is to be used, it is limited to 32MB of address space. Insure that the desired memory configuration works with CS1B. CS3 is the default configuration.

1.5.8 General-Purpose Mode Support

The OMAP5912 comes with an internal boot ROM that enables you to boot and flash the external flash memory on the board. There are two different ways of booting the OMAP5912 device:

- **Full Boot**. The device boots from the internal ROM. When used with the external Boot loader software the internal ROM can then be used to boot the Flash device on the board.
- **Fast Boot**. The device boots from the external Flash that is on CS3.

In order to select between these modes, GPIO_13 is tested. If GPIO_13 is low, then the Fast Boot method is selected. If GPIO_13 is high, then the Full Boot method is selected. In order to allow the setting of GPIO_13 either high or low, JP3 is provided.

1.6 DDR SDRAM

This section covers the design of the SDRAM section of the OMAP5912 target module. While the OMAP5912 supports SDR (Single Data Rate) SDRAM, this design uses an DDR (Dual Data Rate) SDRAM device. The device is the Elpida 246 Mb Mobile DDR EDK2516CBBH™.

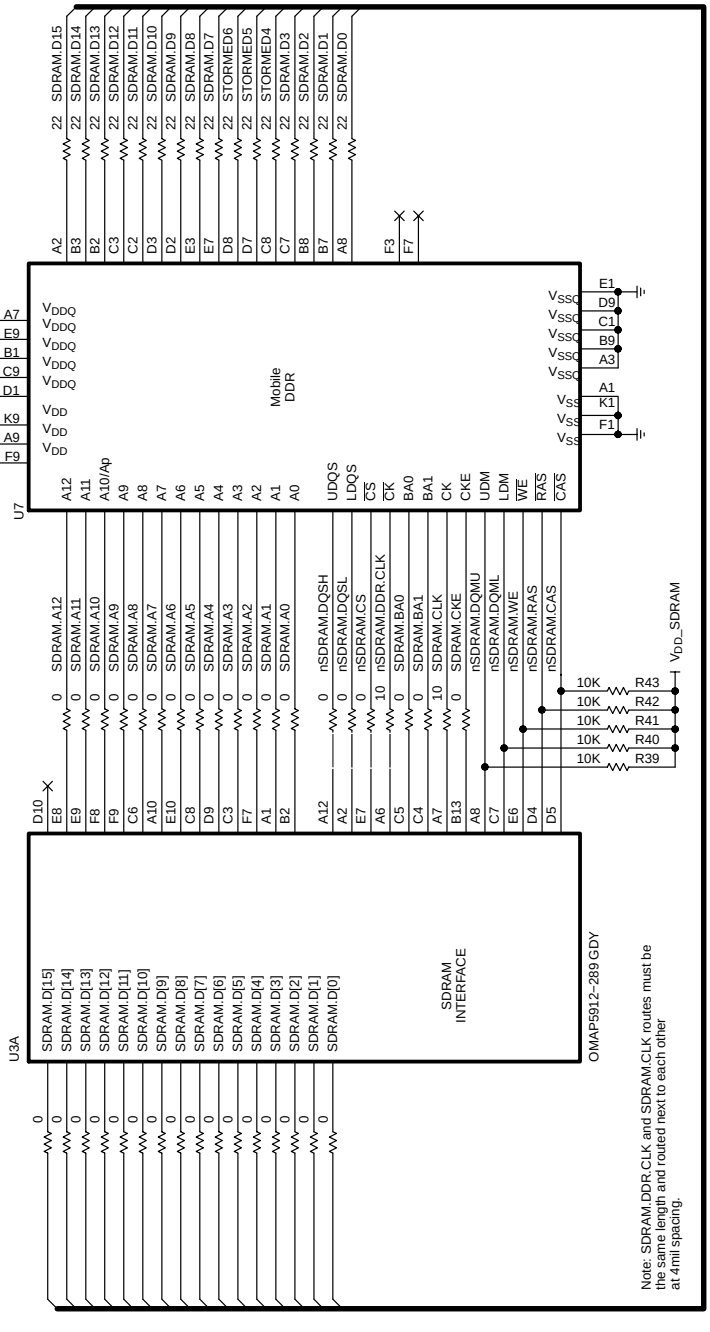
Only Mobile DDR devices are supported by the OMAP5912. Mobile provides for low current operation and supports only 1.8 V voltage rails and interfaces. The OMAP5912 supports up to 512 Mb of DDR SDRAM. Due to the limitation of the single device, the maximum memory is limited by the single devices that are on the market.

Refer to the Elpida *256 bits DDR Mobile RAM EDK2516CBBH* data sheet for more infomation.

1.6.1 DDR SDRAM Circuit Design

Figure 1−22 illustrates the design of the DDR SDRAM interface on the OMAP5912 target module.

Figure 1−22. Mobile DDR SDRAM Design



1.6.2 Elpida EDK2516CBBH DDR Device

The features of the Elpida EDK2516CBBH device include:

- ❏ Low voltage power supply
  - ■ V_{DD}: 1.8 V ± 0.15 V
  - ■ V_{DDQ}: 1.8 V ± 0.15 V
- ❏ Wide temperature range (.25°C to 85°C)
- ❏ Programmable partial array self refresh
- ❏ Programmable driver strength
- ❏ Auto temperature compensated self-refresh by built-in temperature sensor
- ❏ Deep power down mode
- ❏ Small package (60-ball FBGA)
- ❏ FBGA package is lead free solder (Sn-Ag-Cu)
- ❏ Data rate of 200 Mbps/IO(max)
- ❏ Double Data Rate architecture with two data transfers per one clock cycle
- ❏ Bi-directional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver.
- ❏ 1.8 V LVCMOS interface
- ❏ Command and address signals refer to a positive clock edge
- ❏ Quad internal banks controlled by BA0 and BA1
- ❏ Data mask (DM) for write data
- ❏ Wrap sequence = sequential/ interleave
- ❏ Programmable burst length (BL) = 2, 4, 8
- ❏ Automatic precharge and controlled precharge
- ❏ Auto refresh and self refresh
- ❏ 8,192 refresh cycles/64 ms (7.8ìs maximum average periodic refresh interval)
- ❏ Burst termination by Burst stop command and Precharge command

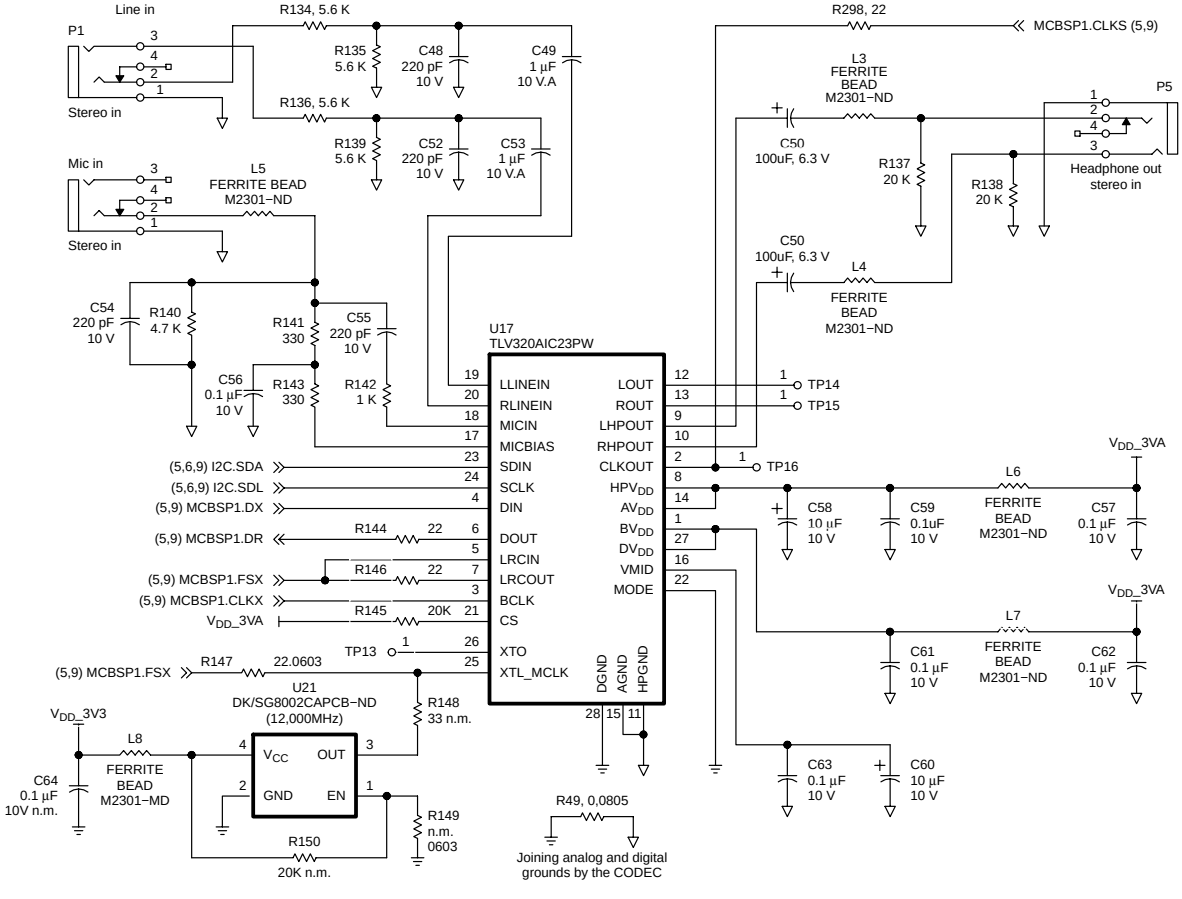
1.7 Audio Codec

An AIC23 audio CODEC is included on the OMAP5912 target module to provide audio input and output. The design of the audio circuit is described in this section.

1.7.1 Audio CODEC Design

Figure 1−23 illustrates the design of the audio CODEC circuit on the OMAP5912 target module.

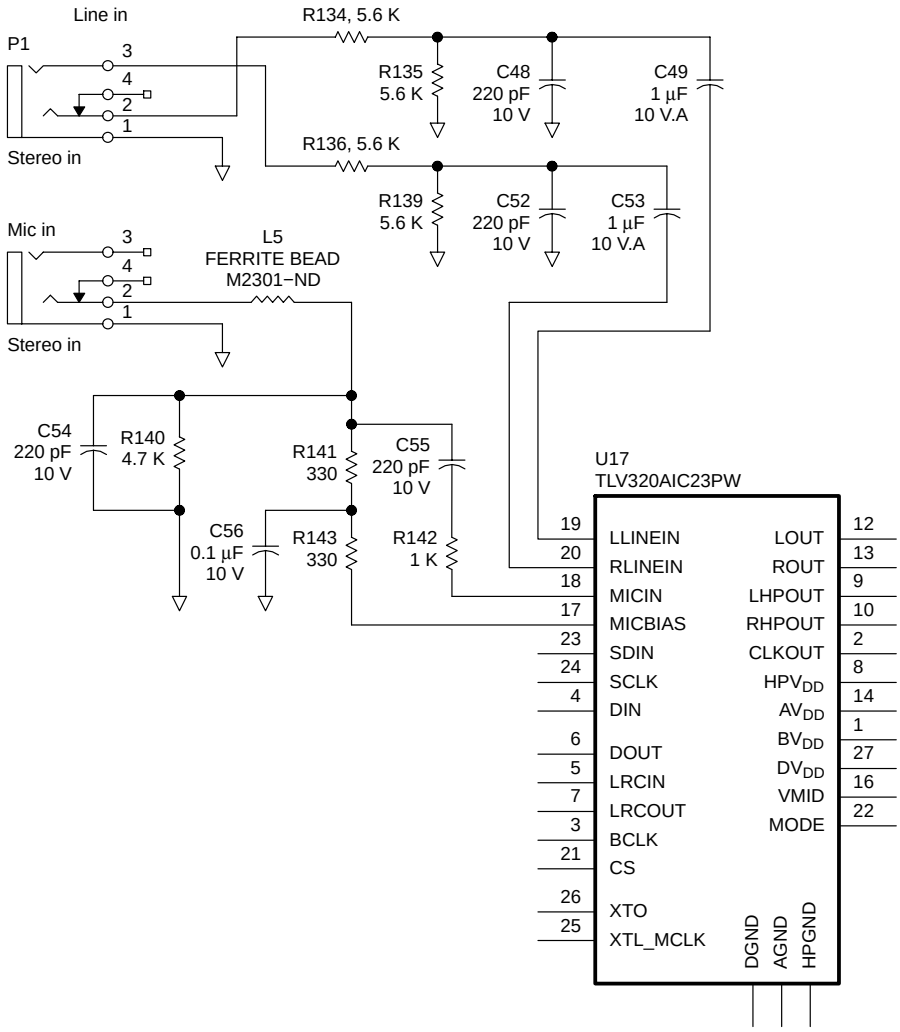
Figure 1−23. AIC23 Audio CODEC Design



1.7.2 Audio Inputs

The audio circuit has two stereo audio inputs. Figure 1−24 shows the audio inputs.

Figure 1−24. AIC23 Audio Inputs



The TLV320AIC23 has line inputs for the left and the right audio channels (RLINEIN and LLINEIN). Access to these signals is gained through connector P1, which is a 3.5mm audio jack. Both line inputs have independently programmable volume controls and mutes. The gain is independently programmable on both left and right line-inputs.

R134 and C48 create a high pass filter for the audio input on the left channel. R136 and C52 create a high pass filter for the audio input on the right channel. Resistors R139 and R136 are used to insure the line inputs are terminated when no signal is present at P1.

Connector P6 is a 3.5mm jack that is used to connect the microphone input to the AIC23. MICIN is a high-impedance, low-capacitance input that is compatible with a wide range of microphones. It has a programmable volume control and a mute function. Active and passive filters prevent high frequencies from folding back into the audio band.

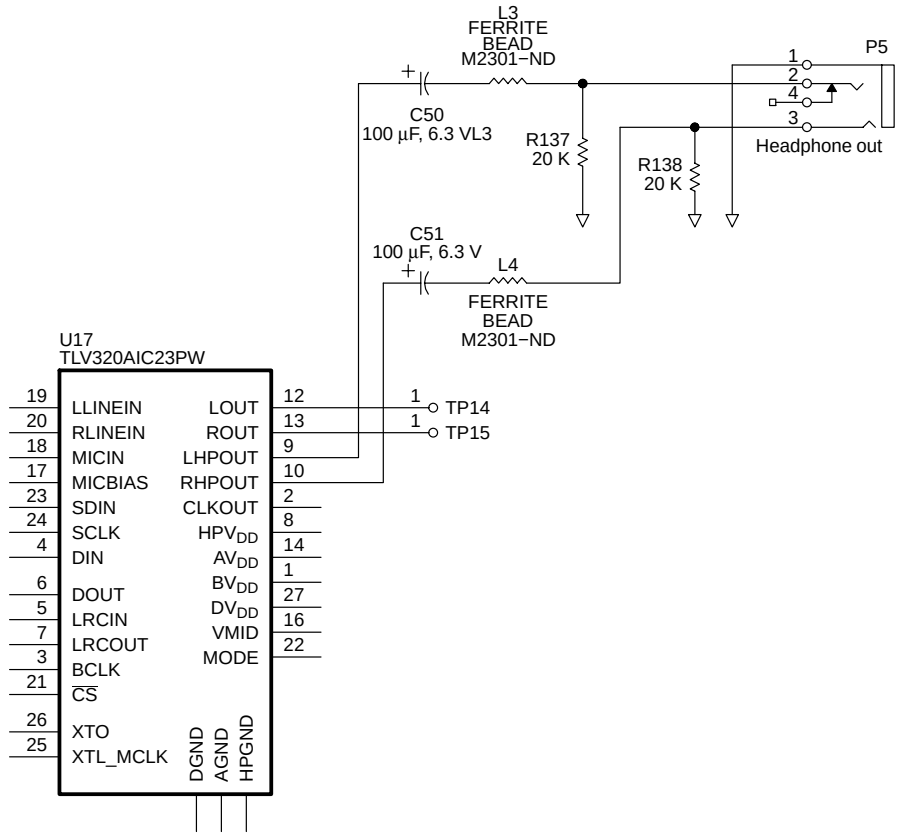
The MICBIAS output provides a low-noise reference voltage suitable for biasing electret-type microphones and the associated external resistor biasing network. The maximum source current capability is 3 mA. This limits the smallest value of external biasing resistors that can be used safely. The MICBIAS output is not active in standby mode.

1.7.3 Audio Outputs

Access to the headphone outputs is through a single 3.5 mm stereo jack. While suitable for driving a headphone, the output is not suitable for driving a set of speakers unless those speakers are powered. The audio is coupled to the left and right channels through C30 and C31. Each channel has a ferrite bead and resistor circuit to help minimize transmissions out the audio jack.

Figure 1−25 illustrates the design of the stereo headphone output of the AIC23 Audio CODEC.

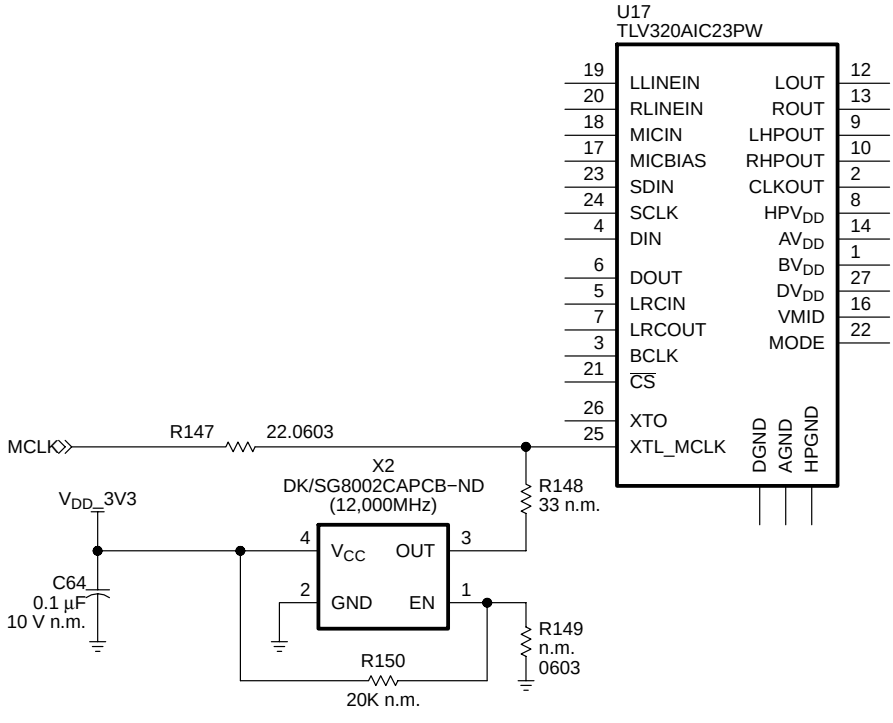
Figure 1−25. AIC23 Audio Outputs



1.7.4 Clocking

The AIC23 requires an external 12 MHZ clock to drive the internal components. Figure 1−26 shows that there are two ways of accomplishing this.

Figure 1−26. AIC23 Clocking Options



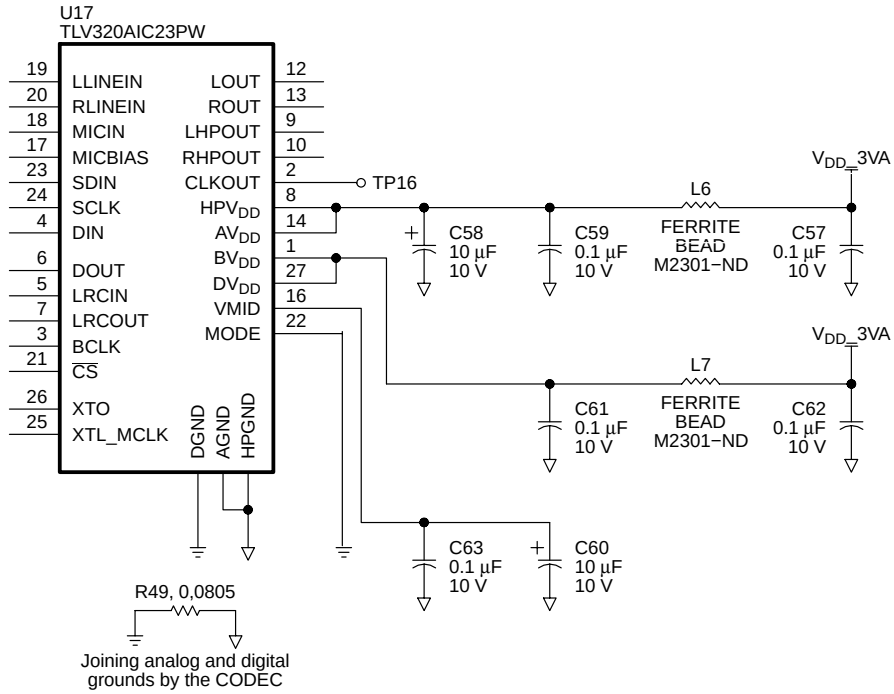
X2 is an external 12 MHZ crystal oscillator that can provide the 12 MHZ clock when installed. R3 must be mounted to make the connection. X2 is not installed on the OMAP5912 target module and the primary clock source option for providing the clock is used.

The primary clock source is the MCLK signal from the OMAP5912. MCLK can be set to 12 MHZ and fed directly into the AIC23. This is the primary method use on the OMAP5912 target module. In this option X2, R150, R149, R148, and C64 are not installed.

1.7.5 Power

Figure 1−27 illustrates the power design for the AIC23.

Figure 1−27. AIC23 Power Section



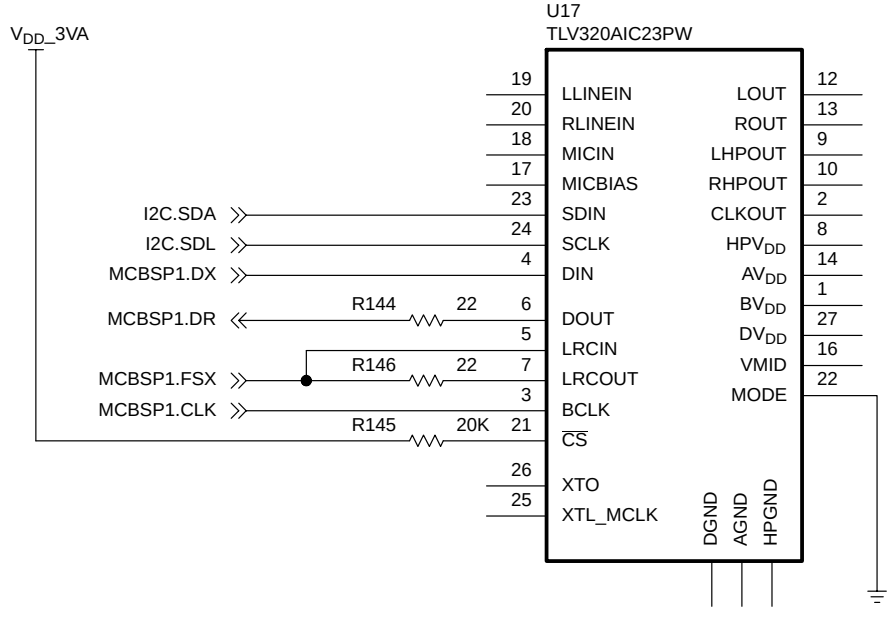
Each of the power inputs is heavily filtered to minimize the affect noise may have on the audio component. The power rails are actually split into analog and digital rails. BV_{DD} and DV_{DD} are the digital rails for the AIC23. HPV_{DD} and AV_{DD} are the analog rails. The LC circuits minimize any high frequency noise from entering the AIC23 whose harmonics could potentially cause noise in the audio.

Resistor R49 allows for the grouping of the grounds for the AIC23 such that they connect at a single point to the system ground. This technique is used to insure that the PCB layout software does not allow the ground to be connected on a common ground plane.

1.7.6 OMAP5912 Interface

Figure 1−28 illustrates the design of the interface between the OMAP5912 and the AIC23 CODEC.

Figure 1−28. AIC23 OMAP5912 Interface



The mode of the AIC23 control interface is controlled by the MODE pin. If the mode pin is tied low, then the interface is a 2-wire interface or I2C. If the mode pin is tied high, then it is in the SPI mode. In the OMAP5912 target module design, the interface is set to 2-wire mode. In 2-wire mode, the data transfer uses SDIN for the serial data and SCLK for the serial clock. The start condition is a falling edge on SDIN while SCLK is high. The seven bits following the start condition determine which device on the 2-wire bus receives the data. R/W determines the direction of the data transfer. The TLV320AIC23 is a write-only device and responds only if R/W is 0. The device operates only as a slave device whose address is selected by setting the state of the $\overline{CS}$ pin as defined in Table 1−10.

Table 1−10. AIC23 I2C Address Definition

CS State	Address
0	0011010
1	0011011

In the OMAP5912 target module design, this signal is pulled high via R145. The I2C bus is used to set up all control functions on the AIC23.

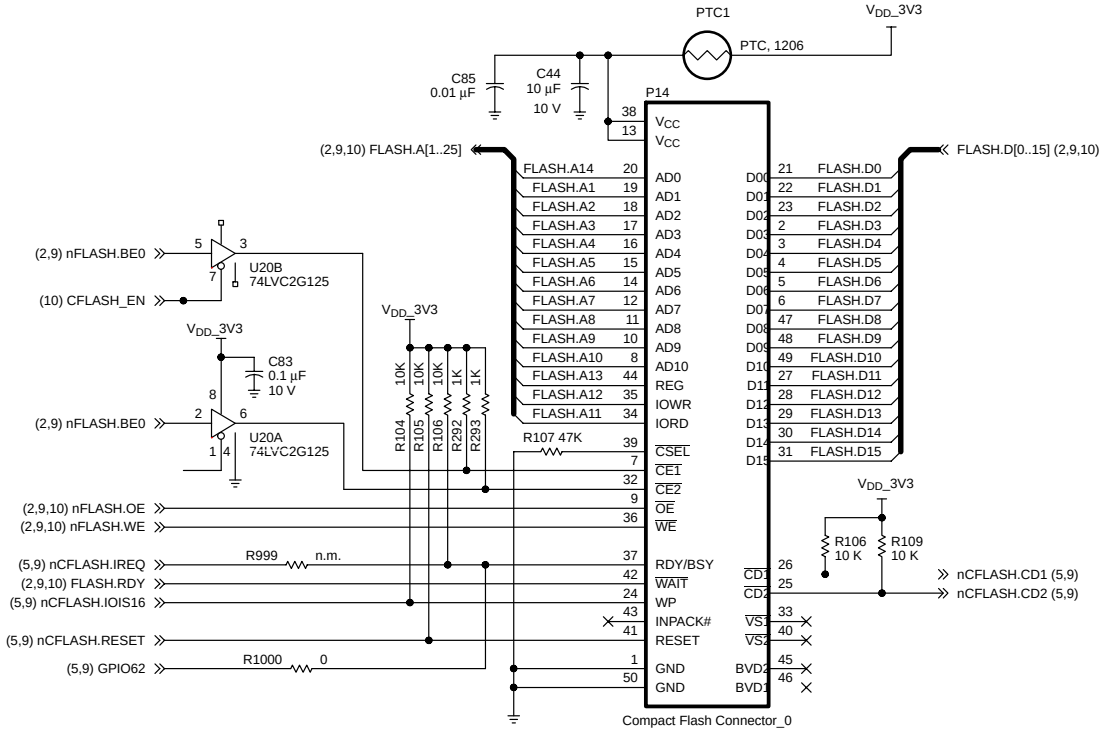
McBSP1 is used from the OMAP5912 as the audio channel interface for the AIC23. The McBSP1 is set up as an I2S interface. McBSP1 is used because in the OMAP5912 the DSP has direct access to McBSP1.

The AIC23 is set up as the master. Thus, the AIC23 provides the frame sync and clock to the OMAP5912. McBSP1.DX is the input path to the AIC23 while MCBSP1.DR is the output path. McBSP1.CLK is the clock output from the AIC23. McBSP1.FSX is the frame clock for the data signal.

1.8 Compact Flash

The OMAP5912 target module has a Compact Flash interface that supports both Type I and Type II cards. Figure 1−29 details the design of the interface.

Figure 1−29. Compact Flash Socket Design



1.8.1 Integrated Interface

The OMAP5912 has an integrated control interface that allows for a Compact Flash device to be connected directly to the OMAP5912. The Compact Flash controller (CFC) interfaces a Compact Flash and a classical memory interface. Control signals from the memory interface are processed through the CFC to drive a Compact Flash card, and control signals from Compact Flash are processed to perform a data transfer to the memory interface.

1.8.2 Compact Flash Interface Signals

Signals on the OMAP5912 are converted to Compact Flash control signals when the Compact Flash is accessed. Table 1−11 defines how the signal functions change when the Compact Flash is accessed.

Table 1−11. OMAP5912 Compact Flash Interface

Compact Flash Name	Name	I/O	Compact Flash Description
A10−A1	FLASH.A[10−1]	OUT	Address bus
A0	FLASH.A[14]	OUT	Address bus
REG	FLASH.A[13]	OUT	Attribute memory select
IOWR	FLASH.A[12]	OUT	I/O data write
IORD	FLASH.A[11]	OUT	I/O data read
WAIT	FLASH.RDY	IN	Wait
WE	FLASH.WE	OUT	Strobe
CE2	FLASH.BE[1]	OUT	Card enable
CE1	FLASH.BE[0]	OUT	Card enable
D15−D0	FLASH.D[15:0]	I/O	Data bus
OE	FLASH.OE	OUT	Output enable
WP IOIS16	CFLASH.IOIS16	IN	Write protect 8/16 bits selection
RESET	CFLASH.RESET	OUT	Reset
CD1	CFLASH.CD1	IN	Card detect
CD2	CFLASH.CD2	IN	Card detect
RDY/BSY IREQ	CFLASH.IREQ	IN	Ready for new data

1.8.3 CFLASH.IREQ

Currently, the CFLASH.IREQ in not working as defined. Therefore, the ability to connect the CFLASH.IREQ to either the predefined CFLASH.IREQ pin or to GPIO62 was added. The default configuration uses GPIO62, although this could change in the future.

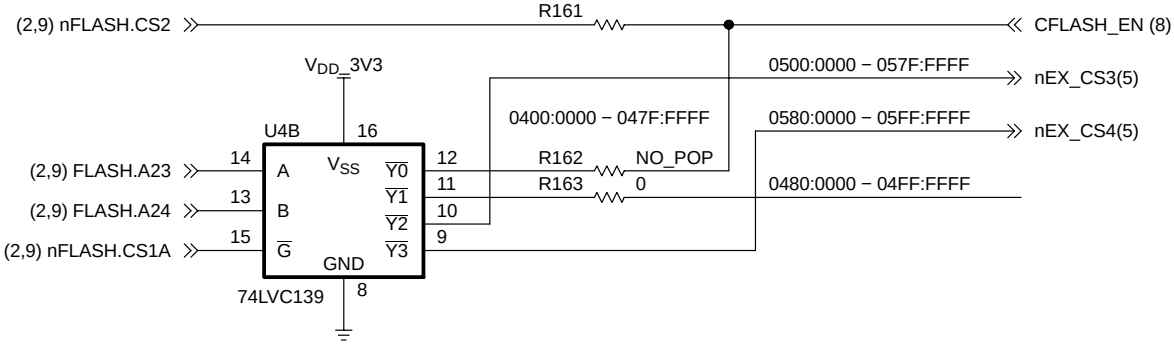
1.8.4 Address Decode Logic

Within the OMAP5912, the Compact Flash interface can be placed at CS0−CS3 by setting a register in the OMAP5912. The OMAP5912 target module design recognizes either CS1 or CS2 only in its design. CS2 is the default selection in order to not interfere with the Ethernet controller that is located at CS1.

No external chip select signal is needed as this is generated on the BE0 and BE1 pins from the OMAP5912. However, BE0 and BE1, when not being used to access the compact flash card, can still be active during other memory accesses, which could lead to false enables being sent to the compact flash card. Therefore, the BE0 and BE1 pins must be qualified with an external chip select signal called CFLASH_EN. This signal is used to activate two SN74LVC2G125 buffers. When qualified with the CFLASH_EN signal, the BE0 and BE1 signals are allowed to pass to the Compact Flash interface. Resistors R292 and R293 are set at 1K to allow for a fast rise time when the CFLASH_EN signal is driven high because this causes the buffers to tri-state. CFLASH_EN is connected to CS2.

Figure 1−30 shows the decode logic for the CFLASH_EN signal.

Figure 1−30. CFLASH_EN Signal Decode Logic



U4B is half of an SN74LVC139™ decoder. The CFLASH_EN signal enables the CE buffers for the Compact Flash interface. This Compact Flash interface can reside in either CS1 or CS2. CS2 is the default configuration, meaning R161 is loaded and R162 is not loaded.

The Compact Flash interface is active for the entire chip select range selected. Depending on what specific addresses are selected, the Compact Flash interface takes on the characteristics of a specific compact flash mode. The compact flash card supports the following access modes:

- ❑ Common memory
- ❑ Attribute memory

The controller manages access to the different modes of the Compact Flash (access protocol in these modes follows the Compact Flash standard). Table 1−12 shows which address range implements which access mode for the Compact Flash interface.

Table 1−12. Compact Flash Memory Mapping

Space Name	Start Address and CS Address	Stop Address	Size
Compact Flash memory space	0000:0000	0000:07FF	2K bytes
Compact Flash attribute space	0000:0800	0000:0FFF	2K bytes

1.8.5 Data Bus Interface

The data bus is connected to the Compact Flash interface and is used as with any normal memory device interface.

1.8.6 Power interface

Power to the Compact Flash interface is supplied by the 3.3 V supply. PTC1 is a self-healing current-limiting device. This is provided in lieu of a fuse device. When the current exceeds 1A max, the resistance of the PTC goes up, limiting the current to the Compact Flash interface. The hold current is specified at 500ma.

1.9 JTAG/Multi-ICE Interface

A 14-pin header is provided for access to the standard JTAG interface. In addition, a 20-pin header is provided for access to the Multi-ICE connector.

1.9.1 JTAG/Multi-ICE Features

The JTAG/Multi-ICE interface provides the following features:

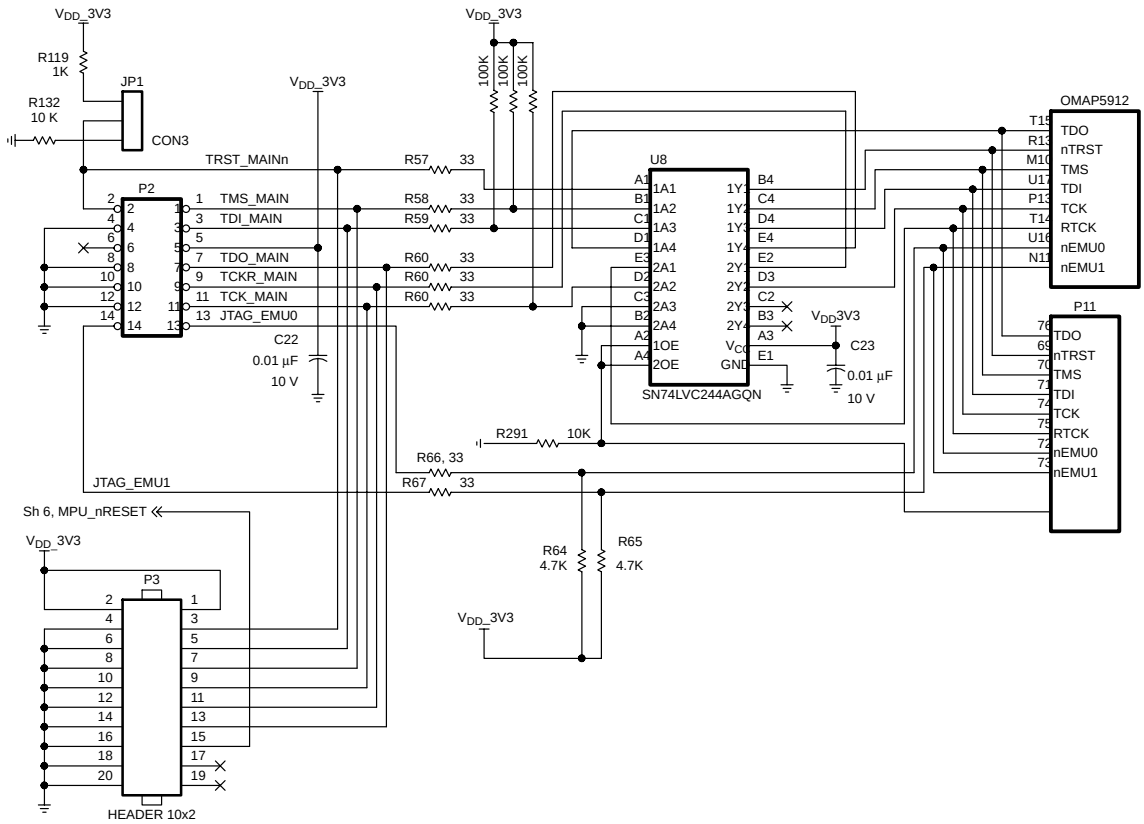
- ❑ JTAG port Buffer
- ❑ Standard 14-pin JTAG connector
- ❑ 20 Pin Multi-ICE Connector
- ❑ Ability to reset the ARM processor for the Multi-ICE interface
- ❑ Strappable JTAG reset nTRST pull down
- ❑ Disable pin for ADM shutdown

1.9.2 Design Description

The OMAP5912 provides the signals for the JTAG interface. The JTAG interface is routed through U8, which is an SN74LVC244AGQN™ buffer. Series resistors R57−62 and R66−67 are intended to control the over and undershoot of the signals. Resistors R54−56 and R64−65 provide additional pull up current for the signals as needed. These values can be adjusted during the testing phase of the board.

Figure 1−31 illustrates the design of the JTAG interface on the OMAP5912 target module.

Figure 1−31. JTAG Interface Design



P2 is the connector for the 14-pin JTAG connector. Pin 6 is removed and acts as a polarization key for the standard JTAG connector. JP1 is used to set the default termination of the nTRST signal to either being pulled down, for the standard JTAG, or pulled up, for the Multi-ICE interface.

P3 is the connector for the Multi-ICE cable. The polarity of the nTRST signal is different on the Multi-ICE than it is on the standard JTAG.

The U8 buffer is normally enabled via the pull down resistor R291. When the OMAP5912 target module is plugged into a motherboard or other test board, the JTAG interface on the OMAP5912 target module can be disabled by pulling this pin high. This allows the JTAG signals to used on the other board as needed. Access to the JTAG signals and the control pin is found on P11.

1.10 USB Port

A standard USB Host Port interface is provided through a standard Type A connector. This can be used to connect such devices as:

- ❑ Keyboard
- ❑ Mouse
- ❑ Digital cameras

The design supports the configuring of the USB port to provide client side capabilities. Both host and client operations are discussed.

1.10.1 USB Features

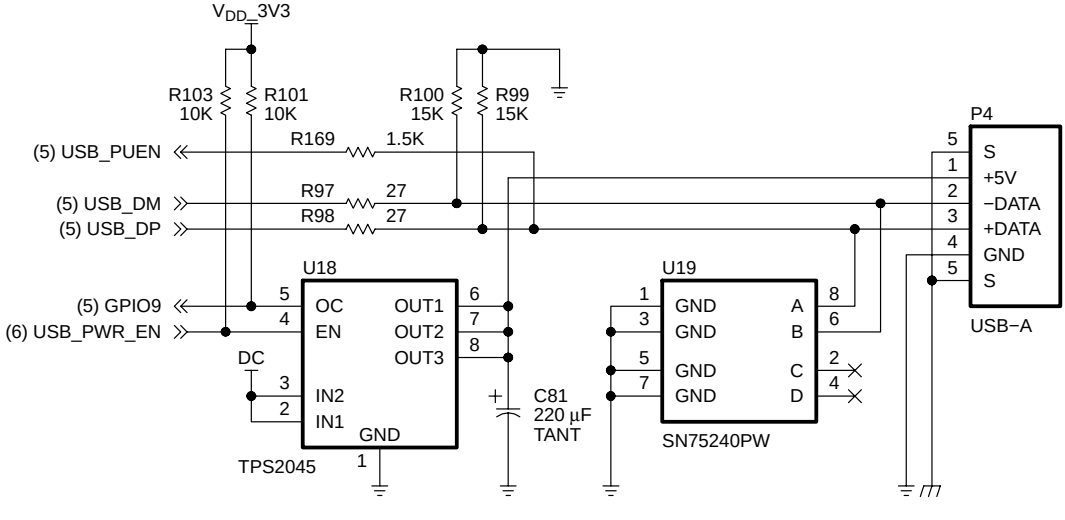
The OMAP5912 USB host controller communicates with USB devices at the USB low-speed (1.5M bit-per-second maximum) and full-speed (12M bit-per-second maximum) data rates. It is compatible with the *Universal Serial Bus Specification Revision 2.0* and the *Open HCI—Open Host Controller Interface Specification for USB,* Release 1.0a.

A single USB Type B connector is provided on the OMAP5912 target module. Power is provided by the OMAP5912 target module through this connector to power external devices.

1.10.2 Design Description

Figure 1−32 illustrates the design diagram of the USB interface.

Figure 1−32. USB Host Design



1.10.2.1 Host Operation

The USB.DM, USB.DP, and GPIO9 signals are used on the OMAP5912 to implement the USB host interface.

USB.DM and USB.DP provide the plus and minus polarity of the interface signals directly to the USB connector P4 through a pair of 27 Ω resistors. Initialization of the OMAP5912 device to support this mode of operation requires proper setting of the top-level pin multiplexing for pins USB.DP and USB.DM and selection of an HMC_MODE value, which routes a host controller port to pin group 0. OTG_SYSCON_1.USB0_TRX_MODE must be set to 3 to allow proper operation of the integrated USB transceiver. OMAP5912 integrated pull downs for pins USB.DP and USB.DM do not meet the USB specifications for D+ and D– pull downs. The external 15K pull down resistors, R199 and R100, are implemented to meet this requirement. USB.PUEN is used in the GPIO mode to detect the over current mode. Proper initialization of the OMAP5912 device to support the host mode of operation on pin P4 requires setting of the top-level pin multiplexing.

To select the USB Host mode, GPIO9 needs to be high (default selection), and ball P4 on OMAP5912 (USB.PUEN) needs to be placed into high Z state (by setting FUNC_MUX_CTRL_D[5:3] = 100) in order to negate the impact of the 1.5k Ω resistor pull up on the D+ signal.

See section 1.10.2.2, *Client Operation*, for information on activating the Client mode of operation.

U16 is a TPS2014 power distribution switch. The TPS2014 power distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The high-side switch is a 95-mW n-channel MOSFET. The switch is controlled by a logic enable that is compatible with 3-V logic. Gate drive is provided by an internal charge pump designed to control the power switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 4 V. When the output load exceeds the current-limit threshold or a short is present, the TPS2014 limits the output current to a safe level by switching into a constant-current mode, and the over-current logic output is set to low. Continuous heavy overloads and short circuits increase the power dissipation in the switch and cause the junction temperature to rise. A thermal protection circuit is implemented, which shuts the switch off to prevent damage when the junction temperature exceeds its thermal limit. An under-voltage lockout is provided to ensure the switch is in the off state at start-up. The TPS2014 is designed to limit at 1.2 A. C81 is a low ESR capacitor required for the output of the TPS2014.

U19 is a USB port transient protection device. The SN75240 is a dual transient voltage suppressor designed to provide additional electrical noise transient protection to two USB ports. Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the OMAP5912 if they are of sufficient magnitude and duration. The SN75240 significantly increases the port ESD protection level and reduces the risk of damage to the large and expensive circuits of the USB port.

U10 is the TPS65010 power management device. In order to save as many GPIO pins on the OMAP5912 as possible, the GPIO pin on the TPS65010 was used as the enable pin for the TPS2014. A high on EN turns off the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 mA. A logic-zero input restores bias to the drive and control circuits, and turns the power on. To access the GPIO pin on the TPS65010, the I2C interface is used to communicate to the GPIO pin.

Access to the USB.DM, USB.DP, and USB.PUEN (GPIO58) signals can be obtained through the B connector P10, if use by the expansion cards is desired. For this to happen, nothing can be plugged into the USB connector P4.

1.10.2.2 Client Operation

With the use of an external adapter (See section 3.11, *USB Client Adapter*), the USB interface can be converted for use as a Client interface.

Resistor R169 is connected to the USB_PUEN signal as shown in Figure 1−32. USB_PUEN is required to activate the client interface. In the host mode, this pin is left tri-stated. By default U18 is not enabled. This must be left disabled in the Client mode.

The external adapter connects to P4 and converts it to the client gender. R169 is used to signal the host that Client mode is active and ready to be identified. This does not interfere with host operation as the USB.PUEN signal is not activated through software.

To select USB Client (function) with the use of an external adapter, GPIO9 must be low, and the USB.PUEN signal must be muxed onto the P4 ball (set FUNC_MUX_CTRL_D[5:3] = 000).

1.11 Serial Port

Access to a single serial port with an RS232 level driver through a DB9 connector is provided. This is used for downloading and connecting to a serial debugger or terminal device.

1.11.1 Features

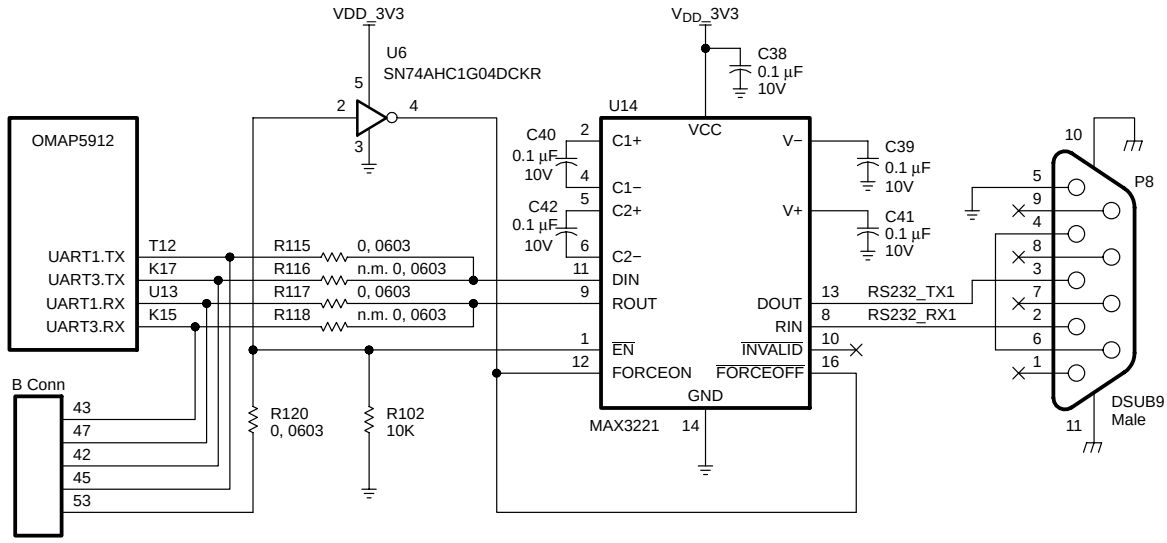
Features of the serial interface are:

- ❏ Default OMAP5912 UART1 connection
- ❏ Optional OMAP5912 UART3 connection
- ❏ 240K baud max speed
- ❏ DB9 male connector
- ❏ Disable pin accessible through the expansion connectors
- ❏ TX,RX signals
- ❏ Ground

1.11.2 Design Description

Figure 1−33 illustrates the design diagram of the serial interface.

Figure 1−33. Serial Port Interface



Serial port UART1 is the default serial port used from the OMAP5912. The port can be switched to UART3 by removing R115 and R117 and installing R116 and R118. R116 and R118 are not populated on the board.The UART1 and UART3 signals from the OMAP5912 are also available on Expansion Connector B for use by the expansion cards. If the use of these signals is needed, pin 53 on the B Connector can be pulled high and the RS232 driver is disabled through the SN74AHC1G04 inverter.

The RS232 driver function is performed by U14, a TI MAX3221, which converts the signals from the OMAP5912 to the required RS232 levels. The output levels of the MAX3221 swing + 3 V and − 3 V. While this is more than adequate to drive a terminal or PC located in the area, it may not be adequate to drive over long distances. If long distance is a requirement, the signals need to be boosted to higher levels.

Pins 4 and 6 are looped back on each other to allow for the detection of the OMAP5912 target module by the applications running on the PC.

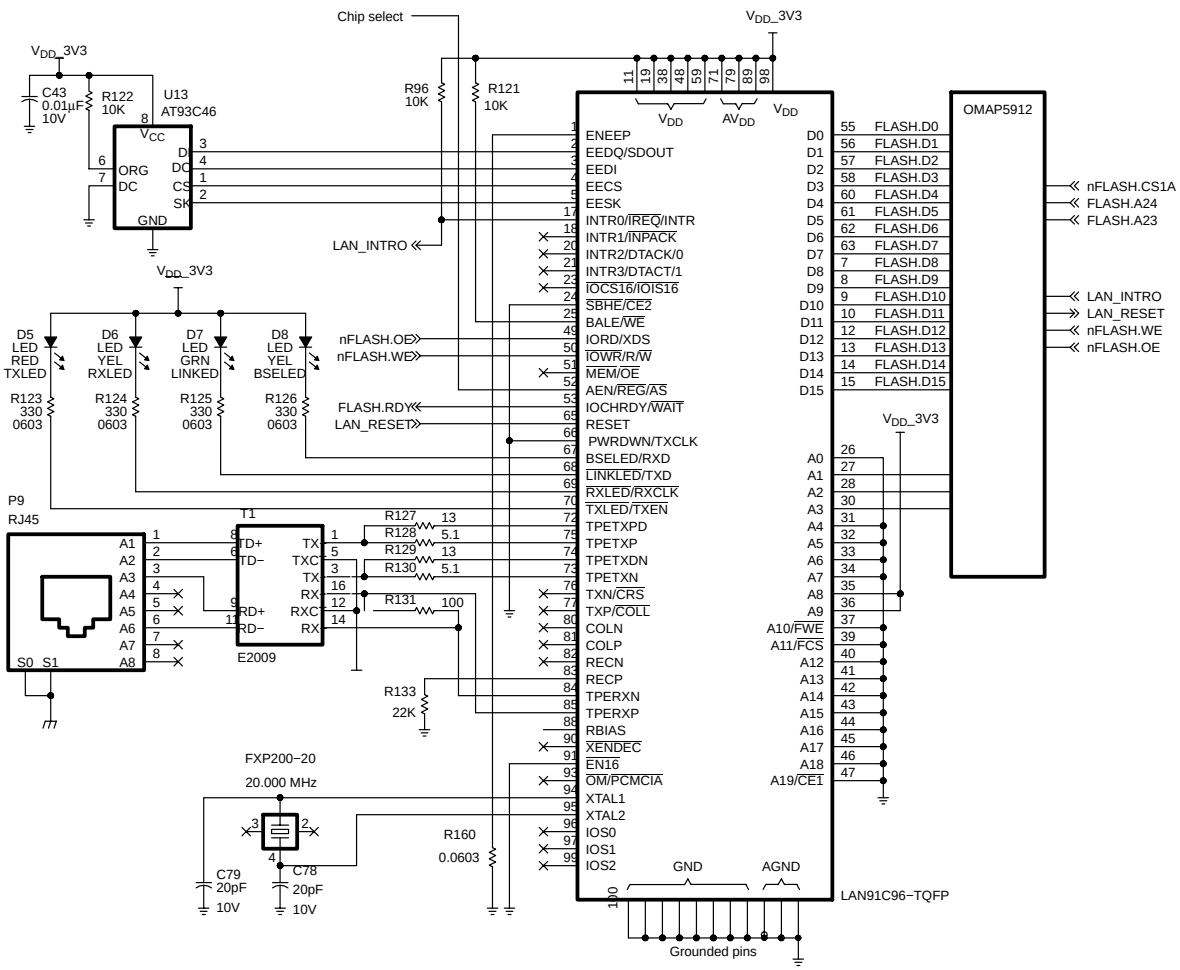
1.12 Ethernet

The OMAP5912 target module is equipped with a 10Mb Ethernet port. This section describes the Ethernet interface and how it connects to the OMAP5912 processor.

1.12.1 Ethernet Circuit Design

Figure 1−34 illustrates the design of the Ethernet interface on the OMAP5912 target module.

Figure 1−34. 10 Mb Ethernet Design



The following sections break down the design and provide detailed description of each section. Included in the descriptions are:

- ❏ Interrupt
- ❏ Memory address decode
- ❏ LAN91C96™
- ❏ Crystal circuit
- ❏ Output section
- ❏ EEPROM
- ❏ Status LEDS

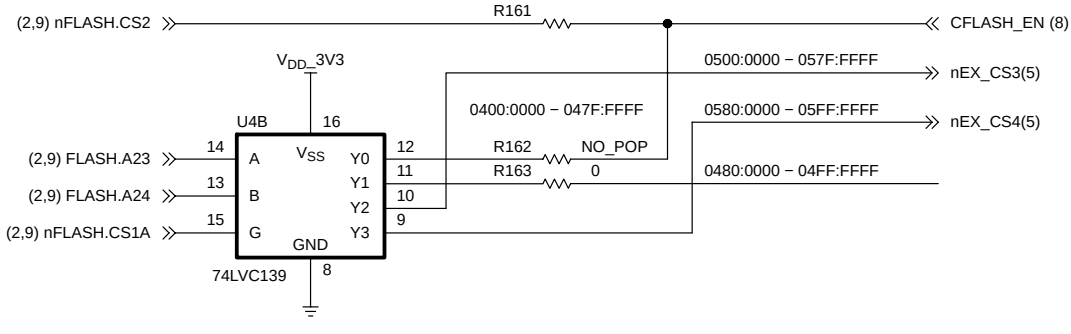
1.12.2 Interrupt

The interrupt line from the LAN91C96 device connects to GPIO0 on the OMAP5912. Pin 93 nROM/nPCMCIA is open, which puts the LAN91C96 in Local Bus mode. In this mode the LAN_INTR0 is an active high line. On the schematic the signal LAN_INTR0 is shown to be active high.

1.12.3 Memory Address Decode

The second half of U4, a 74LVC139™ device from Phillips Electronics, is used to create the address decode for the Ethernet controller and the Compact Flash. Figure 1−35 illustrates the design of the decode circuit.

Figure 1−35. Ethernet Address Decode Logic



CS1A can be shared with the Compact Flash circuit or the Compact Flash circuit can have its own address chip select. There are two different scenarios that are supported by this design:

- ❏ Compact Flash and Ethernet share CS1A
- ❏ Compact Flash uses CS2 and Ethernet uses CS1A

The default configuration is that the Compact Flash occupies CS2 and the Ethernet occupies CS1A.

1.12.3.1 Chip Select Shared

CS1A from the OMAP5912 is used as the primary chip select. Address lines A24 and A23 from the OMAP5912 are also used to minimize the amount of the CS1A block that is being used by the LAN91C96. Address line A24 must be low and A23 must be high to select the LANC9196 device. This results in an effective address range of 0480:0000−04FF:FFFF for the Compact Flash. Use address 0490:0000 as the base address for the LAN91C96 in this scenario.

1.12.3.2 Compact Flash CS2 and Ethernet CS1A

The Compact Flash is mapped to CS2 and the Ethernet is mapped to CS1A as the default configuration.

1.12.3.3 Expansion Chip Selects

Two signals are provided for use by the expansion cards. These are nEX_CS3 and nEX_CS4. These signals are brought out onto the expansion connectors.

1.12.4 LAN91C96

The LAN91C96 Ethernet Transceiver from SMSC provides the interface for the Ethernet function on the OMAP5912 target module. The features of the LAN91C96 are:

- ISA/PCMCIA single-chip ethernet controller
- A subset of Motorola 68000 Bus Interface Support
- Supports full duplex switched ethernet
- Supports enhanced Transmit Queue Management
- 6K bytes of on-chip RAM
- Supports IEEE 802.3 (ANSI 8802-3) Ethernet Standards
- Automatic detection of TX/RX polarity reversal
- Simultasking early transmit and early receive functions
- Enhanced early transmit function
- Receive counter for enhanced early receive
- Hardware memory management unit
- Optional configuration via Serial EEPROM interface (jumperless)

- ❏ Supports single + 3.3 V V_{CC} Designs
- ❏ 6 Bit Data and Control Paths
- ❏ Fast Access Time (40 ns)
- ❏ Pipelined Data Path
- ❏ Handles Block Word Transfers for any Alignment
- ❏ High Performance Chained (”Back-to-Back”) Transmit and Receive
- ❏ Dynamic Memory Allocation Between Transmit and Receive
- ❏ Flat Memory Structure for Low CPU Overhead
- ❏ Buffered Architecture, Insensitive to Bus Latencies (No Overruns/Underruns)
- ❏ Integrated 10BASE-T Transceiver Functions:
  - ■ Driver and Receiver
  - ■ Link Integrity Test
  - ■ Receive Polarity Detection and Correction
- ❏ 10 Mb/s Manchester Encoding/Decoding and Clock Recovery
- ❏ Automatic Retransmission, Bad Packet Rejection, and Transmit Padding
- ❏ External and Internal Loopback Modes
- ❏ Four Direct Driven LEDs for Status/ Diagnostics

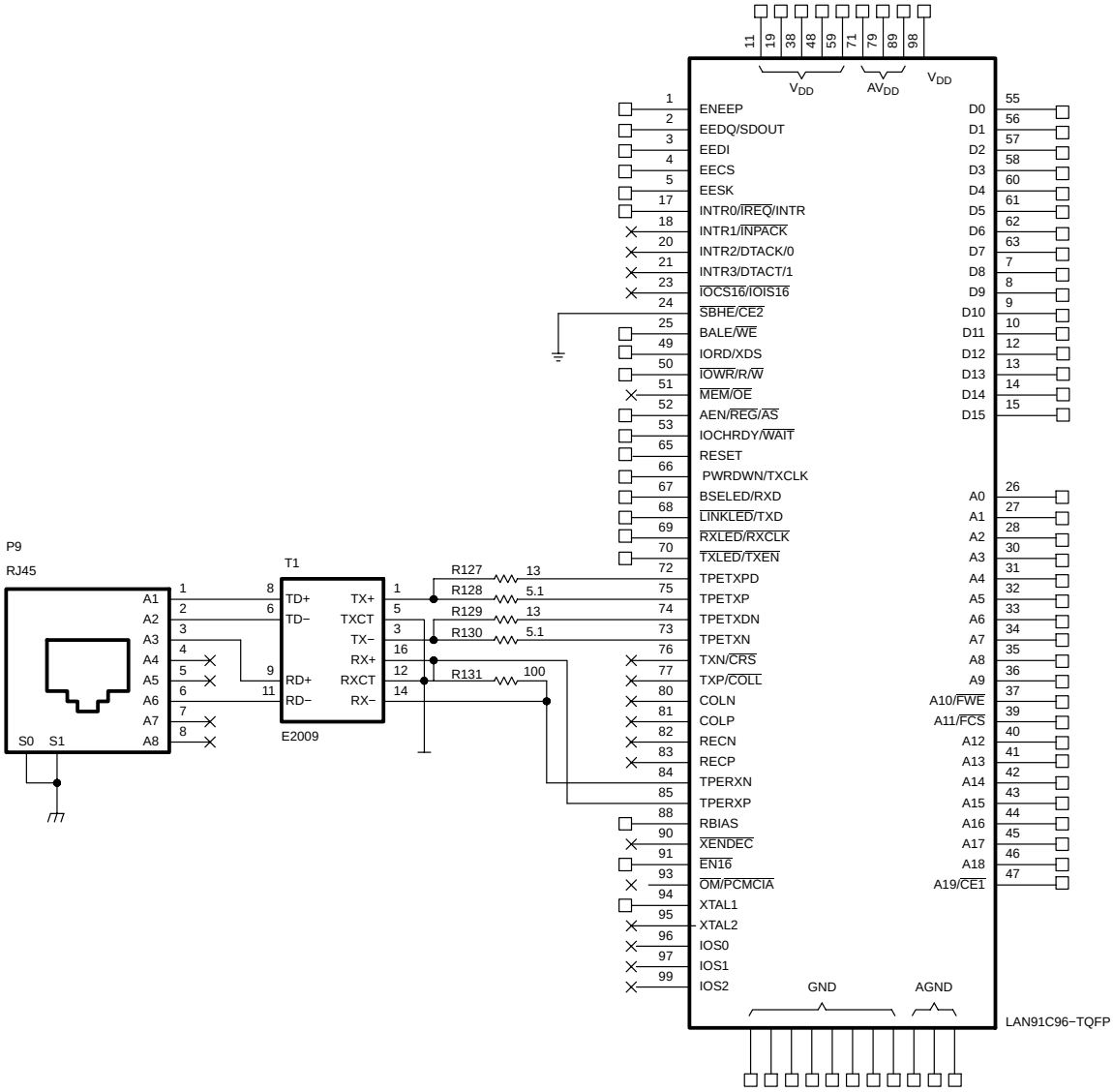
1.12.5 Crystal

An external 20 MHZ crystal is used to supply the clock source for the LAN91C96. The crystal was chosen as a lower cost option.

1.12.6 Output Section

Figure 1−36 shows the design of the output section of the Ethernet circuitry.

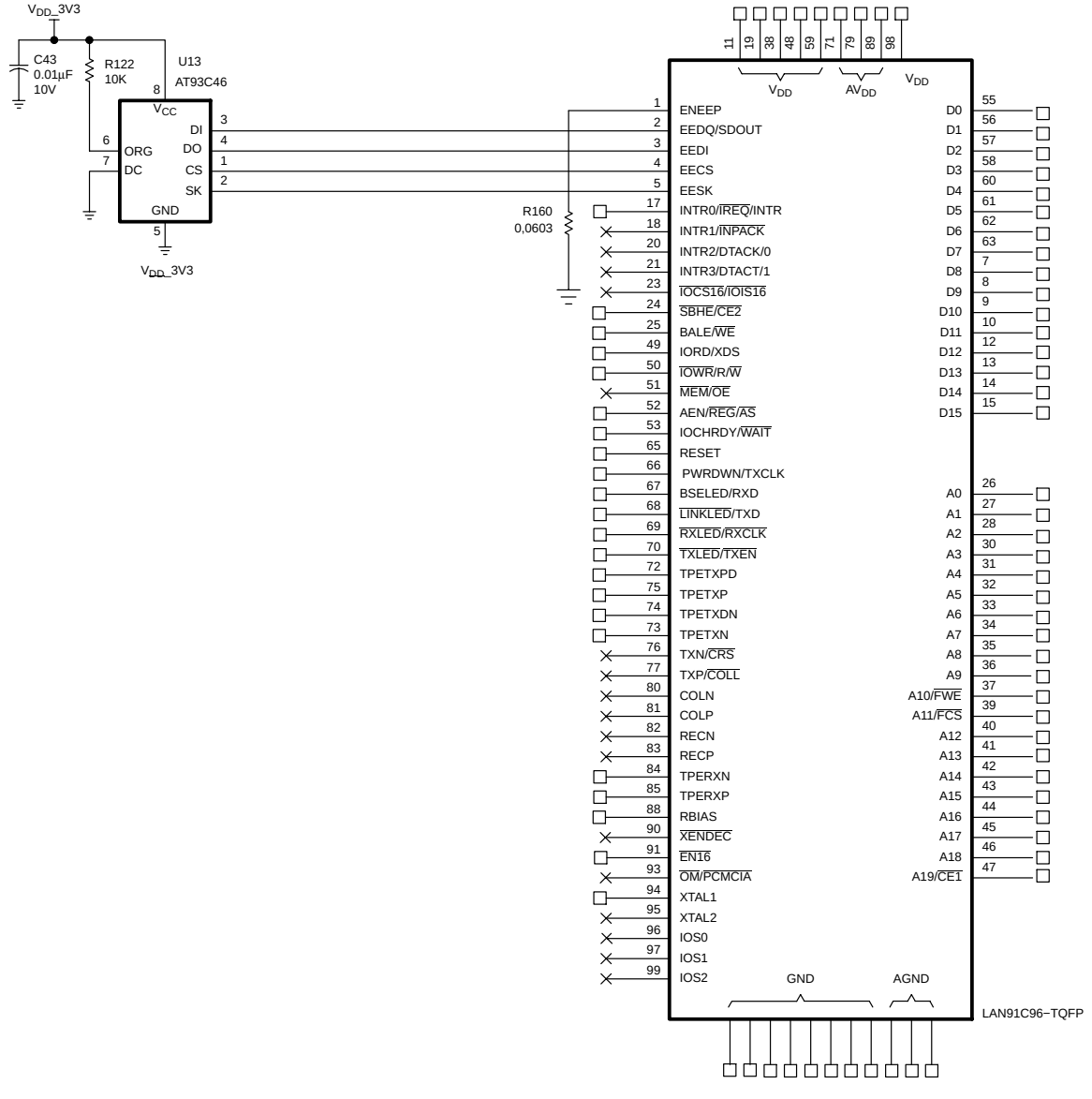
Figure 1−36. Ethernet Output Section



1.12.7 EEPROM

Figure 1−37 is the interface between the EEPROM and the LAN91C96 Ethernet Controller.

Figure 1−37. Ethernet EEPROM



The LAN91C96 has the ability to retrieve configuration information from a serial EEPROM on reset or power-up. The serial EPROM acts as storage of configuration and IEEE Ethernet address information.

The device used is the AT93C46™ EEPROM from Atmel Corporation. The AT93C46 provides 1024 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 64 words of 16 bits each. The ORG pin is pulled high, which controls the bit configuration.

Pin 1 on the LAN91C96 is the EEPROM enabled pin. It has an internal pull-up in the LAN91C96. If the EEPROM is not to be used, then R160 must be populated. The default is that R160 is not installed. Power for the AT93C46 is provided by the 3.3 V voltage rail, which is the same rail as is used by the LAN91C96.

1.12.8 Status LEDS

There are four status LEDS on the LAN91C96 device. Table 1−13 defines the meaning of each LED and the corresponding color for each LED and how each of the status LEDS are used by the LANC9196.

Table 1−13. Ethernet Status LEDs

LED	Function
TX	Activated by transmit activity.
RX	Activated by receive activity.
LINK	Reflects the link integrity status.
BSE	Board select LED. Activated when the board space is accessed, namely on accesses to the LAN91C96 register space or the ROM area decoded by the LAN91C96. The signal is stretched to 125 ms.

Chapter 2

Expansion Connectors

This section defines the type and pinout of the expansion connectors for the system. In order to insure proper operation of the system, the functions of each pin on the connector are static. Not all pins on the connectors are used by all processors.

A lot of the pins have multiple functions that they can perform. All of the expansion cards have access to all of the functions found on each pin if needed. The default naming convention does not show any additional functions in the name; however, the additional functions are defined in the *OMAP5912 Applications Processor* (literature number SPRS231) data sheet. If certain signals are used by the OMAP5912 target module in something other than the default mode, this is also indicated. Descriptions for the signals only cover the signal as it is used on the OMAP5912 target module.

The following sections cover each of the four expansion connectors.

Topic **Page**

2.1 Connector A

Connector A contains the Flash Bus and its control signals. It also contains the SD/MMC interface for the OMAP5912. Table 2−1 shows the pinout of the A Connector.

Table 2−1. Connector A Pinout

Name	No.	Name	Name
GND	1	2	GND
GND	3	4	GND
3.3 V	5	6	3.3 V
3.3 V	7	8	3.3 V
	9	10	
MPU_BOOT	11	12	MMC.CMD
MMC.DAT2	13	14	MMC.DAT3
MMC.DAT0	15	16	MMC.DAT1
MMC.CLK	17	18	FLASH.ADV
FLASH.RDY	19	20	FLASH.CLK
FLASH.BE0	21	22	FLASH.BE1
FLASH.WE	23	24	FLASH.WP
FLASH.RP	25	26	FLASH.OE
FLASH.CS3	27	28	FLASH.CS2U
FLASH.CS2	29	30	FLASH.CS1U
FLASH.CS1	31	32	FLASH.D[15]
FLASH.D[14]	33	34	FLASH.D[13]
FLASH.D[12]	35	36	FLASH.D[11]
FLASH.D[10]	37	38	FLASH.D[9]
FLASH.D[8]	39	40	FLASH.D[7]
FLASH.D[6]	41	42	FLASH.D[5]
FLASH.D[4]	43	44	FLASH.D[3]
FLASH.D[2]	45	46	FLASH.D[1]

Table 2−1. Connector A Pinout (Continued)

Name	No.	Name	Name
FLASH.D[0]	47	48	GPIO1
FLASH.A25	49	50	FLASH.A24
FLASH.A23	51	52	FLASH.A22
FLASH.A21	53	54	FLASH.A20
FLASH.A19	55	56	FLASH.A18
FLASH.A17	57	58	FLASH.A16
FLASH.A15	59	60	FLASH.A14
FLASH.A13	61	62	FLASH.A12
FLASH.A11	63	64	FLASH.A10
FLASH.A9	65	66	FLASH.A8
FLASH.A7	67	68	FLASH.A6
FLASH.A5	69	70	FLASH.A4
FLASH.A3	71	72	FLASH.A2
FLASH.A1	73	74	nEX_CS3
nEX_CS4	75	76	FLASH_DIS
GND	77	78	GND
GND	79	80	GND

2.2 Connector B

Expansion Connector B contains the serial buses such as SPI, McBSP, MCSI, and standard serial ports. Table 2−2 shows the pin out of the B connector.

Table 2−2. Expansion Connector B Pin Out

Name	No.		Name
GND	1	2	GND
GND	3	4	GND
DC	5	6	DC
DC	7	8	DC
3.3 V	9	10	3.3 V
3.3 V	11	12	3.3 V
NC	13	14	NC
RTC_WAKE_INT	15	16	MCBSP1.FSX
MCSI1.SYNC	17	18	MCSI1.CLK
MCSI1.DIN	19	20	MCSI1.DOUT
MCSI2.SYNC	21	22	MCSI2.CLK
MCSI2.DIN	23	24	MCCS2.DOUT
BCLK	25	26	MCLK_REQ
BCLK_REQ	27	28	CLK32K_OUT
MCLK	29	30	MCBSP1.DX
MCBSP1.CLKS	31	32	MCBSP1.DR
NC	33	34	NC
MCBSP1.CLKX	35	36	MCBSP2.DR
MCBSP2.FSR	37	38	MCBSP2.CLKX
MCBSP2.DX	39	40	MCBSP2.CLKR
MCBSP2.FSX	41	42	UART3.TX
UART3.RX	43	44	UART1.RTS
UART1.Tx	45	46	UART1.CTS
UART1.RX	47	48	UART2.CTS

Table 2−2. Expansion Connector B Pin Out (Continued)

Name	No.		Name
UART2.TX	49	50	UART2.RX
UART2.RTS	51	52	UART2.BCLK
UART1.DIS	53	54	BFAIL
USB_DM	55	56	RTC_ON_OFF
USB_DP	57	58	USB_PUEN
RESET_IN	59	60	nRESET_OUT
GPIO 4	61	62	GPIO 8
MCBSP3.CLKX	63	64	GPIO 11
MPUI04	65	66	MPUI03
JTAG_DIS	67	68	GPIO62
nTRST	69	70	TMS
TDI	71	72	nEMU0
nEMU1	73	74	TCK
RTCK	75	76	TDO
GND	77	78	GND
GND	79	80	GND

2.3 Connector C

Expansion Connector C contains the camera, LCD, GPIO, I2C, and GPIO pins. Table 2−3 shows the pin out of the C connector.

Table 2−3. Connector C Pin Out

Name	No.		Name
GND	1	2	GND
GND	3	4	GND
DC	5	6	DC
DC	7	8	DC
3.3 V	9	10	3.3 V
3.3 V	11	12	3.3 V
NC	13	14	NC
GPIO7	15	16	GPIO 3
GPIO2	17	18	GPIO 6
GPIO 9	19	20	GPIO 13
GPIO 12	21	22	GPIO 15
GPIO14	23	24	MPUIO2
MPUIO1	25	26	CAM.EXCLK
CAM.D0	27	28	CAM.D1
CAM.D2	29	30	CAM.D3
CAM.D4	31	32	CAM.D5
CAM.D6	33	34	CAM.D7
CAM.LCLK	35	36	CAM.HS
CAM.VS	37	38	CAM.RST
I2C.SDA	39	40	I2C.SCL
LCD.P0	41	42	LCD.P1
LCD.P2	43	44	LCD.P3
LCD.P4	45	46	LCD.P5
LCD.P6	47	48	LCD.P7

Table 2−3. Connector C Pin Out (Continued)

Name	No.		Name
LCD.P8	49	50	LCD.P9
LCD.P10	51	52	LCD.P11
LCD.P12	53	54	LCD.P13
LCD.P14	55	56	LCD.P15
LCD.PCLK	57	58	LCD.AC
LCD.VS	59	60	LCD.HS
KB.C0	61	62	KB.C1
KB.C2	63	64	KB.C3
KB.C4	65	66	KB.C5
KB.R0	67	68	KB.R1
KB.R2	69	70	KB.R3
KB.R4	71	72	UWIRE.SDI
UWIRE.CS0	73	74	UWIRE.CS3
UWIRE.SDO	75	76	UWIRE.SCLK
GND	77	78	GND
GND	79	80	GND

2.4 Connector D

Expansion connector D is mainly reserved for future expansion to allow other cards that meet the OMAP5912 target module form factor, but needs additional signals to be routed to the expansion cards. Table 2−4 shows the pin out of the D connector.

Table 2−4. Expansion Connector D Pin Out

Name	No.		Name
GND	1	2	GND
GND	3	4	GND
DC	5	6	DC
DC	7	8	DC
3.3 V	9	10	3.3 V
3.3 V	11	12	3.3 V
	13	14	
GND	15	16	VLYNQ.TX1
GND	17	18	VLYNQ.TX0
GND	19	20	VLYNQ.CLK
GND	21	22	VLYNQ.RX1
GND	23	24	VLYNQ.RX0
	25	26	
	27	28	
	29	30	
	31	32	
	33	34	
	35	36	
	37	38	
	39	40	
	41	42	
	43	44	

Table 2−4. Expansion Connector D Pin Out (Continued)

Name	No.		Name
	45	46	
	47	48	
	49	50	
	51	52	
	53	54	
	55	56	
	57	58	
	59	60	
	61	62	
	63	64	
	65	66	
	67	68	
	69	70	
	71	72	
	73	74	
	75	76	
GND	77	78	GND
GND	79	80	GND

2.5 Connector Specification

Each expansion connector is a Hirose FX2 series 1.27 mm pitch connector. This is required due to the minimum height restrictions from board to board. This connector and the mating connector give a .484”(12.3 mm) spacing between cards. Figure 2−1 is a picture of the connector.

Figure 2−1. Expansion Connector

Each connector has 2 rows with 40 pins per row. The Hirose part number for the connector is FX2−80P−1.27SV. The target module uses the header part. The connector is a surface mount device. Surface mount connectors are required for the Expansion cards to allow for connectors to be placed on both sides of the board and still be aligned with each other.

Chapter 3

I/O Connectors

This section defines the pin outs of each of the I/O connectors on the OMAP5912 target module.

Topic **Page**

3.1 Serial

Table 3−1 defines the pin out of the DB9 connector on the OMAP5912 target module.

Table 3−1. Serial Connector Pin out

Description	Name	No.		Name	Description
		1	2	RX	Receive Input
Transmit Output	TX	3	4		
Ground	GND	5	6		
		7	8		
			9		

All other pins on the DB9 connector are not connected.

3.2 Ethernet

Table 3−2 defines the pin out of the RJ45 connector.

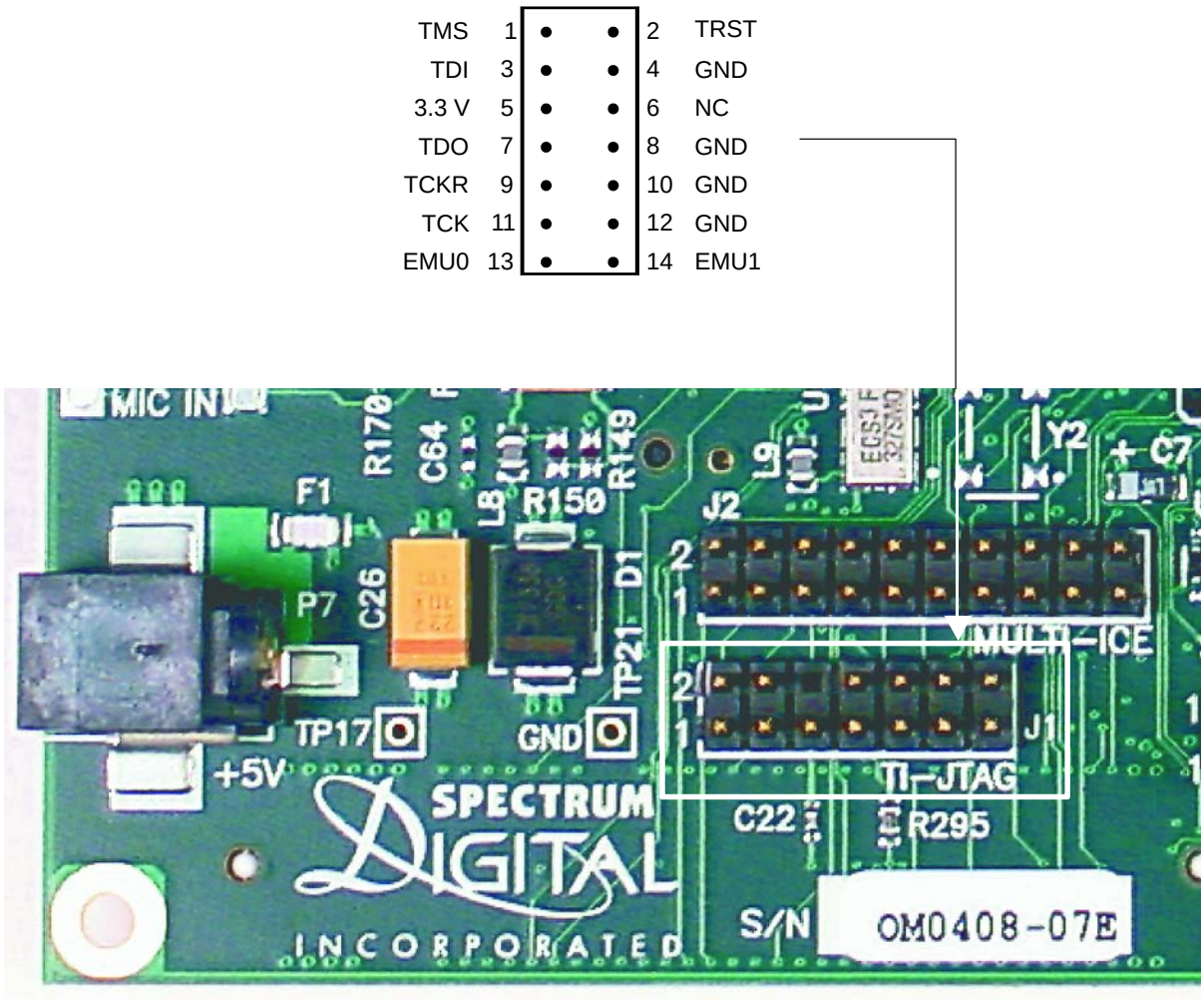
Table 3−2. Ethernet Pin out

No.	Name	Description
1	TX+	Plus side of transmit pair
2	TX−	Minus side of receive pair
3	RX+	Plus side of receive pair
4		
5		
6	RX−	Minus side of receive pair.
7		
8		

3.3 JTAG

Figure 3−1 defines the pin out of the JTAG connector on the OMAP5912 target module.

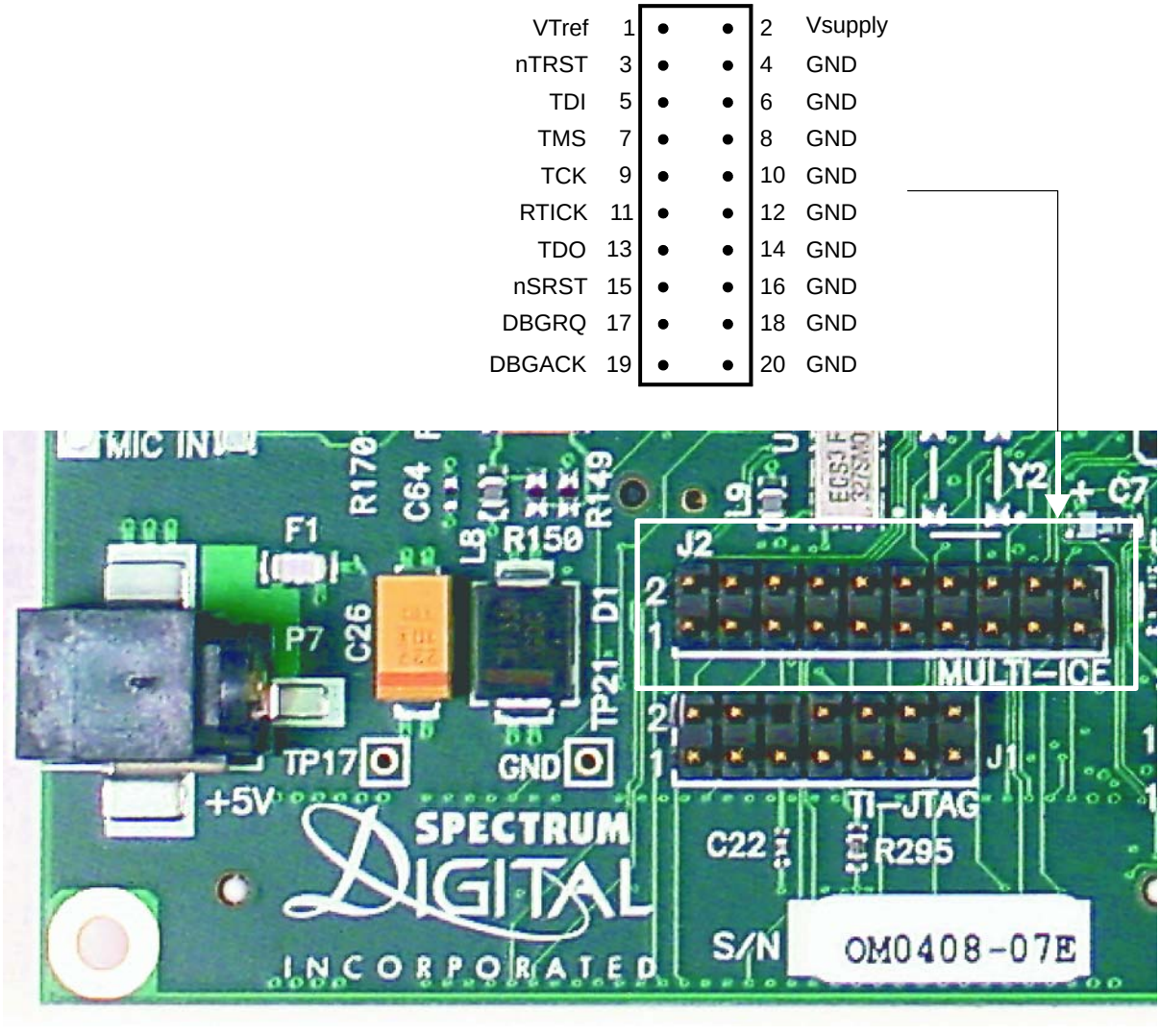
Figure 3−1. JTAG Pinout



3.4 Multi-ICE

Figure 3−2 is the pin out of the Multi-ICE connector.

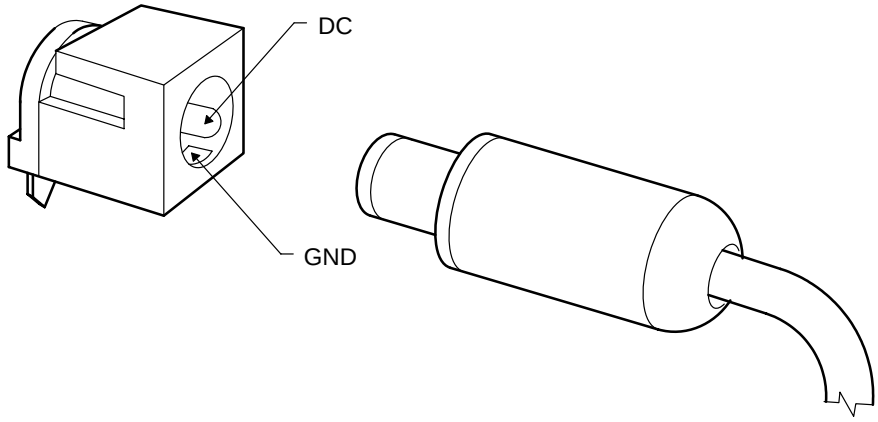
Figure 3−2. Multi-ICE Connector Pin Out



3.5 DC Power

Figure 3−3 shows the pin configuration of the DC connector on the OMAP5912 target module.

Figure 3−3. DC Power Jack Pin Out



3.6 Compact Flash

Table 3−3 is the pin out of the Compact Flash connector.

Table 3−3. Compact Flash Connector Pin Out

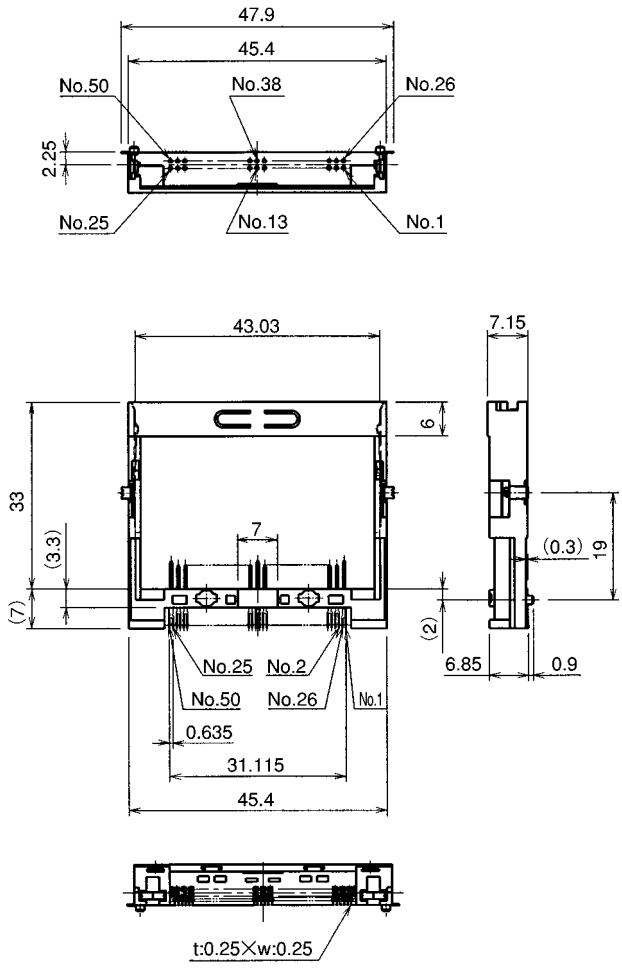
Function						Function	
Mem	I/O		Pin			Mem	I/O
GND		−−−	1	26	−−>	nCD1	
D03		<−>	2	27	<−>	D11	
D04		<−>	3	28	<−>	D12	
D05		<−>	4	29	<−>	D13	
D06		<−>	5	30	<−>	D14	
D07		<−>	6	31	<−>	D15	
nCE1		−−>	7	32	<−−	nCE2	
A10		−−>	8	33	−−>	nVS1	
!OE		−−>	9	34	<−−	NU	nIORD
A09		−−>	10	35	<−−	NU	nIOWR

Table 3−3. Compact Flash Connector Pin Out (Continued)

Function						Function	
Mem	**I/O**		**Pin**			**Mem**	**I/O**
	A08	−−>	11	36	<−−		nWE
	A07	−−>	12	37	−−>	RDY/BSY	IREQ
	VCC	−−−	13	38	−−−		VCC
	A06	−−>	14	39	<−−		nCSEL
	A05	−−>	15	40	−−>		nVS2
	A04	−−>	16	41	<−−		RESET
	A03	−−>	17	42	−−>		nWAIT
	A02	−−>	18	43	−−>	NU	nINPACK
	A01	−−>	19	44	<−−	nREG	
	A00	−−>	20	45	<−>	BVD2(H)	nSPKR
	D00	<−>	21	46	<−>	BVD1(H)	!STSCHG
	D01	<−>	22	47	<−>		D08
	D02	<−>	23	48	<−>		D09
WP	!IOIS16	−−>	24	49	<−>		D10
	nCD2	<−−	25	50	−−−		GND

Figure 3−4 is the mechanicals of the CF connector used on the OMAP5912 target module.

Figure 3−4. Compact Flash Connector



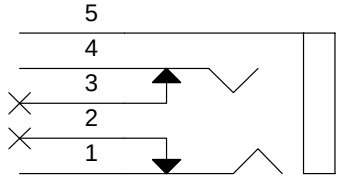
3.7 Headphones

Table 3−4 is the pin out of the headphone jack. Figure 46 gives the locations of the pin numbers.

Table 3−4. Headphone Pin out

Description	Name	No.
Left Channel Out	Left	1
		2
		3
Right Channel Out	Right	4
Ground	GND	5

Figure 3−5. Headphone Pin out



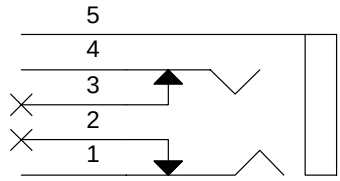
3.8 Line In

Table 3−5 is the pin out of the Lin In jack on the OMAP5912 target module. Figure 3−6 gives the pin out of the connector.

Table 3−5. Line In Pin Out

Description	Name	No.
Left Channel In	Left In	1
		2
		3
Right Channel IN	Right In	4
Ground	GND	5

Figure 3−6. Line In Pin Out



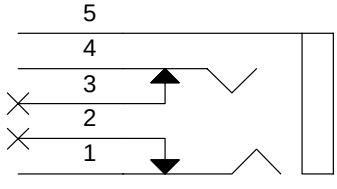
3.9 Microphone In

Table 3−6 is the pin assignments for the Microphone input jack. Figure 3−7 gives the pin out of the connector.

Table 3−6. Microphone Input Pin Out

Description	Name	No.
Ground	GND	1
Microphone In	MIC In	2
		3
		4
		5

Figure 3−7. Microphone Jack Pin Out



3.10 USB Host

Table 3−7 gives the pin out of the USB host connector.

Table 3−7. USB Host Pinout

Description	Name	No.
+ 5 V power output	+ 5 V	1
Negative polarity data	− DATA	2
Positive polarity data	+ DATA	3
Ground	GND	4

3.11 USB Client Adapter

Figure 3−8 is the adapter used to convert the Host interface to the Client interface.

Figure 3−8. USB Client Adapter

This adapter is made by Video Products Inc.

Part Number	Description	UPC Code
USBAF−USBBF	USB Adapter and Gender Changers : USB A Female to B Female Adapter	

It can be purchased at www.vpi.us

Chapter 4

Mechanical Specifications

This section defines the physical requirements for each of the card types.

Topic **Page**

4.1 OMAP5912 Target Module Card

This section defines the mechanical dimensions and configuration of the OMAP5912 target module card. The exact dimensions of the module are subject to change based on the final layout of the PCB. Figure 4−1 gives the general outline and component placement of the OMAP5912 target module from the top side.

Figure 4−1. OMAP5912 Target Module Top Side

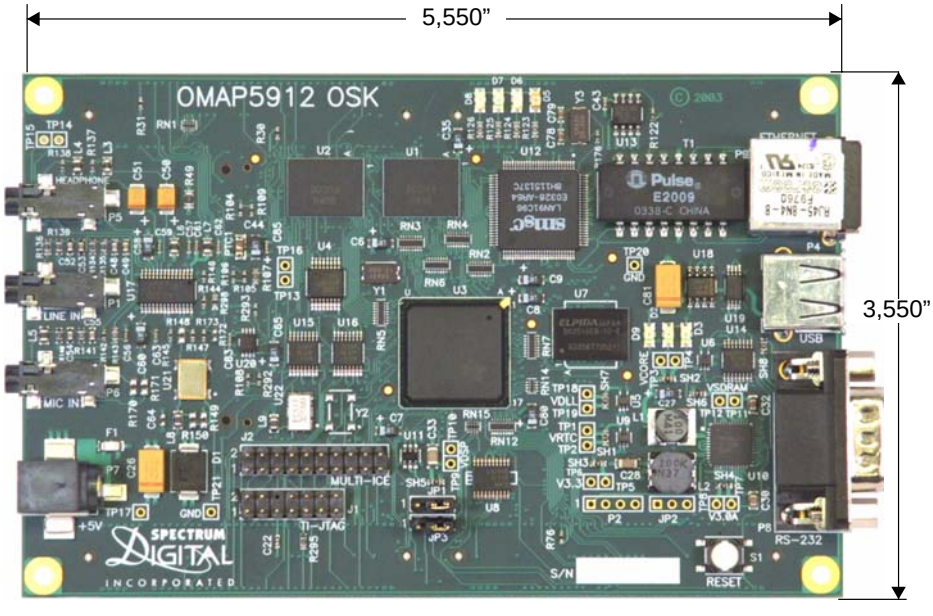
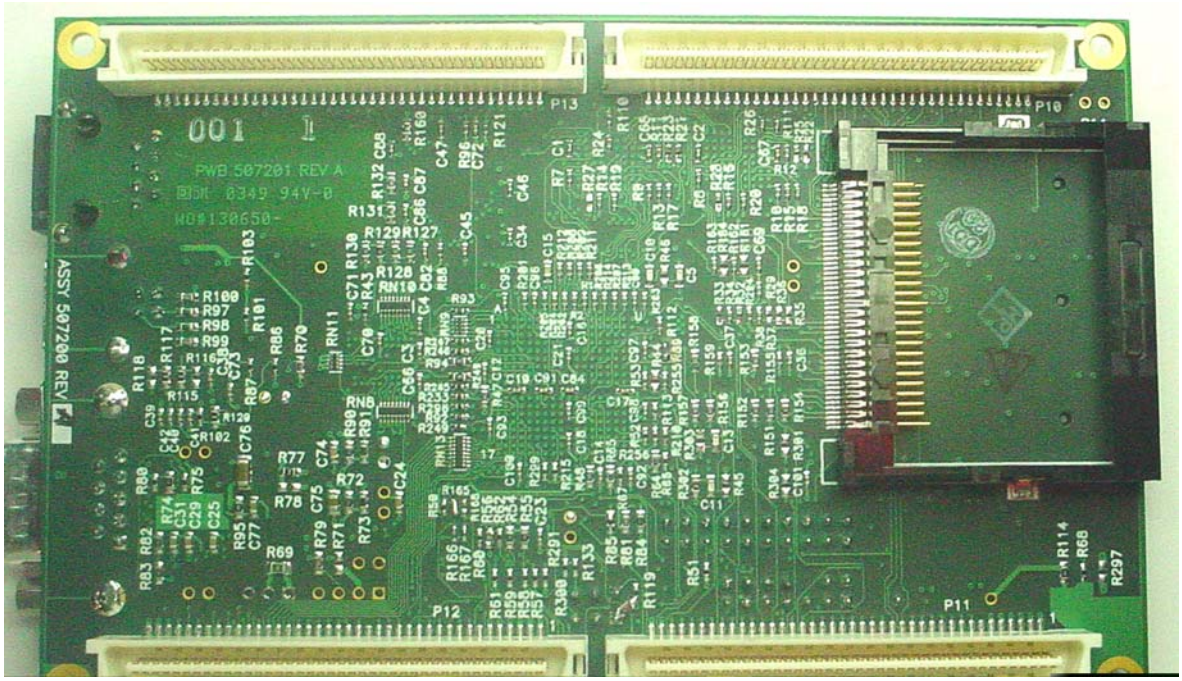


Figure 4−2 shows the OMAP5912 target module from the back side.

Figure 4−2. OMAP5912 Target Module Back Side



Chapter 5

Component Locations

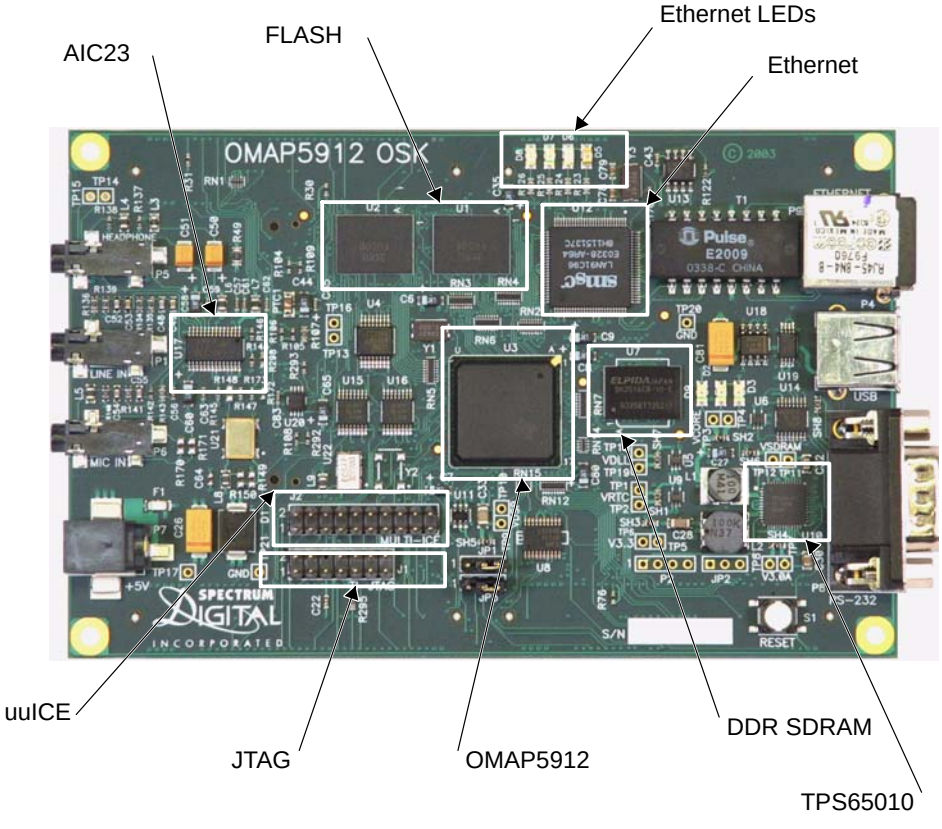
The following sections describe where on the OMAP5912 target module the different components can be found.

Topic **Page**

5.1 Key Components

Figure 5−1 shows the key components on the top side of the OMAP5912 target module.

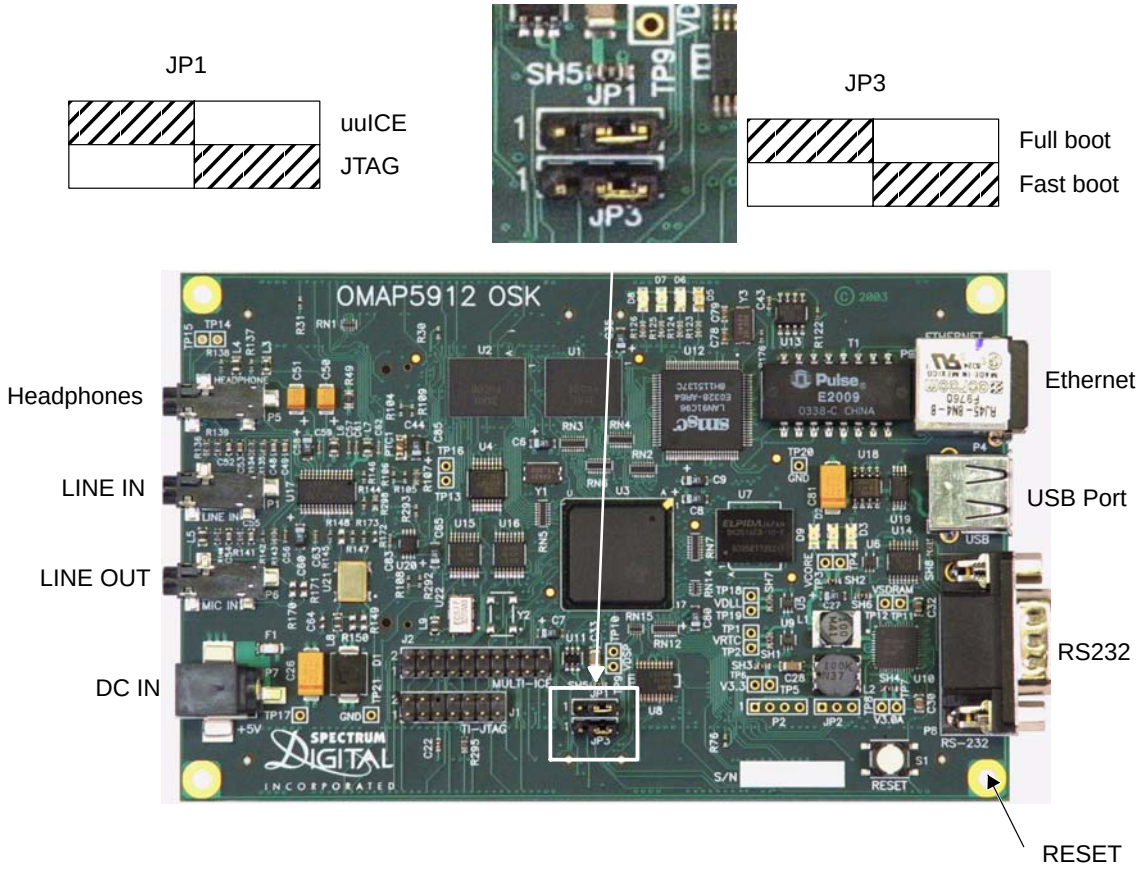
Figure 5−1. OMAP5912 Target Module Key Top Side Components



5.2 Connectors and Jumpers

Figure 5−2 defines the connectors and jumpers for the OMAP5912 target module.

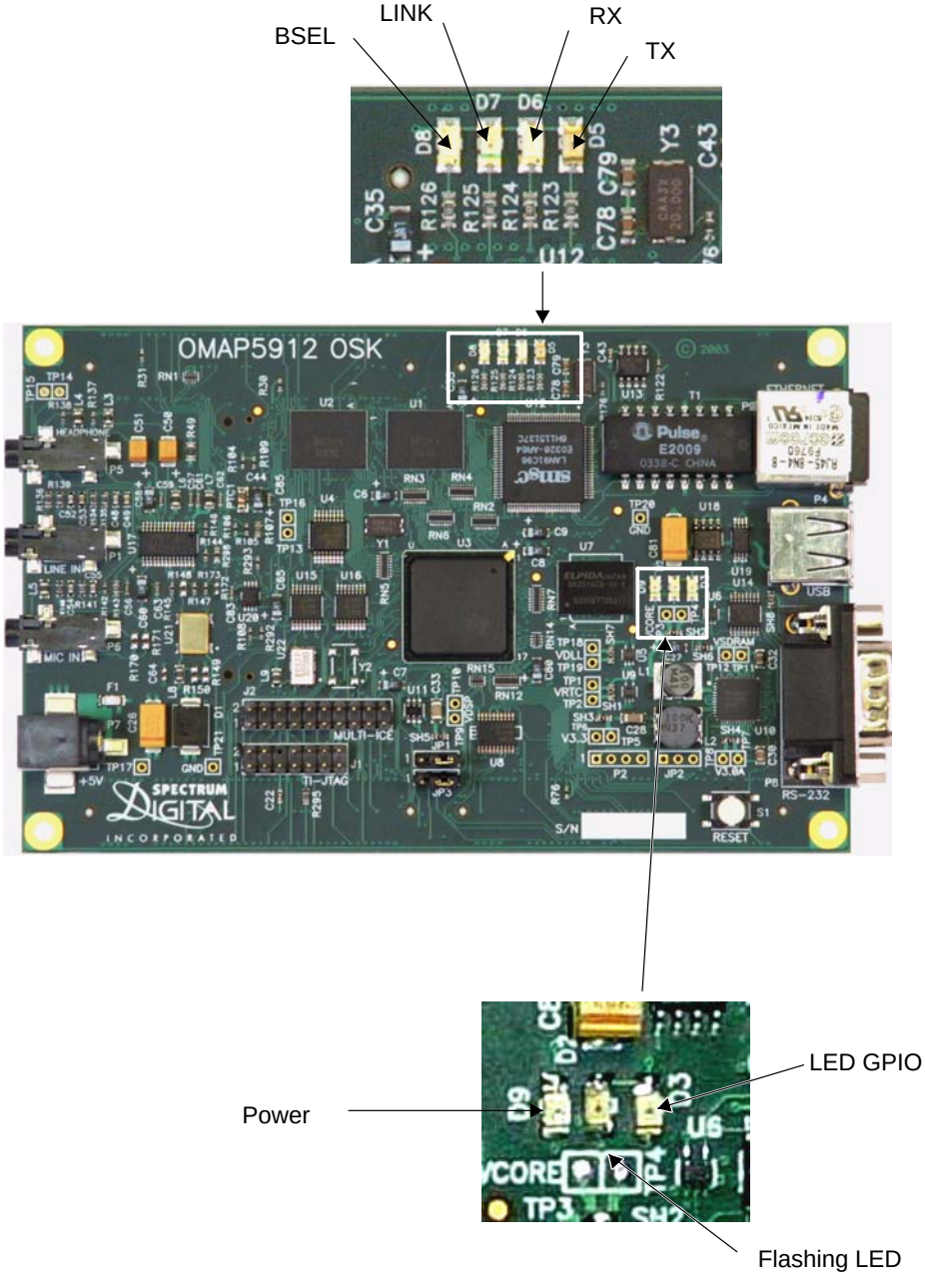
Figure 5−2. OMAP5912 Target Module Connectors



5.3 Indicators

Figure 5−3 shows the placement of the indicators on the OMAP5912 target module.

Figure 5−3. OMAP5912 Target Module Indicators



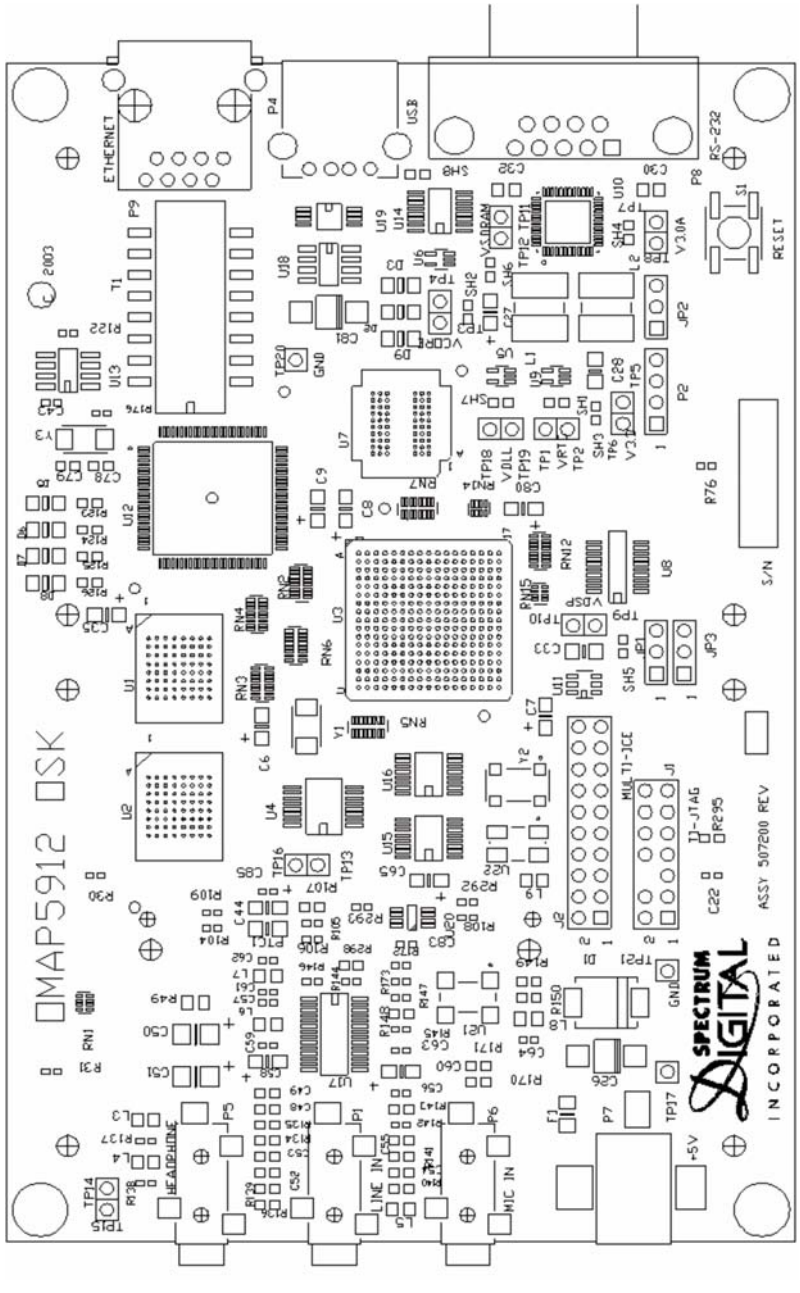
Appendix A

Component Locations

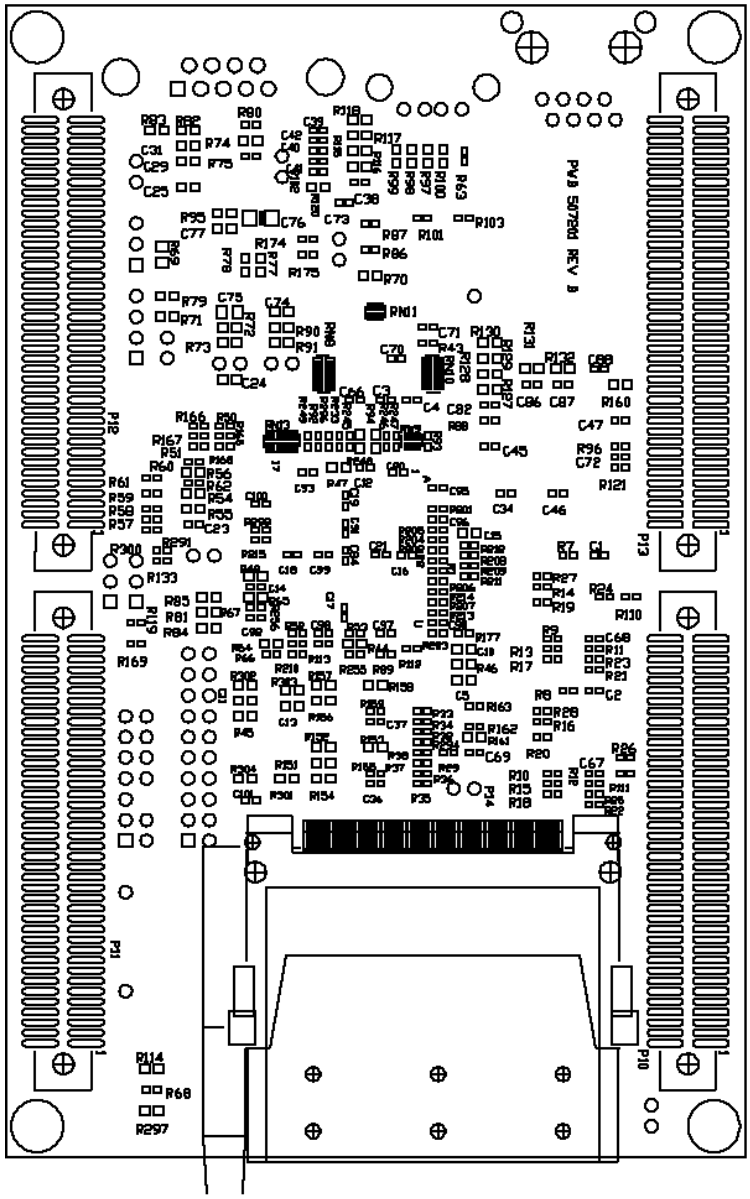
The following figures illustrate the board layouts for the OMAP5912 target module.

Topic **Page**

A.1 Top Side Component Locations

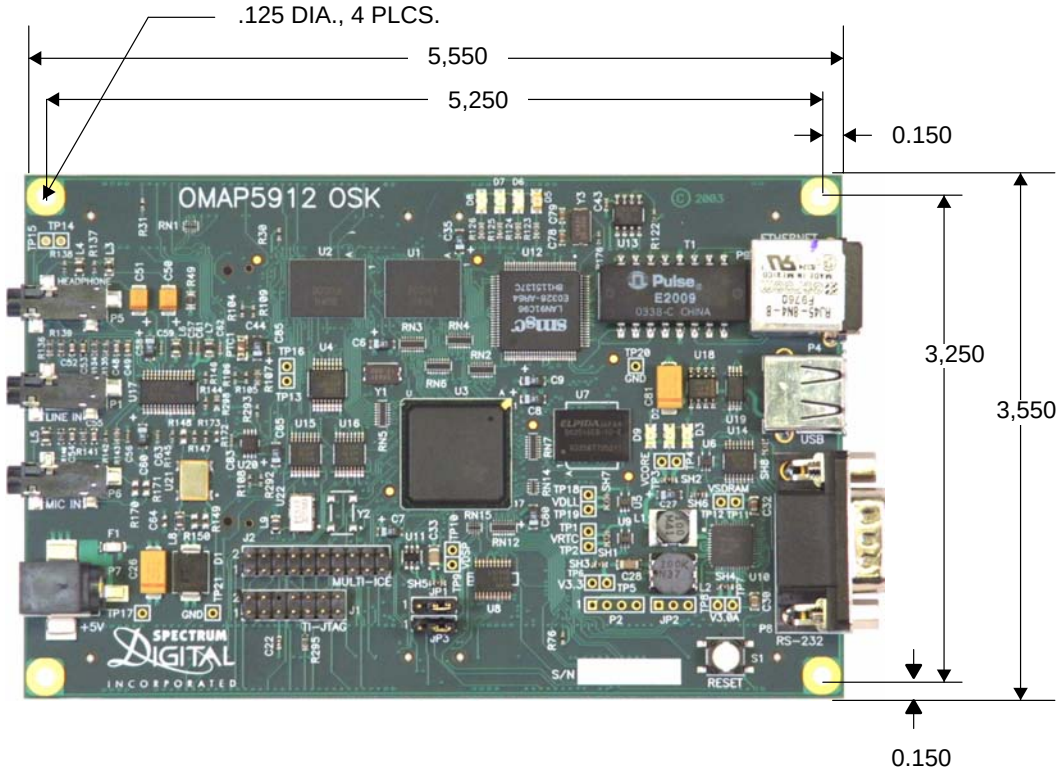


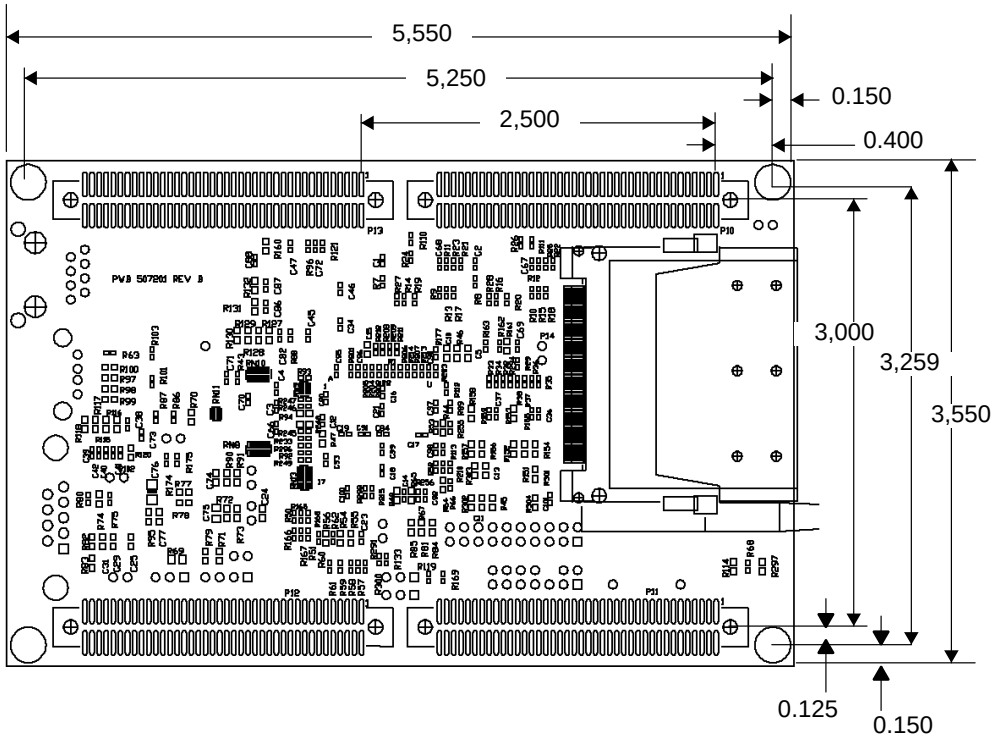
A.2 Bottom Side Component Locations



Appendix B

OMAP5912 Target Module Dimensions




5,550
5,250
2,500
0.150
0.400
3,000
3,259
3,550
0.125
0.150

Appendix C

OMAP5912 Target Module Schematics

This appendix contains the schematics for the OMAP5912 target module.

Version	Date	Author	Notes
A	5/11/04	G. Coley	Revision A release.
A1	7/26/04	G. Coley	Updated Symbol to official symbol. Make corrections for a few typos.

NOTES:

1. All resistors are in the 0402 package unless otherwise specified.
2. There is an ESD ring around the outer edges of the board on the top and bottom side.
3. The ESD ring is connected to the standoffs and extends around the edge of the board.

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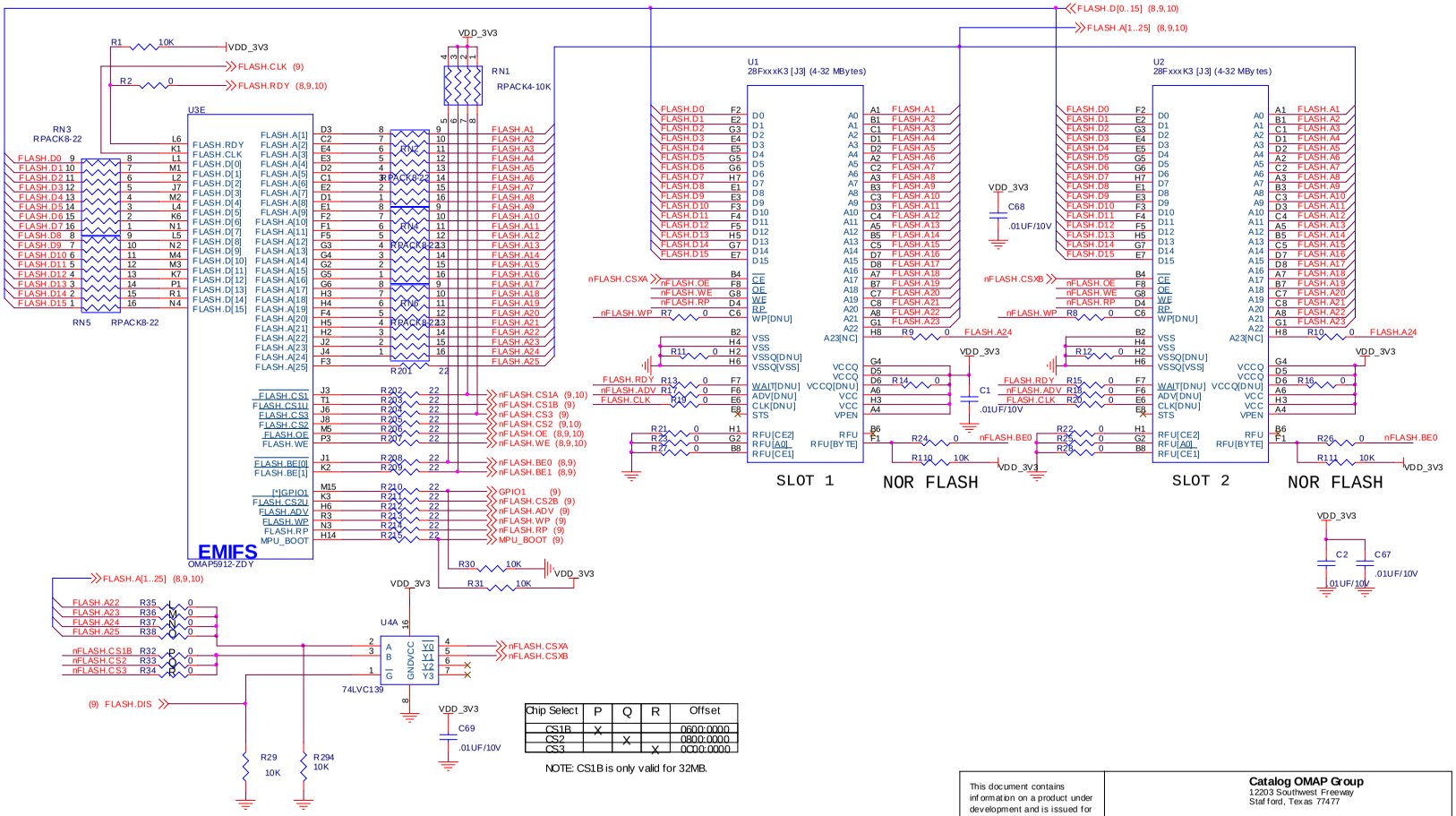
Title : OMAP5912 Starter Kit
Notes Page

Size	Document Number	Modified by:	Rev
B		G. Coley	A1

Date: Monday, July 26, 2004 Sheet 1 of 10


U1
28FxxxK3 [J3] (4-32 MBytes)
SLOT 1
NOR FLASH
U2
28FxxxK3 [J3] (4-32 MBytes)
SLOT 2
NOR FLASH
U3E
EMIFS
OMAP5912-ZDY
U4A
74LVC139
RN1
RPACK4-10K
RN3
RPACK8-22
RN5
RPACK8-22
FLASH.D[0..15] (8,9,10)
FLASH.A[1..25] (8,9,10)
FLASH.CLK (9)
FLASH.RDY (8,9,10)
VDD_3V3
nFLASH.CSXA
nFLASH.CSXB
nFLASH.OE
nFLASH.WE
nFLASH.RP
nFLASH.WP
FLASH.RDY
nFLASH.ADV
FLASH.CLK
nFLASH.BE0
nFLASH.BE1
nFLASH.CS1A (9,10)
nFLASH.CS1B (9)
nFLASH.CS3 (9)
nFLASH.CS2 (9,10)
nFLASH.OE (8,9,10)
nFLASH.WE (8,9,10)
GPIO1 (9)
nFLASH.CS2B (9)
nFLASH.ADV (9)
nFLASH.WP (9)
nFLASH.RP (9)
MPU_BOOT (9)
(9) FLASH.DIS
Chip Select
P
Q
R
Offset
CS1B
CS2
CS3
0600:0000
0800:0000
0C00:0000
NOTE: CS1B is only valid for 32MB.
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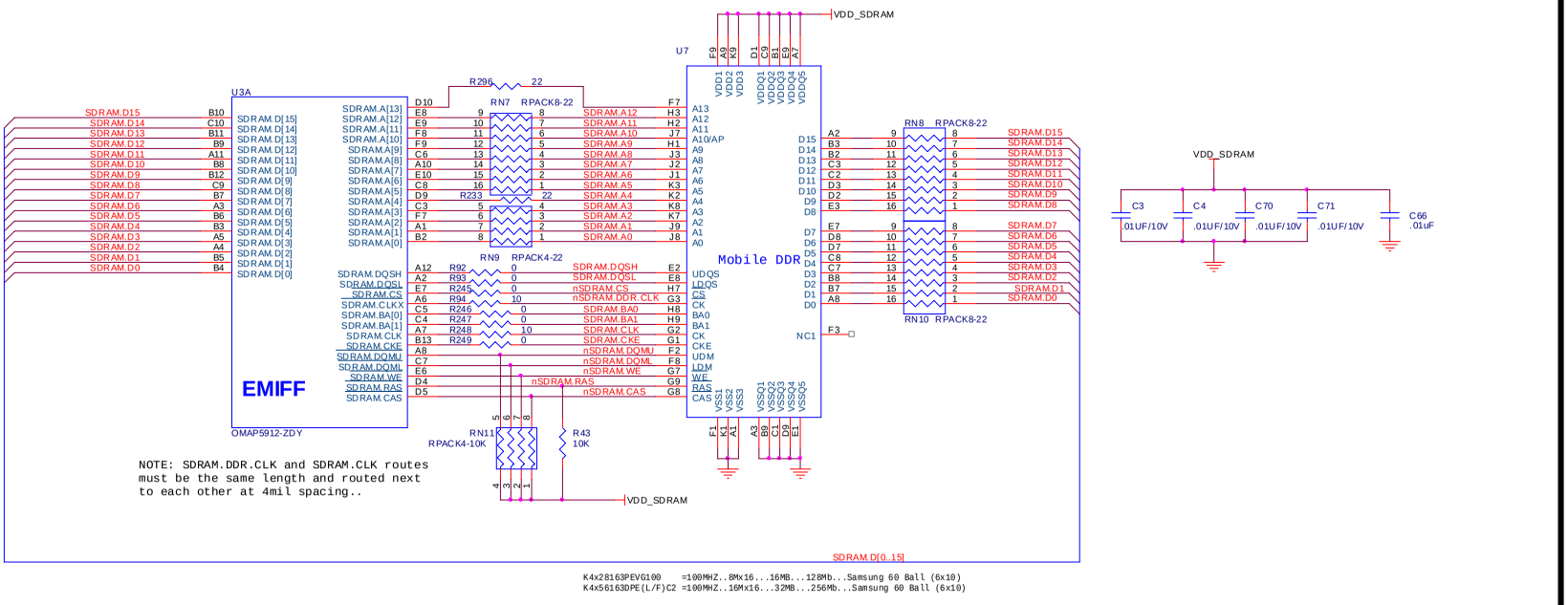
Title : OMAP5912 Starter Kit
NOR Flash Memory
Size B
Document Number <Doc>
Modified by: G. Coley
Rev A1
Date: Monday, July 26, 2004
Sheet 2 of 10



K4x28163PEVG100 =100MHZ..8Mx16...16MB...128Mb...Samsung 60 Ball (6x10)
K4x56163DPE(L/F)C2 =100MHZ..16Mx16...32MB...256Mb...Samsung 60 Ball (6x10)

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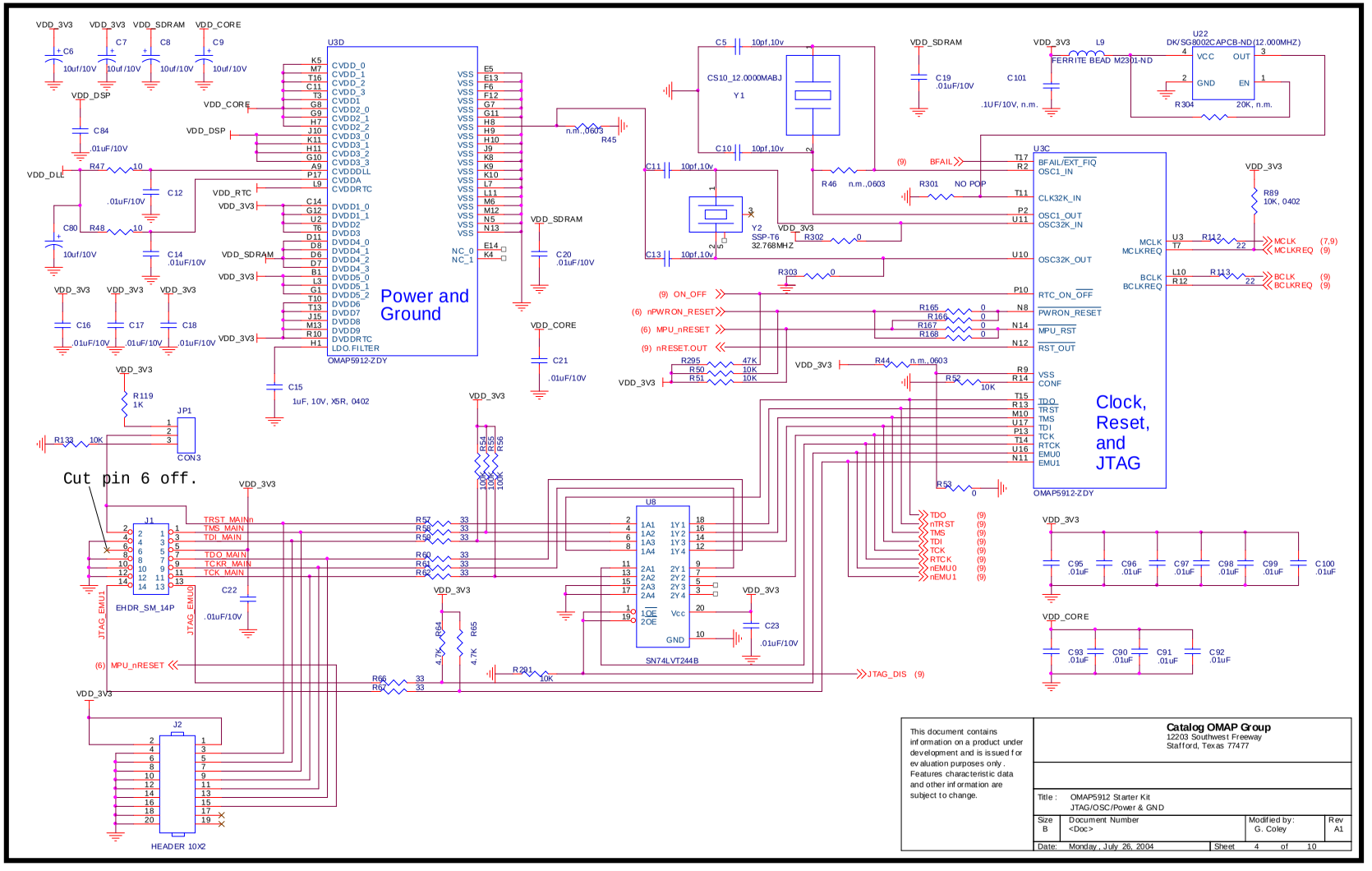
DDR SDRAM

Size	Document Number	Modified by :	Rev
B	<Doc>	G. Coley	A1

Date: Monday, July 26, 2004 Sheet 3 of 10


Power and Ground
Clock, Reset, and JTAG
OMAP5912-ZDY
Cut pin 6 off.
EHDR_SM_14P
SN74LVT244B
HEADER 10X2
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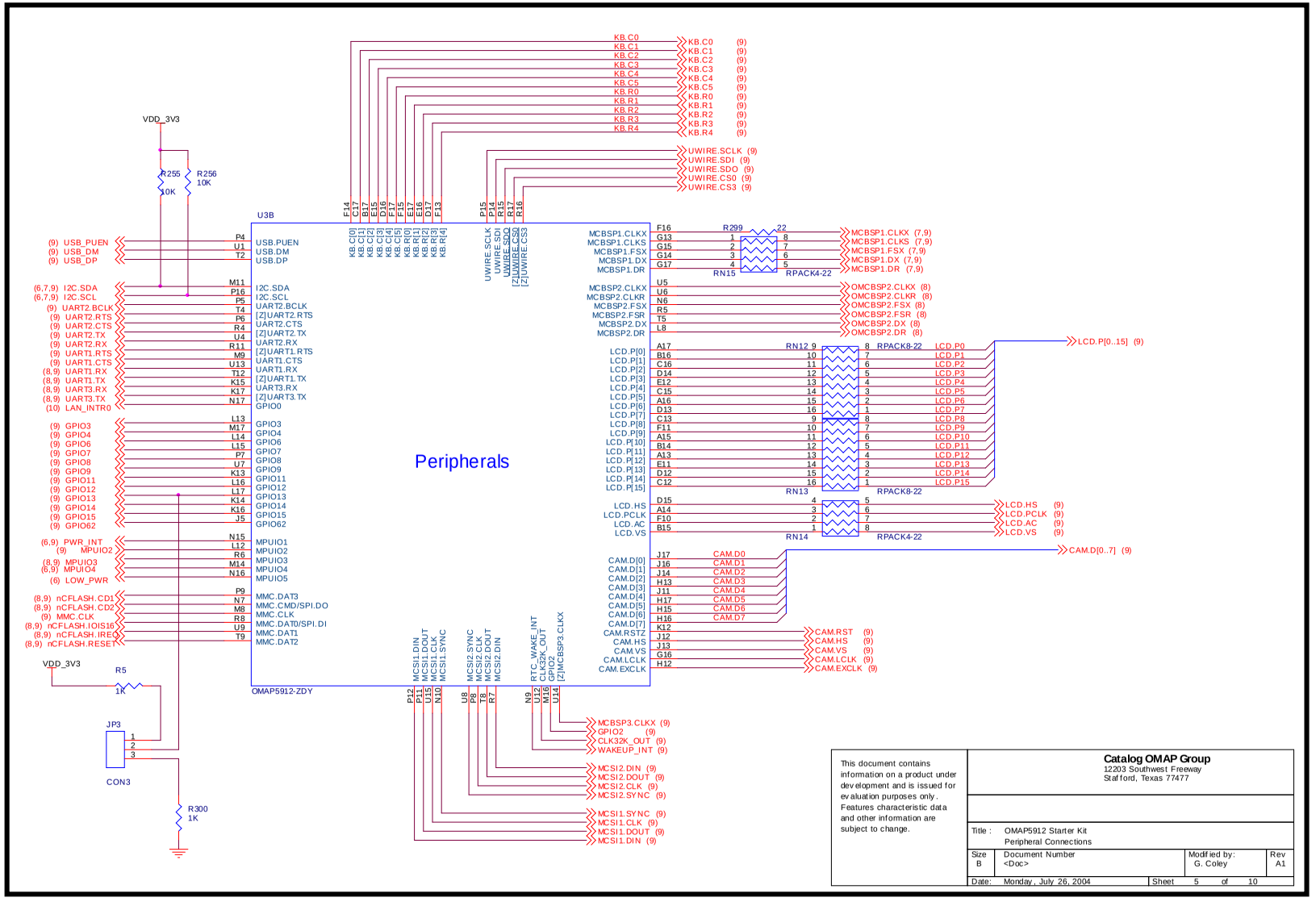
Title : OMAP5912 Starter Kit
JTAG/OSC/Power & GND
Size B
Document Number <Doc>
Modified by: G. Coley
Rev A1
Date: Monday, July 26, 2004
Sheet 4 of 10


Peripherals
U3B
OMAP5912-ZDY
VDD_3V3
R255 10K
R256 10K
R5 1K
R300 1K
JP3
CON3
KB.C0 (9)
KB.C1 (9)
KB.C2 (9)
KB.C3 (9)
KB.C4 (9)
KB.C5 (9)
KB.R0 (9)
KB.R1 (9)
KB.R2 (9)
KB.R3 (9)
KB.R4 (9)
UWIRE.SCLK (9)
UWIRE.SDI (9)
UWIRE.SDO (9)
UWIRE.CS0 (9)
UWIRE.CS3 (9)
USB.PUEN (9)
USB.DM (9)
USB.DP (9)
I2C.SDA (6,7,9)
I2C.SCL (6,7,9)
UART2.BCLK (9)
UART2.RTS (9)
UART2.CTS (9)
UART2.TX (9)
UART2.RX (9)
UART1.RTS (9)
UART1.CTS (9)
UART1.RX (8,9)
UART1.TX (8,9)
UART3.RX (8,9)
UART3.TX (8,9)
LAN_INTR0 (10)
GPIO3 (9)
GPIO4 (9)
GPIO6 (9)
GPIO7 (9)
GPIO8 (9)
GPIO9 (9)
GPIO11 (9)
GPIO12 (9)
GPIO13 (9)
GPIO14 (9)
GPIO15 (9)
GPIO62 (9)
PWR_INT (6,9)
MPUIO2 (9)
MPUIO3 (8,9)
MPUIO4 (6,9)
LOW_PWR (6)
nCFLASH.CD1 (8,9)
nCFLASH.CD2 (8,9)
MMC.CLK (9)
nCFLASH.IOIS16 (8,9)
nCFLASH.IREQ (8,9)
nCFLASH.RESET (8,9)
MCBSP1.CLKX (7,9)
MCBSP1.CLKS (7,9)
MCBSP1.FSX (7,9)
MCBSP1.DX (7,9)
MCBSP1.DR (7,9)
MCBSP2.CLKX (8)
MCBSP2.CLKR (8)
MCBSP2.FSX (8)
MCBSP2.FSR (8)
MCBSP2.DX (8)
MCBSP2.DR (8)
LCD.P[0..15] (9)
LCD.HS (9)
LCD.PCLK (9)
LCD.AC (9)
LCD.VS (9)
CAM.D[0..7] (9)
CAM.RST (9)
CAM.HS (9)
CAM.VS (9)
CAM.LCLK (9)
CAM.EXCLK (9)
MCBSP3.CLKX (9)
GPIO2 (9)
CLK32K_OUT (9)
WAKEUP_INT (9)
MCSI2.DIN (9)
MCSI2.DOUT (9)
MCSI2.CLK (9)
MCSI2.SYNC (9)
MCSI1.SYNC (9)
MCSI1.CLK (9)
MCSI1.DOUT (9)
MCSI1.DIN (9)
RN15 RPACK4-22
RN13 RPACK8-22
RN14 RPACK4-22
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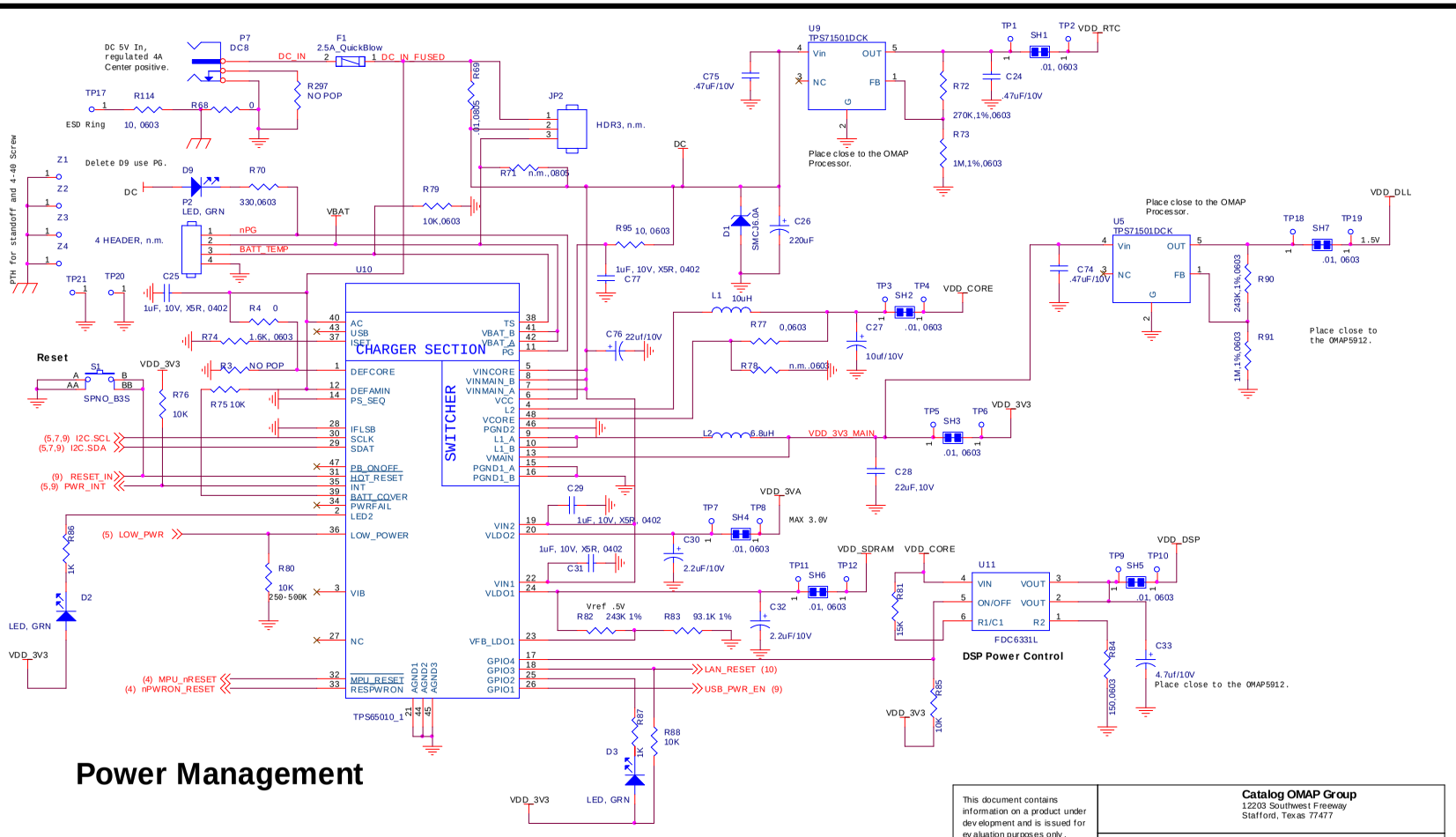
Title : OMAP5912 Starter Kit
Peripheral Connections
Size B
Document Number <Doc>
Modified by: G. Coley
Rev A1
Date: Monday, July 26, 2004
Sheet 5 of 10



Power Management

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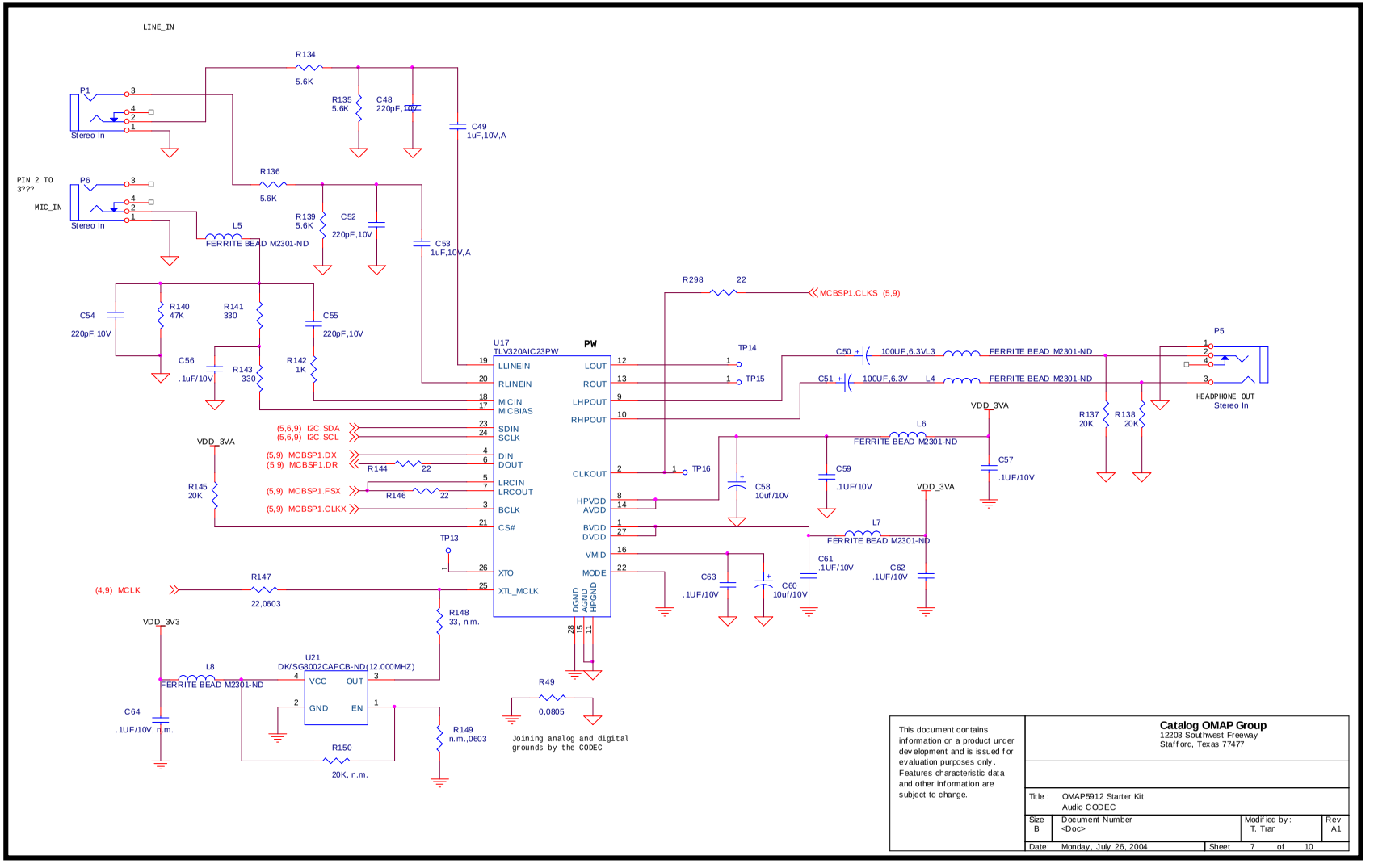
Title :	OMAP5912 Starter Kit Power Management		
Size B	Document Number <Doc>	Modified by : G. Coley	Rev A1
Date: Monday , July 26, 2004		Sheet 6 of 10	



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Title : OMAP5912 Starter Kit
Audio CODEC

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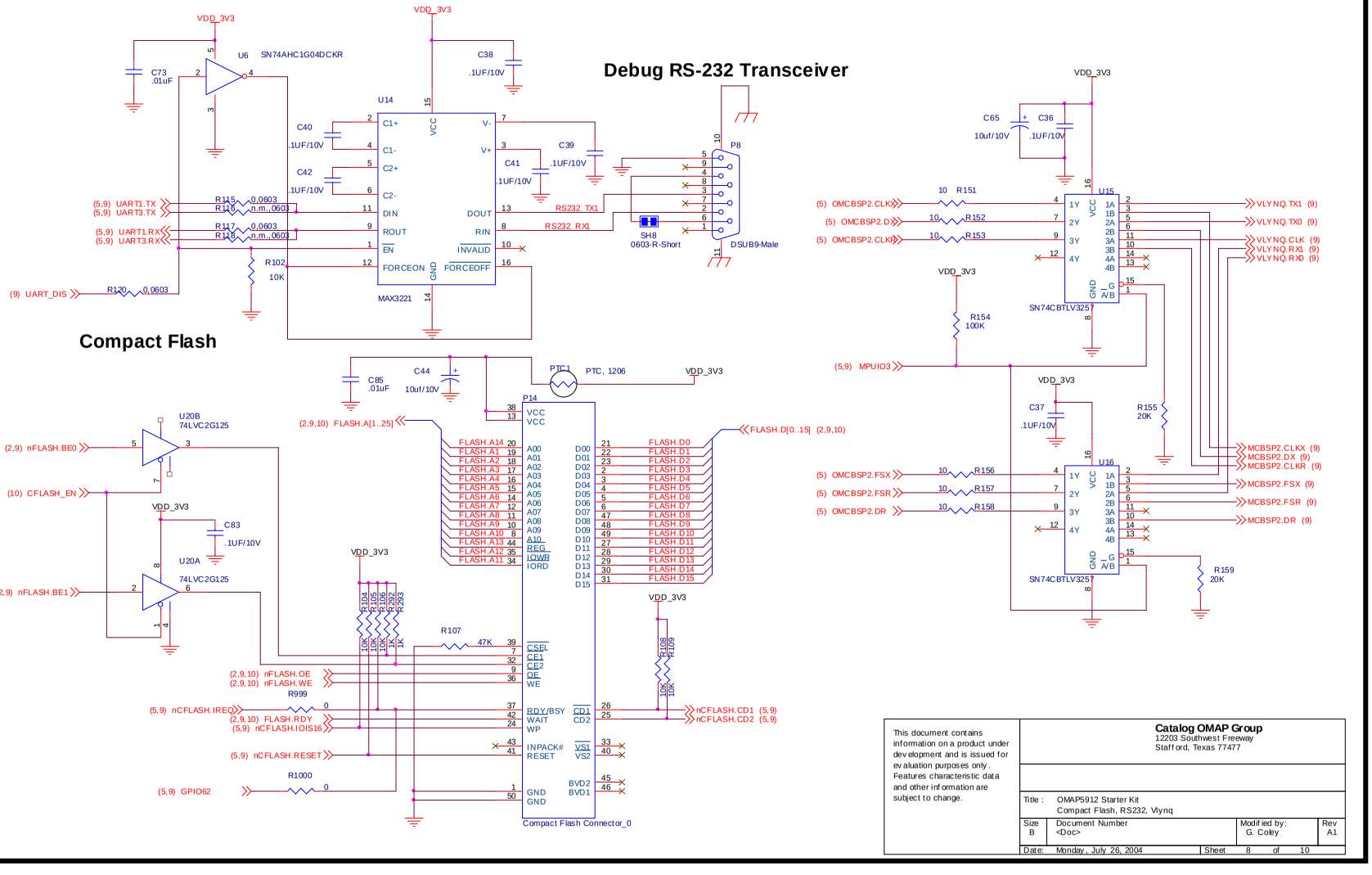
B	<Doc>	T. Tran	A1

Date: Monday, July 26, 2004 Sheet 7 of 10


Debug RS-232 Transceiver
Compact Flash
U6 SN74AHC1G04DCKR
U14 MAX3221
P8 DSUB9-Male
SH8 0603-R-Short
U15 SN74CBTLV3257
U16 SN74CBTLV3257
U20A 74LVC2G125
U20B 74LVC2G125
P14 Compact Flash Connector_0
PTC1 PTC, 1206
VDD_3V3
(5,9) UART1.TX
(5,9) UART3.TX
(5,9) UART1.RX
(5,9) UART3.RX
(9) UART_DIS
RS232_TX1
RS232_RX1
(5) OMCBSP2.CLK
(5) OMCBSP2.D
(5) OMCBSP2.CLKR
(5) OMCBSP2.FSX
(5) OMCBSP2.FSR
(5) OMCBSP2.DR
(5,9) MPUIO3
VLYNQ.TX1 (9)
VLYNQ.TX0 (9)
VLYNQ.CLK (9)
VLYNQ.RX1 (9)
VLYNQ.RX0 (9)
MCBSP2.CLKX (9)
MCBSP2.DX (9)
MCBSP2.CLKR (9)
MCBSP2.FSX (9)
MCBSP2.FSR (9)
MCBSP2.DR (9)
(2,9) nFLASH.BE0
(2,9) nFLASH.BE1
(10) CFLASH_EN
(2,9,10) FLASH.A[1..25]
FLASH.D[0..15] (2,9,10)
(2,9,10) nFLASH.OE
(2,9,10) nFLASH.WE
(2,9,10) FLASH.RDY
(5,9) nCFLASH.IREQ
(5,9) nCFLASH.IOIS16
(5,9) nCFLASH.RESET
(5,9) GPIO62
nCFLASH.CD1 (5,9)
nCFLASH.CD2 (5,9)
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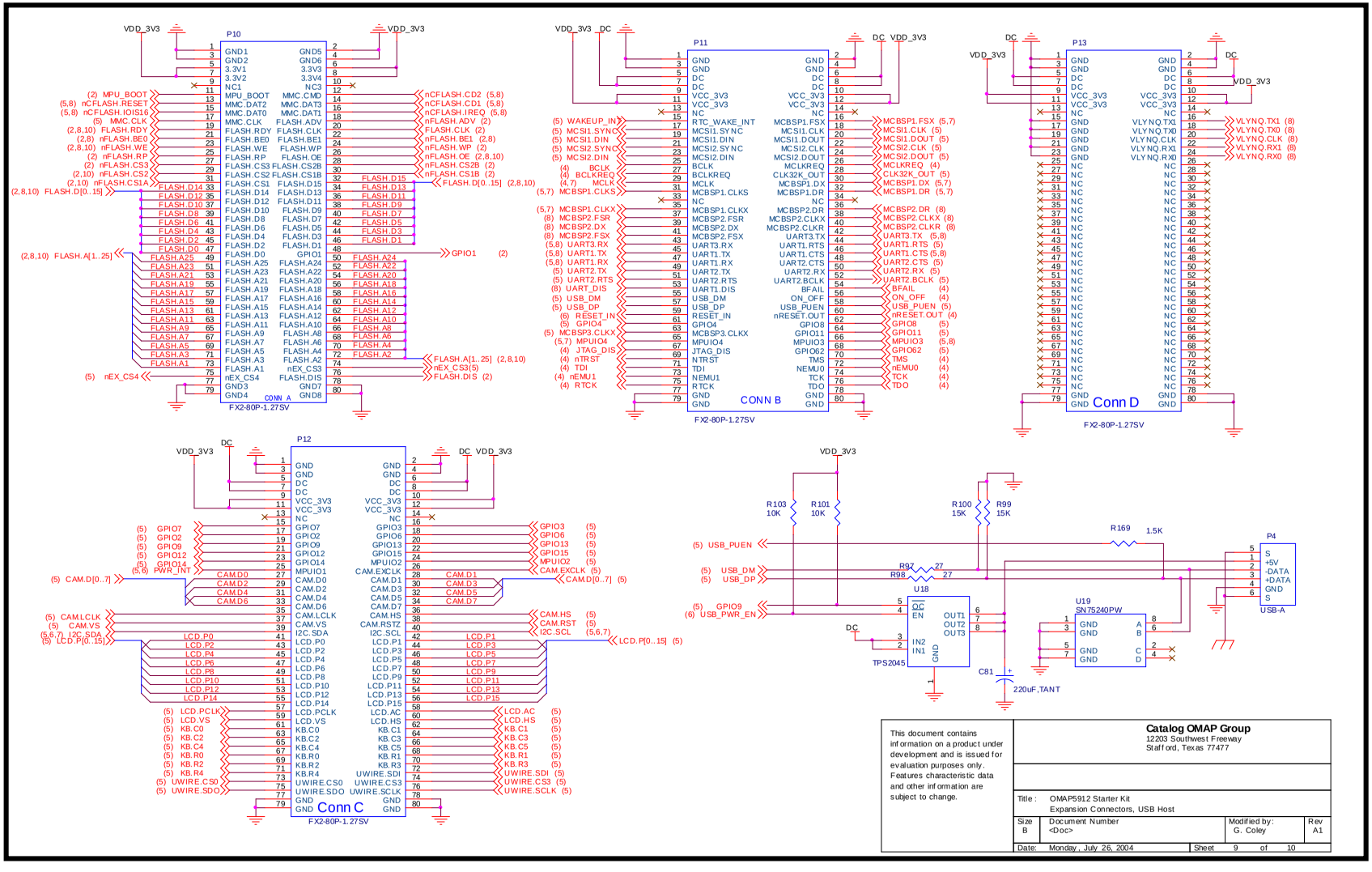
Stafford, Texas 77477
Title : OMAP5912 Starter Kit
Compact Flash, RS232, Vlynq
Size B
Document Number <Doc>
Modified by: G. Coley
Rev A1
Date: Monday, July 26, 2004
Sheet 8 of 10



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Title : OMAP5912 Starter Kit
Expansion Connectors, USB Host

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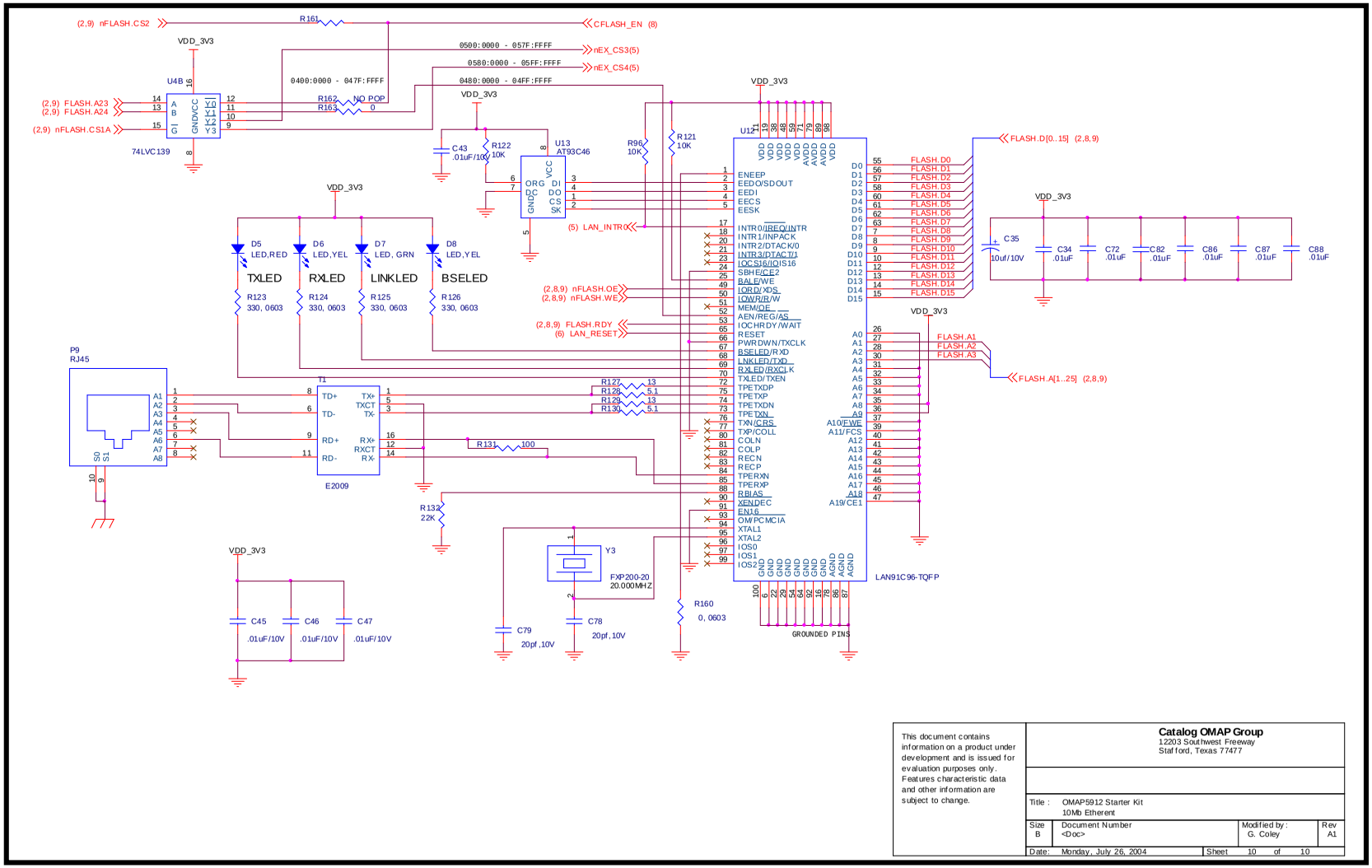
B	<Doc>	G. Coley	A1

Date: Monday, July 26, 2004 Sheet 9 of 10



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Title : OMAP5912 Starter Kit
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Size	Document Number	Modified by :	Rev
B	<Doc>	G. Coley	A1

Date: Monday, July 26, 2004 Sheet 10 of 10

Appendix D

Current Measurement Procedures

This appendix describes how to use the test points on the OMAP5912 target module to take current measurements for each of the voltage rails.

D.1 Basic Principle

The basic concept is measuring the voltage drop across a .1 Ω resistor to determine the total current consumed. This technique is voltage level independent. The formula used to determine the current is:

Voltage Drop /resistor = Current (ma)

The table below shows the measured voltage drop across a .1 Ω resistor for each of the subsequent current flows:

Voltage Drop	Current(ma)
.0001	1
.001	10
.05	50
.01	100
.02	200
.05	500
.1	1000

The reason such a small value has been chosen is to do the following:

- ❏ Limit the power
- ❏ Limit the size of the resistor
- ❏ Limit the voltage drop to a point where it minimizes the impact on the actual voltage level

D.2 Basic Measuring Techniques

Care must be taken to minimize the impact on the operation of the circuitry on the voltage rails while taking the measurements. There are two basic ways in which the voltage drop across the resistors can be measured without impacting the operation of the circuit:

- ❏ Mill volt Voltmeter
  - ■ Good for steady state current readings
  - ■ Poor response to current changes
- ❏ Oscilloscope
  - ■ Good for real-time measurement
  - ■ Good for storage of the data
  - ■ Good response to current changes

D.3 Connection Methods

Following are the connection methods and setup for each of these methods.

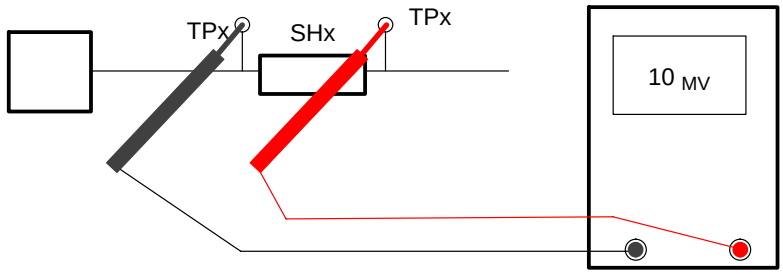
D.3.1 Connecting a Voltmeter to Measure Voltage Drop

Voltmeter Power and Ground

Insure that the voltmeter used is either battery powered or if AC powered, that the ground of the meter is isolated from the earth and system ground. We don't want to tie one side of the resistor to ground while attempting the test . It results in shorting out the voltage supply.

1) Power off the system.
2) Set the meter to the Mv setting
3) Set the scale to 1000 mv
4) Connect the voltmeter as shown in Figure D−1:

Figure D−1. Connecting Voltmeter to Measure Voltage



5) Turn on the system power.
6) The voltage displayed is in mV. A display of 10 mV is equal to 100 ma.

D.3.2 Connecting an Oscilloscope to Measure Voltage Drop

Oscilloscope Power and Ground

Insure that the Oscilloscope used is either battery powered or if AC powered, that the ground of the scope is isolated from the earth and system ground. We don't want to tie one side of the resistor to ground while attempting the test. It results in shorting out the voltage supply.

This test takes two probes for the test. It takes the voltage measured at TPx and add it to the inverted level measured at TPy, giving the differential voltage between the two points displayed on the Oscilloscope.

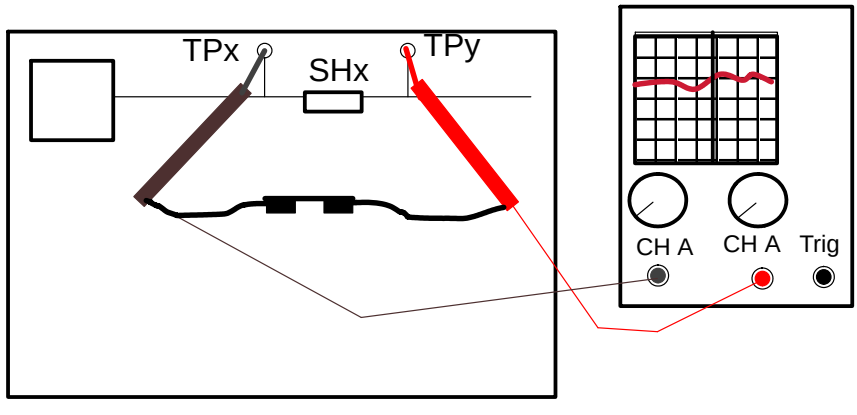
1) Power off the system.

2) Set the Oscilloscope as follows:

   a) A channel to DC
   b) B channel to DC
   c) Set trigger source as A
   d) Set A channel to .01 V/DIV
   e) Set B channel to .01 V/DIV
   f) Set B channel to inverted
   g) Set A channel + B channel (Add)
   h) Set to .1 Sec/Div (Various settings are OK)

3) Connect the Oscilloscope as shown in Figure D−2:

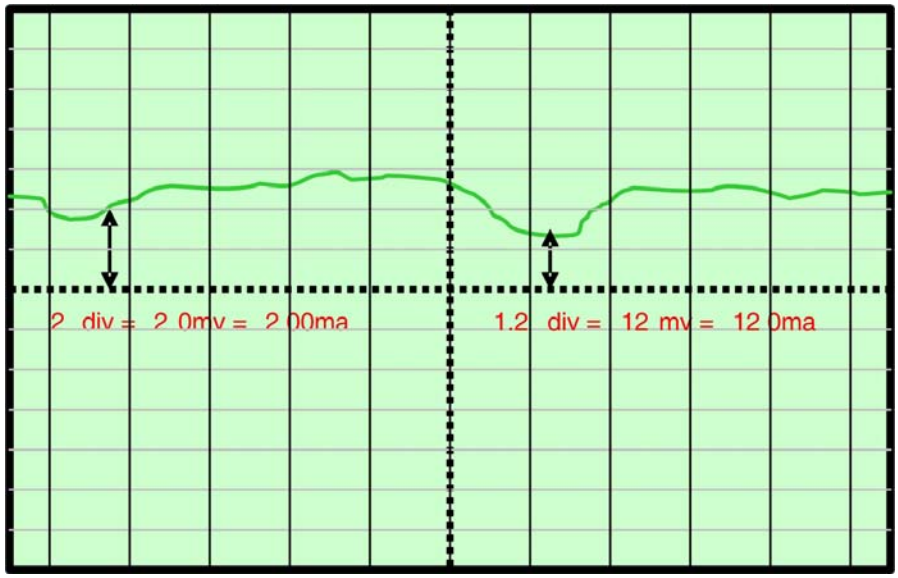
Figure D−2. Connecting Oscilloscope to Measure Voltage



4) Turn on the system power.

5) The voltage displayed is in mV. A display of 10 mV is equal to 100 ma.

6) Current can be measured over time by getting the value at any point across the trace. As current loads change, the voltage display changes. An example scope display is shown below.



D.3.3 Connecting an Oscilloscope to Trigger Data Collection

Another function of the oscilloscope is to trigger the collection of data. This can be useful when you want to measure the current based upon an event from software or during a specific period where the software is in a particular piece of code.

The following procedure shows how to set things up for this technique. This requires a 4-channel scope.

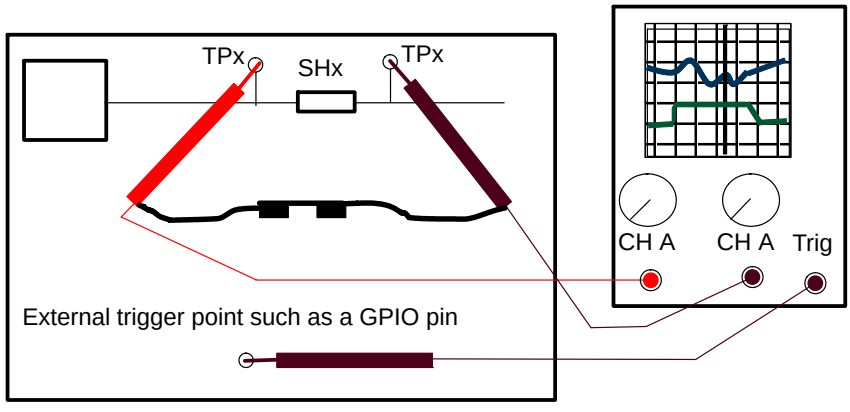
1) Power off the system.

2) Set the Oscilloscope as follows:

   a) A channel to dc
   b) B channel to dc
   c) Set trigger source as external
   d) Set A channel to .01 V/DIV
   e) Set B channel to .01 V/DIV
   f) B channel inverted
   g) Set A channel + B channel
   h) Set to .1 Sec/Div

3) Connect the Oscilloscope as shown in Figure D−3:

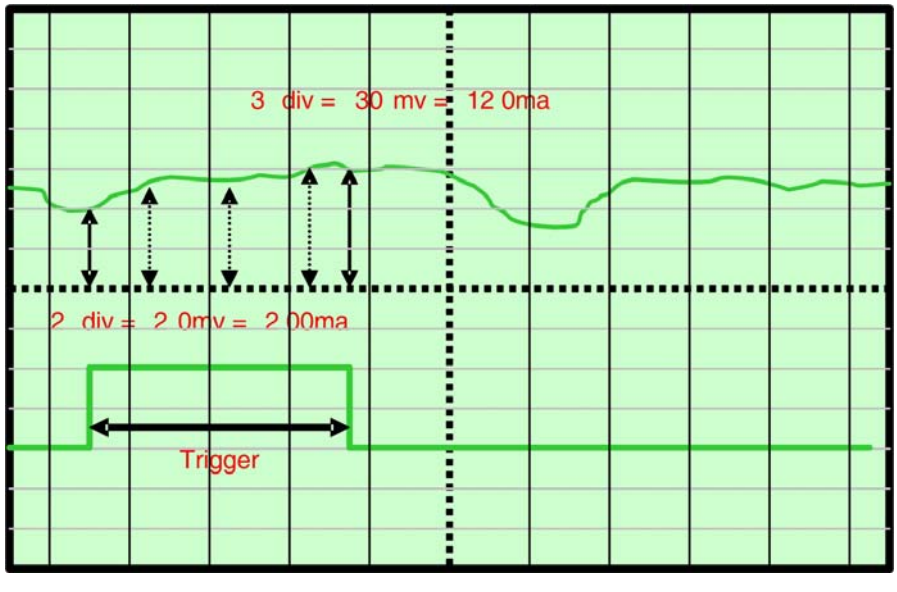
Figure D−3. Connecting Oscilloscope for Data Collection



4) Turn on the system power.

5) The voltage displayed is in mV. A display of .100 mV is equal to 10 ma.

6) Using the storage mode of the scope, current can be measured during the event or triggered by the event. As current loads change, the voltage display changes. An example scope display is shown below.



By measuring the voltage at multiple points within the trigger window, the average current can be calculated.

Index

D

E

F

G

H

I

J

L

M

N

O

P

R

S

T

U

V

X