TMS320DM355 Digital Media System-on-Chip (DMSoC) Peripherals Overview

Reference Guide

TEXAS INSTRUMENTS

Contents

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About This Manual

Provides an overview of the peripherals supported in the TMS320DM355 Digital Media System-on-Chip (DMSoC).

Related Documentation From Texas Instruments

The following documents describe the TMS320DM35x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the internet at www.ti.com.

SPRS463 — *TMS320DM355 Digital Media System-on-Chip (DMSoC) Data Manual* This document describes the overall TMS320DM355 system, including device architecture and features, memory map, pin descriptions, timing characteristics and requirements, device mechanicals, etc.

SPRZ264 — *TMS320DM355 DMSoC Silicon Errata* Describes the known exceptions to the functional specifications for the TMS320DM355 DMSoC.

SPRUFB3 — *TMS320DM35x Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* This document describes the ARM Subsystem in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the components of the ARM Subsystem, the peripherals, and the external memories.

SPRUED1 — *TMS320DM35x Digital Media System-on-Chip (DMSoC) Asynchronous External Memory Interface (EMIF) Reference Guide* This document describes the asynchronous external memory interface (EMIF) in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The EMIF supports a glueless interface to a variety of external devices.

SPRUED2 — *TMS320DM35x Digital Media System-on-Chip (DMSoC) Universal Serial Bus (USB) Controller Reference Guide* This document describes the universal serial bus (USB) controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices and also supports host negotiation.

SPRUED3 — *TMS320DM35x Digital Media System-on-Chip (DMSoC) Audio Serial Port (ASP) Reference Guide* This document describes the operation of the audio serial port (ASP) audio interface in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The primary audio modes that are supported by the ASP are the AC97 and IIS modes. In addition to the primary audio modes, the ASP supports general serial port receive and transmit operation, but is not intended to be used as a high-speed interface.

SPRUED4 — *TMS320DM35x Digital Media System-on-Chip (DMSoC) Serial Peripheral Interface (SPI) Reference Guide* This document describes the serial peripheral interface (SPI) in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

SPRUED9 — *TMS320DM35x Digital Media System-on-Chip (DMSoC) Universal Asynchronous Receiver/Transmitter (UART) Reference Guide* This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

SPRUEE0 — *TMS320DM35x Digital Media System-on-Chip (DMSoC) Inter-Integrated Circuit (I2C) Peripheral Reference Guide* This document describes the inter-integrated circuit (I2C) peripheral in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit and receive up to 8-bit wide data to and from the DMSoC through the I2C peripheral. This document assumes the reader is familiar with the I2C-bus specification.

SPRUEE2 — *TMS320DM35x Digital Media System-on-Chip (DMSoC) Multimedia Card (MMC)/Secure Digital (SD) Card Controller Reference Guide* This document describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The MMC/SD card is used in a number of applications to provide removable data storage. The MMC/SD controller provides an interface to external MMC and SD cards. The communication between the MMC/SD controller and MMC/SD card(s) is performed by the MMC/SD protocol.

SPRUEE4 — *TMS320DM35x Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Reference Guide* This document describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The EDMA controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DMSoC.

SPRUEE5 — *TMS320DM35x Digital Media System-on-Chip (DMSoC) 64-bit Timer Reference Guide* This document describes the operation of the software-programmable 64-bit timers in the TMS320DM35x Digital Media System-on-Chip (DMSoC). Timer 0, Timer 1, and Timer 3 are used as general-purpose (GP) timers and can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode; Timer 2 is used only as a watchdog timer. The GP timer modes can be used to generate periodic interrupts or enhanced direct memory access (EDMA) synchronization events and Real Time Output (RTO) events (Timer 3 only). The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

SPRUEE6 — *TMS320DM35x Digital Media System-on-Chip (DMSoC) General-Purpose Input/Output (GPIO) Reference Guide* This document describes the general-purpose input/output (GPIO) peripheral in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of the input by reading the state of an internal register. When configured as an output, you can write to an internal register to control the state driven on the output pin.

SPRUEE7 — *TMS320DM35x Digital Media System-on-Chip (DMSoC) Pulse-Width Modulator (PWM) Reference Guide* This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRUEH7 — *TMS320DM35x Digital Media System-on-Chip (DMSoC) DDR2/Mobile DDR (DDR2/mDDR) Memory Controller Reference Guide* This document describes the DDR2/mDDR memory controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC). The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM and mobile DDR devices.

SPRUF71 — *TMS320DM35x Digital Media System-on-Chip (DMSoC) Video Processing Front End (VPFE) Reference Guide* This document describes the Video Processing Front End (VPFE) in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRUF72 *— TMS320DM35x Digital Media System-on-Chip (DMSoC) Video Processing Back End (VPBE) Reference Guide* This document describes the Video Processing Back End (VPBE) in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRUF74 *— TMS320DM35x Digital Media System-on-Chip (DMSoC) Real-Time Out (RTO) Controller Reference Guide* This document describes the Real Time Out (RTO) controller in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRUFC8 *— TMS320DM35x Digital Media System-on-Chip (DMSoC) Peripherals Overview Reference Guide* This document provides an overview of the peripherals in the TMS320DM35x Digital Media System-on-Chip (DMSoC).

SPRAAR3 *— Implementing DDR2/mDDR PCB Layout on the TMS320DM35x DMSoC* This provides board design recommendations and guidelines for DDR2 and mobile DDR.

SPRAAR7 *— USB 2.0 Board Design and Layout Guidelines* This provides board design recommendations and guidelines for high speed USB.

TMS320DM355 DMSoC Peripherals Overview

1 Overview

The TMS320DM355 Digital Media System-on-Chip (DMSoC) is a highly-integrated hardware and software platform, designed to meet the application processing needs of next-generation embedded devices. The DM355 DMSoC enables OEMs and ODMs to quickly bring to market devices featuring rich user interfaces, high-processing performance, and long battery life through the maximum flexibility of a fully-integrated mixed-processor solution.

The user-accessible peripherals available on the DM355 DMSoC are configured using a set of memory-mapped control registers. The peripheral bus controller performs the arbitration for accesses of on-chip peripherals. Peripherals available on the DM355 DMSoC and their associated literature number are listed in Table 1.

Table 1. TMS320DM355 DMSoC Peripherals Documentation

Peripheral/Module	Acronym	Lit #
Asynchronous External Memory Interface	EMIF	SPRUED1
Audio Serial Port	ASP	SPRUED3
DDR2 Memory Controller	DDR2	SPRUEH7
Enhanced Direct Memory Access Controller	EDMA	SPRUEE4
General-Purpose Input/Output	GPIO	SPRUEE6
Inter-Integrated Circuit Module	I2C	SPRUEE0
Multimedia Card/Secure Digital Card Controller	MMC/SD	SPRUEE2
Pulse-Width Modulator	PWM	SPRUEE7
Serial Peripheral Interface	SPI	SPRUED4
64-Bit Timer	Timer	SPRUEE5
Universal Asynchronous Receiver/Transmitter	UART	SPRUED9
Universal Serial Bus	USB	SPRUED2
Video Processing Back End	VPBE	SPRUF72
Video Processing Front End	VPFE	SPRUF71
Real Time Out	RTO	SPRUF74

2 Asynchronous External Memory Interface (EMIF)

The asynchronous external memory interface (EMIF) provides a means to connect to a variety of external devices including:

- NAND Flash
- Asynchronous devices including Flash and SRAM
- OneNAND flash

The most common use for the EMIF is to interface with both Flash devices and SRAM devices. The EMIF includes many features to enhance the ease and flexibility of connecting to external asynchronous devices. The EMIF features includes support for:

- Two addressable chip select spaces of up to 64KB each
- 8-bit and 16-bit data bus widths
- Programmable cycle timings such as setup, strobe, and hold times as well as turnaround time
- Select strobe mode
- Extended Wait mode
- NAND 1-bit and 4-bit Flash ECC generation
- Data Bus Parking

3 Audio Serial Port (ASP)

The audio serial port (ASP) is used for audio interface purposes. The primary audio modes that are supported by the ASP are the AC97 and IIS modes. In addition to the primary audio modes, the ASP supports general serial port receive and transmit operation, but is not intended to be used as a high-speed interface. The ASP can be controlled by the ARM CPU.

The ASP provides the following functions:

- Full-duplex communication
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected analog-to-digital (A/D) and digital-to-analog (D/A) devices
- External shift clock or an internal, programmable frequency shift clock for data transfer

In addition, the ASP has the following capabilities:

- Direct interface to:
  - AC97 compliant devices (the necessary multiphase frame synchronization capability is provided)
  - IIS compliant devices
  - SPI protocol (master mode only)
- A wide selection of data sizes, including 8, 12, 16, 20, 24, and 32 bits
- μ-Law and A-Law companding
- 8-bit data transfers with the option of LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation

4 DDR2/mDDR Memory Controller

The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM devices and standard Mobile DDR SDRAM devices. Memories types such as DDR1 SDRAM, SDR SDRAM, SBSRAM, and asynchronous memories are not supported. The DDR2/mDDR memory is the major memory location for program and data storage in the DM355 system.

The DDR2/mDDR memory controller supports the following features:

- JESD79D-2A standard compliant DDR2 SDRAM

- Standard compliant Mobile DDR
- 256 Mbyte memory space
- Data bus width of 16 bits
- CAS latencies:
  - DDR2: 2, 3, 4, and 5
  - mDDR: 2 and 3
- Internal banks:
  - DDR2: 1, 2, 4, and 8
  - mDDR: 1, 2, and 4
- Burst length: 8
- Burst type: sequential
- 1 CS signal
- Page sizes: 256, 512, 1024, and 2048
- SDRAM auto-initialization
- Self-refresh mode
- Partial array self-refresh (for mDDR)
- Power down mode
- Prioritized refresh
- Programmable refresh rate and backlog counter
- Programmable timing parameters
- Little endian

5   Enhanced Direct Memory Access (EDMA) Controller

The enhanced direct memory access (EDMA) controller handles all user-programmed data transfers between two slave endpoints on the device. The EDMA enables movement of data to/from any addressable memory spaces (internal/external), slave peripherals. The EDMA on the TMS320DM355 DMSoC has a different architecture from previous EDMA controllers on the C621x/C671x and C64x devices, it includes several enhancements over the previous EDMA controller and provides enhanced debug visibility and error reporting.

The EDMA controller has two principal blocks:
- EDMA channel controller
- EDMA transfer controller(s)

The EDMA channel controller primarily serves as the user interface for the EDMA controller. It also serves as event interface for the EDMA controller and is responsible for event latch-up, event prioritization, queue management, and transfer request (TR) submission to the EDMA transfer controllers. The EDMA transfer controllers are primarily responsible for data movement. The transfer controller is responsible for issuing read/write commands to the slaves.

6   General-Purpose Input/Output (GPIO)

The general-purpose input/output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of an internal register.

The GPIO peripheral consists of the following features.

- Output set/clear functionality through separate data set and clear registers allows multiple software processes to control GPIO signals without critical section protection.
- Set/clear functionality through writing to a single output data register is also supported.
- Separate input/output registers
  - Output register can be read to reflect output drive status.

    – Input register can be read to reflect pin status.
- All GPIO signals can be used as interrupt sources with configurable edge detection.
- All GPIO signals can be used to generate events to the EDMA.
- Programmable debounce circuit provided on GPIO[7:0].

7 Inter-Integrated Circuit (I2C) Module

The inter-integrated circuit (I2C) module provides an interface between the TMS320DM355 DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit and receive up to 8-bit wide data to and from the DM355 DMSoC through the I2C module.

The I2C module has the following features:
- Compliance with the Philips Semiconductors I2C-bus specification (version 2.1):
  - Support for byte format transfer
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers mode
  - Support for multiple slave-transmitters and master-receivers mode
  - Combined master transmit/receive and receive/transmit mode
  - I2C data transfer rate of from 10 kbps up to 400 kbps (Philips I2C rate)
- 2 to 7 bit format transfer
- Free data format mode
- One read DMA event and one write DMA event that can be used by the DMA
- Seven interrupts that can be used by the CPU
- Module enable/disable capability

8 Multimedia Card (MMC)/Secure Digital (SD) Card Controller

The multimedia card (MMC)/secure digital (SD) card is used in a number of applications to provide removable data storage. The MMC/SD card controller provides an interface to external MMC and SD cards. The communication between the MMC/SD card controller and MMC/SD card(s) is performed by the MMC/SD protocol.

The MMC/SD card controller has the following features:
- Supports interface to multimedia cards (MMC)
- Supports interface to Secure Digital (SD) memory cards
- Ability to use the MMC/SD protocol and Secure Digital Input Output (SDIO) protocol
- Programmable frequency of the clock that controls the timing of transfers between the MMC/SD card controller and memory card
- 256-bit read/write FIFO to lower system overhead
- Signaling to support enhanced direct memory access (EDMA) transfers (slave)
- 50 MHz maximum clock to SD (specification version 1.1)

9 Pulse-Width Modulator (PWM)

The pulse-width modulator (PWM) peripheral is very common in embedded systems. It provides a way to generate a pulse periodic waveform for motor control or can act as a digital-to-analog converter with some external components. This PWM peripheral is basically a timer with a period counter and a first-phase duration comparator, where bit width of the period and first-phase duration are both programmable.

The PWM peripheral has the following features:
- 32-bit period counter

- 32-bit first-phase duration counter
- 8-bit repeat counter for one-shot operation. One-shot operation will produce N + 1 periods of the waveform, where N is the repeat counter value.
- Configurable to operate in either one-shot or continuous mode.
- One-shot operation can be triggered by the CCD VSYNC output of the video processing subsystem to allow any of the PWM instantiations to be used as a CCD timer.
- Configurable PWM output pin inactive state.
- Interrupt and enhanced direct memory access (EDMA) synchronization events.

10   Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the TMS320DM355 DMSoC at a programmed bit-transfer rate. The SPI is normally used for communication between the DM355 DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

The SPI allows serial communication with other SPI devices through a 3-pin or 4-pin mode interface. The DM355 DMSoC implementation supports multichip-select operation for up to two SPI slave devices. The SPI operates as a master SPI device only.

The SPI has the following features:
- 16-bit shift register
- Receive buffer register
- 8-bit clock prescaler
- Programmable SPI clock frequency range
- Programmable character length (2 to 16 bits)
- Programmable clock phase (delay or no delay)
- Programmable clock polarity (high or low)

11   64-Bit Timer

TheTMS320DM355 DMSoC processor contains four software-programmable 64-bit timers (Timer 0, Timer 1, Timer 2, and Timer 3). Timer 0, Timer 1, and Timer 3 are used as general-purpose timers and can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode; Timer 2 is used only as a watchdog timer. The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop. Timer 3 supports the following additional features that are not available in the other timers:
- External clock/event input
- Period reload
- output event tied to Real Time Output (RTO) module
- external event capture
- timer counter register read reset

The 64-bit timer has the following features:
- 64-bit count-up counter
- Timer modes:
  - 64-bit general-purpose timer mode
  - Dual 32-bit general-purpose timer mode
  - Watchdog timer mode
- Two possible clock sources:
  - Internal clock
  - External clock/event input via timer input pins (Timer 3 only)
- Three possible operation modes:

– One-time operation (timer runs for one period then stops)
– Continuous operation (timer automatically resets after each period)
– Continuous operation with period reload (Timer 3 only)
• Generates interrupts to the ARM CPU
• Generates sync event to EDMA
• Generates output event to device reset (Timer 2 only)
• Generates output event to Real Time Out (RTO) module (Timer 3 only)
• External event capture via timer input pins (Timer 3 only)

12   Universal Asynchronous Receiver/Transmitter (UART)

This universal asynchronous receiver/transmitter (UART) peripheral performs serial-to-parallel conversion on data received from a peripheral device or modem, and parallel-to-serial conversion on data received from the TMS320DM355 DMSoC processor CPU or DMA. The CPU can read the UART status at any time. The UART includes control capability and a processor interrupt system that can be tailored to minimize software management of the communications link.

The UART peripheral has the following features:
• Programmable baud rates (frequency pre-scale values from 1 to 65535)
• Fully programmable serial interface characteristics:
    – 5, 6, 7, or 8-bit characters
    – Even, odd, or no PARITY bit generation and detection
    – 1, 1.5, or 2 STOP bit generation
• 16-byte depth transmitter and receiver FIFOs:
    – The UART can be operated with or without the FIFOs
    – 1, 4, 8, or 14 byte selectable receiver FIFO trigger level for autoflow control and DMA
• DMA signaling capability for both received and transmitted data
• CPU interrupt capability for both received and transmitted data
• False START bit detection
• Line break generation and detection
• Internal diagnostic capabilities:
    – Loopback controls for communications link fault isolation
    – Break, parity, overrun, and framing error simulation
• Programmable autoflow control using RTS and CTS signals for UART2
• Modem control functions (CTS, RTS) for UART2. No Modem control functions are available for UART0 and UART1.

13   Universal Serial Bus (USB)

The universal serial bus (USB) controller in the TMS320DM355 DMSoC supports high-speed USB device mode and high-speed limited host mode operations. The USB controller can be operated by the ARM through the memory-mapped registers.

The USB has the following features:
• Supports USB 2.0 peripheral at high speed (480 Mbps) and full speed (12 Mbps)
• Supports USB 2.0 host at high speed (480 Mbps), full speed (12 Mbps), and low speed (1.5 Mbps)
• Supports 4 simultaneous transmit (TX) and 4 receive (RX) endpoints, more can be supported by dynamically switching
• Each endpoint can support all transfer types (control, bulk, interrupt, and isochronous)
• Supports USB extensions for session request (SRP) and host negotiation (HNP)
• Includes a 4K endpoint FIFO RAM, and supports programmable FIFO sizes
• External 5V power supply for VBUS can be controlled through I2C

- Includes a DMA controller that supports 4 transmit (TX) and 4 receive (RX) DMA channels
- Includes RNDIS mode of DMA for accelerating RNDIS-type protocols using short packet termination over USB

14 Video Processing Back End (VPBE)

The video processing back-end (VPBE) block is comprised of the on-screen display (OSD) and the video encoder (VENC) modules. Together, these modules provide DM35x with a powerful and flexible back-end display interface. These are described below:

- The on-screen display (OSD) graphic accelerator manages display data in various formats for several types of hardware display windows and handles the blending of the display windows into a single display frame, which is then output by the video encoder module.
- The video encoder (VENC) takes the display frame from the OSD and formats it into the desired output format and output signals, including data, clocks, sync, etc. required to interface to display devices. The VENC consists of three primary sub-blocks:
  - The analog video encoder generates the signaling, including video A/D conversion, to interface to NTSC/PAL television displays.
  - The digital LCD controller supports interfaces to various digital LCD display formats as well as standard digital YUV outputs to interface to Hi-Def video encoders and/or DVI/HDMI interface devices.
  - The timing generator to generate the specific timing required for analog video output as well as various digital video output modes.

14.1 On Screen Display (OSD) Features

The primary function of the OSD module is to gather and blend video data and display/bitmap data and then pass it to the video encoder (VENC) in YCbCr format. The video and display data is read from external DDR2/mDDR memory. The OSD is programmed via control and parameter registers. The following are the primary features that are supported by the OSD:

- Support for two video windows and two OSD bitmapped windows that can be displayed simultaneously (VIDWIN0/VIDWIN1 and OSDWIN0/OSDWIN1)
- Video windows support YCbCr data in 422 format from external memory, with the ability to interchange the order of the CbCr component in the 32-bit word
- OSD bitmap windows support 1/2/4/8 bit width index data of color palette
- In addition, one OSD bitmap window at a time can be configured to one of the following:
  - YUV422 (same as video data)
  - RGB format data in 16-bit mode (R=5bit, G=6bit, B=5bit)
  - 24-bit mode (each R/G/B=8bit) with pixel level blending with video windows
- Programmable color palette with the ability to select between a RAM/ROM table with support for 256 colors.
- Support for two ROM tables, one of which can be selected at a given time
- Separate enable/disable control for each window
- Programmable width, height, and base starting coordinates for each window
- External memory address and offset registers for each window
- Support for x2 and x4 zoom in both the horizontal and vertical direction
- Pixel-level blending/transparency/blinking attributes can be defined for OSDWIN0 when OSDWIN1 is configured as an attribute window for OSDWIN0
- Support for blinking intervals to the attribute window
- Ability to select either field/frame mode for the windows (interlaced/progressive)
- An eight-step blending process between the bitmap and video windows
- Transparency support for the bitmap and video data (when a bitmap pixel is zero, there will be no blending for that corresponding video pixel)
- Ability to resize from VGA to NTSC/PAL (640x480 to 720x576) for both the OSD and video windows
- Horizontal rescaling x1.5 is supported

- Support for a rectangular cursor window and a programmable background color selection
- The width, height, and color of the cursor is selectable
- The display priority is: Rectangular-Cursor > OSDWIN1 > OSDWIN0 > VIDWIN1 > VIDWIN0 > background color
- Support for attenuation of the YCbCr values for the REC601 standard.

The following restrictions exist in the OSD module:

- If the vertical resize filter is enabled for either of the video windows, the maximum horizontal window dimension cannot be greater than 720 currently. This is due to the limitation in the size of the line memory.
- It is not possible to use both of the CLUT ROMs at the same time. However, a window can use RAM while another uses ROM.

14.2 Video Encoder (VENC) Features

The VENC/DLCD consists of three major blocks: a) the video encoder that generates analog video output, b) the digital LCD controller that generates digital RGB/YCbCr data output and timing signals, and c) the timing generator.

The analog video encoder features are described below
- Master clock Input-27MHz (x2 upsampling)
- SDTV Support
  - Composite NTSC-M, PAL-B/D/G/H/I
  - CGMS/WSS attribute insertion
  - Line 21 Closed caption data encoding
  - Chroma low-pass filter 1.5 MHz/3 MHz
  - Programmable SC-H phase
- 10-bit oversampling D/A converters (27 MHz)
- Optional 7.5% pedestal
- 16-235/0-255 input amplitude selectable
- Programmable luma delay
- Master/slave operation
- Internal color bar generation (100%/75%)

The digital LCD interface features are described below
- Programmable DCLK
- Various output formats
  - YCbCr 16-bit
  - YCbCr 8-bit
  - ITU-R BT. 656
  - Parallel RGB (16/18 bit)
  - Serial RGB
- Low-pass filter for digital RGB output
- Programmable timing generator
- Master/slave operation
- Internal color bar generation (100%/75%)
- 8-bit programable gamma correction

15   Video Processing Front End (VPFE)

The VPFE or Video Processing Front-End block is comprised of the CCD Controller (CCDC), Image Pipe (IPIPE), Image Pipe Interface (IPIPEIF), and Hardware 3A Statistic Generator (H3A) blocks. Together, these modules provide the DM355 with a powerful and flexible front-end interface. These modules can be broken down into 2 distinct types. The first type consists of major processing modules that are in the direct data flow path and affect the input image data stream. These are described below:

15.1   CCD Controller (CCDC)

The CCDC is responsible for accepting RAW (unprocessed) image/video data from a sensor (CMOS or CCD). In addition, the CCDC can accept YCbCr video data in numerous formats, typically from so-called video decoder devices. In the case of RAW inputs, the CCDC output requires additional image processing to transform the RAW input image to the final processed image. This processing can be done in the Image Pipe. The CCDC is programmed via control and parameter registers. The following features are supported by the CCDC module.

- Support for conventional Bayer pattern sensor format.
- Support for complimentary color pattern input via a color space converter.
- Generates HD/VD timing signals to an external timing generator or can synchronize to the external timing generator.
- Support for progressive and interlaced sensors (hardware support for up to 2 fields and firmware support for higher number of fields, typically 3-, 4-, and 5-field sensors).
- Support for up to 75-MHZ sensor pixel clock, if H3A is not used; otherwise, the pixel clock must be less than 67.5 MHZ.
- Support for ITU-R BT.656 standard format, either 8-bit or 10-bit.
- Support for YCbCr422 format, either 8-bit or 16-bit with discrete H and VSYNC signals.
- Support for up to 14-bit raw data from a CCD/CMOS sensor.
- Generates optical black clamping signals.
- Support for shutter signal control.
- Support for digital clamping and black level compensation.
- Defect correction based on a lookup table that contains row and column position of the pixel to be corrected.
- Programmable Lens Shading Correction.
- Support for 10-bit to 8-bit A-law compression.
- Support for a low-pass filter prior to writing to SDRAM. If this filter is enabled, 2 pixels each in the left and right edges of each line are cropped from the output.
- Support for generating output to range from 14-bits to 8-bits wide (8-bits wide allows for 50% saving in storage area).
- Support for downsampling via programmable culling patterns.
- Ability to control output to the DDR2/mDDR controller via an external write enable signal.
- Supported maximum CCD imager size is 32,768 × 32,768.

15.2 Image Pipe – Hardware Image Signal Processor (IPIPE)

The Image Pipe (IPIPE) is a programmable hardware image processing module that generates image data in YCbCr-4:2:2 format from raw CCD/CMOS data. The IPIPE can also be configured to operate in a resize only mode, which allows YCbCr-4:2:2 to be resized without applying the processing of every module in the IPIPE. The following features are supported by the IPIPE.

- Support for 14 bit RAW data image processing or 16 bit YCbCr resizing
- Support RGB Bayer pattern for input color filter array. (Support for complementary CMYG pattern is also provided via the Color Space Converter.)
- Require at least 8 pixels for horizontal blanking and 4 lines for vertical blanking. In one shot mode, 10 blanking lines after processing area are required.
- Maximum horizontal and vertical offset of IPIPE processing area from synchronous signal is 8191.
- Support for a maximum input and output widths up to 1344 pixels wide (640 for RSZ[1]).
- Support dark frame subtract in IPIPEIF by providing a raw pass-though mode supporting images wider than 1344 pixels.
- Support for automatic mirroring of pixels/lines when edge processing is performed so that the width and height is consistent throughout.
- Defect correction based on a lookup table that contains row and column position of the pixel to be corrected.
- Horizontal /Vertical noise reduction filter
- Gain control for white balancing at each component
- CFA interpolation for good quality CFA interpolation with reduced false color artifacts
- Programmable RGB-to-RGB blending matrix (9 coefficients for the 3×3 matrix).
- Programmable coefficients for RGB to YCbCr conversion
- Programmable lookup table for Luminance edge enhance
- Faulty-color suppression filter
- Programmable down or up-sampling filter for both horizontal and vertical directions with range from 1/16x to 8x, in which the filter outputs two images with different magnification simultaneously.
- Flipping image vertically and/or horizontally
- RGB (32bit/16bit) output to SDRAM
- Programmable Histogram engine (4 windows, 256 bins)
- Boxcar calculation

15.3 Hardware 3A (H3A)

The H3A module is designed to support the control loops for Auto Focus, Auto White Balance and Auto Exposure by collecting metrics about the imaging/video data. The metrics are to adjust the various parameters for processing the imaging/video data. There are 2 main blocks in the H3A module:

- Auto Focus Engine
- Auto Exposure & Auto White Balance Engine

The AF engine extracts and filters the red, green, and blue data from the input image/video data and provides either the accumulation or peaks of the data in a specified region. The specified region is a two-dimensional block of data and is referred to as a "paxel" for the case of AF.

The AE/AWB Engine accumulates the values and checks for saturated values in a sub sampling of the video data. In the case of the AE/AWB, the two-dimensional block of data is referred to as a "window". Thus, other than referring them by different names, a paxel and a window are essentially the same thing. However, the number, dimensions, and starting position of the AF paxels and the AE/AWB windows are separately programmable.

15.3.1 Auto Focus Engine Features

The following features are supported by the AF engine.

- Support for a Peak Mode in a Paxel (a Paxel is defined as a two dimensional block of pixels).
  - Accumulate the maximum Focus Value of each line in a Paxel
- Support for an Accumulation/Sum Mode (instead of Peak mode).
- Support for an Accumulation/Sum Mode (instead of Peak mode).
- Support for up to 36 Paxels in the horizontal direction and up to 128 Paxels in the vertical direction.
- Programmable width and height for the Paxel. All paxels in the frame will be of same size.
- Programmable red, green, and blue position within a 2×2 matrix.
- Separate horizontal start for paxel and filtering.
- Programmable horizontal and vertical line increments within a paxel.
- Parallel IIR filters configured in a dual-biquad configuration with individual coefficients (2 filters with 11 coefficients each). The filters are intended to compute the sharpness/peaks in the frame to focus on.

15.3.2 Auto Exposure and Auto White Balance Features

The following features are supported by the AE/AWB engine.

- Accumulate clipped pixels along with all non-saturated pixels.
- Support for up to 36 horizontal windows and up to 128 vertical windows..
- Programmable width and height for the windows. All windows in the frame will be of same size.
- Separate vertical start coordinate and height for a black row of paxels that is different than the remaining color paxels.
- Programmable Horizontal Sampling Points in a window
- Programmable Vertical Sampling Points in a window

15.4 Image Pipe Interface (IPIPEIF)

The Image Pipe Input Interface module is an input extension to the Image Pipe. It can receive data from the CCDC, SDRAM, or both (darkframe subtract) and pass the data to the IPIPE. Depending on the functions performed, it may also readjust the HD, VD, and PCLK timing to the IPIPE input.

- Supports dark-frame subtract of raw image stored in DDRAM from image from CCDC
- Supports inverse ALAW decompression of RAW data from DDRAM.
- Supports (1,2,1) average filtering before horizontal decimation
- Supports horizontal decimation (downsizing) of input lines to <= 1344 maximum required by the Image Pipe
- Supports gain multiply for raw data

IMPORTANT NOTICE